Design of a Rad-Hard Library of Digital Cells for Space Applications

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Abstract—This paper proposes a design methodology for a digital library of cells resistant to cosmic radiation. Most important effects due to radiation are avoided or mitigated using ad hoc design techniques. Fault injection techniques are used to validate the design. Simulations results demonstrate that the cells designed in a 180 nm CMOS technology are tolerant to 1.5 mA current peak due to interaction with a single high-energy particle.

I. INTRODUCTION

During last decades, design techniques for integrated circuits have brought tremendous evolution, leading to reduction in components size and improvement in performance. However, niche sectors exist in the world, where the conventional technology is not immediately applicable. An example is the electronics for aerospace applications. Space environment is plenty of radiations, which do not reach the earth surface, due to the mitigating effect of atmosphere. Therefore, design methodologies for aerospace applications are different from design methodologies for commercial electronics.

Cosmic radiations cause various kinds of phenomena, that can be divided into two major categories: cumulative effects, due to a long-time exposure to radiation, and single event effects, due to interaction with a single particle.

Cumulative effects can be divided into Total Ionizing Dose (TID) effects, caused by charged particles (e.g., electrons or protons), and Displacement Damage Dose (DDD) effects, caused by neutral particles (e.g., neutrons). TID effects are due to electron-hole pairs created in the oxide layer by radiations crossing the integrated circuit. The holes remain trapped within the oxide for a long time [1]. Further, channel carriers can be trapped within Si-SiO₂ interface. These effects cause variations in transistor parameters, e.g., increase or decrease of threshold voltage, increase of parasitic currents, decrease of carrier mobility and transconductance, etc. DDD effects are due to collisions between neutral particles and nuclei of silicon belonging to the lattice structure [2]. These collisions may create vacancies into the silicon lattice, introducing energy states in the band-gap. These trap states facilitate electron transitions between valence band and conduction band, and a mobility degradation is observed [3].

Single event effects (SEE) can be divided into two categories. Soft errors are non-destructive, temporary effects: for instance, the wrong flipping of bit (Single Event Upset (SEU), or Single Event Transient (SET) [4]). Hard errors are destructive, hence they cause irreversible effects (e.g., Single Event Latch-up (SEL) [5]). The scientific literature proposes a large number of techniques to avoid or mitigate damaging effects due to cosmic radiations [6]-[9]. This paper describes several techniques “by-design” that may be adopted with conventional fabrication process. These techniques are used at circuit and layout description level. Especially, in circuit description, the number of feedback loops is minimized, while in layout description, guard-rings are used to avoid Single Event Latch-up (SEL), and Edge-Less Transistors (ELT) are used to avoid leakage currents. In addition, latch circuit nodes are designed with large capacitance to avoid Single Event Upset (SEU). Finally, fault injection analysis and simulations are used to evaluate the effectiveness of the proposed approach.

II. CUMULATIVE EFFECT SOLUTIONS

In integrated circuits, the region most sensitive to cumulative effects is the gate oxide. When a single particle collides with the oxide, electron-hole pairs are created. The number of pairs created is directly proportional to Linear Energy Transfer (LET) from particle to target material. When the ionized region is crossed by an electric field, electrons and holes are separated. Electrons are quickly collected by nearer electrodes, while holes remain trapped into the oxide for a long time. These trapped holes can be seen as fixed positive charges. Obviously, these fixed positive charges introduce a negative shift in threshold voltage.

![Fig. 1. Positive charged particles trapped into the “bird’s beak” region.](image_url)
Lattice defects at Si-SiO$_2$ interface introduce energy states in band-gap, which may trap channel carriers. About the latter phenomenon, we have to distinguish n-MOS transistors from p-MOS transistors. In n-MOS transistors, threshold voltage shift is positive, because channel carriers have a negative charge. Vice versa, in p-MOS transistors, threshold voltage shift is negative.

Normally, threshold shift increases with gate oxide thickness. For thin gate oxide (i.e., for thickness lower than approximately 3 nm), threshold shift is negligible [10].

Positive charged particles remain trapped also in the field oxide, especially in the region called “bird’s beak”, at the transition between field thick oxide and gate thin oxide (Fig. 1). Positive charged particles trapped in “bird’s beak” region attract negative carries, thus creating a parasitic path between drain and source, in parallel with the MOS transistor channel. A noticeable leakage current between drain and source can be observed if this phenomenon happens near an n-MOS transistor in “off state”. The most interesting solution consists in designing Edge-Less Transistors (ELT) [6]. Fig. 2 shows the pull-down of a two-input NAND gate designed with ELT. In the “bird’s beak” region, the parasitic path is created between two regions belonging to the same node. P-MOS transistors are also designed using a edge-less shape, to easily maintain the ratio between pull-up and pull-down transistor sizes (Fig. 3).

### III. Single Event Effect Solutions

When a high energy particle collides with an IC, it creates a region of electron-hole pairs. If the target region is crossed by an electric field, electrons and holes are separated and a parasitic current results. This parasitic current consists in a fast spike with a high value, followed by a long diffusion time ($\approx$ 1 ns) with a low current value. In addition, this current can easily propagate to other adjacent circuit nodes. Depending on LET, the ionized region may be larger than single node area, and in such case the total current observed in a single node may be due also to parasitic currents generated in other adjacent nodes.

To minimize SET propagation, we have minimized the number of transistors not directly connected to supply and ground voltages. In this case, if SET does not exceed threshold voltage, it cannot propagate towards other logic gates. On the contrary, if we use pass-transistor logic (e.g., the six-transistor XOR logic gate in Fig. 4), SET may propagate to other logical nodes. For this reason, we designed fully-CMOS XOR gates as shown in Fig. 5, in which the number of transistors directly connected to supply or ground voltages is maximized.

We can distinguish two effects depending on LET. If the parasitic charge collected into a node is less than the node critical charge, a voltage transient is observed (SET). On the contrary, if the parasitic charge collected is greater than the...
node critical charge, a logical switch occurs (e.g., SEU). In the latter case, effects can be destructive or non-destructive. Each node has a critical charge value, due to node capacitance and voltage supply. To mitigate single event effects, extra capacitances may be added to sensitive nodes. In this way, critical charge values increase and SEE rate decreases.

To avoid SEU effects, the number of feedback loops must be minimized at circuit description level. Feedback loops may include parasitic components. Among parasitic structures in CMOS ICs, the most important is the thyristor: a PNPN structure which acts as a PNP and an NPN BJT stacked next to each other (Fig. 6) [5]. In a thyristor, when parasitic charge created by a single particle has enough energy to switch on one of the parasitic BJTs, we observe a single event latch-up. Both BJTs are conducting and the structure is forward-biased. Due to the positive feedback loop, the latch-up current may increase to a value high enough to destroy the integrated circuit.

To avoid SEL, physical design must minimize parasitic resistances associated with the PNPN structure. A first rule consists in designing a large number of contacts. A second rule involves the design of n-well and bulk contacts as close as possible to n-well/p-substrate junction, to reduce the resistive path. Overall, we designed a double guard ring structure around any n-well region. Guard rings are composed of p+ implant in the p-substrate and n+ implant inside n-well regions. All guard rings are designed very close to p-n junctions and are biased through as many contacts as possible. Supply metal lines are large, to ensure a large current. Fig. 7 shows a detail of the double guard ring.

IV. Results

We designed a set of logic gates in a 180 nm CMOS technology. In particular, we designed simple gates as INVERTER, NAND, NOR, XOR, and more complex architectures as demultiplexer, Error Correcting Code (ECC) encoder and decoder. All gates have been designed using n-MOS and p-MOS transistors with complementary characteristics. All the transistors of the same type have the same W/L ratio. In all cells, ground and supply voltage metalizations are placed in the same position to simplify routing.

The ten-transistor XOR gate shown in Fig. 5 is the basic block to calculate parity bits required in a Hamming ECC. The XOR is composed by three gates: a NOR2 gate follow by a NAND2 gate driven by an INVERTER. Routing is made using higher metal layers. Fig. 8 shows the layout designed with the rules described in the previous section.

To simulate the behavior of a XOR gate affected by radiations, we use fault injection techniques. Drain current due to single event effect is modeled with a double exponential [11]:

\[ i(t) = \frac{Q}{t_1 - t_2} \left( e^{-t/t_1} - e^{-t/t_2} \right) \]

where \( Q \) is the total injected charge, \( t_1 \) is the collection time of the junction and \( t_2 \) is the time for the ion track. The current is injected in the NOR output (OutNOR node in Fig. 5) at \( t_0 = 1 \) ns when the NOR2 output is at high logic value. Fig. 9 shows simulation results, obtained with two different values of the charge; \( Q = 100\) fC (corresponding to a peak current of 1 mA), and \( Q = 150\) fC (corresponding to a peak current of 1.5 mA). Figs. 9(c) and (d) show the voltage waveforms at OutNOR and Output nodes with 1 mA peak current. We observe a SET occurring at \( t_0 = 1 \) ns in OutNOR node, which does not propagate to Output node. On the contrary, from Figs. 9(e) and (f) we notice that a 1.5 mA peak current causes a logical transient at the OutNOR node, which propagates to
the adjacent Output node. However, parasitic currents do not generate fixed SEU or more damaging SEE.

Overall, to design the entire encoder, XOR gates are stacked as in Fig. 10 and routed with a “Manhattan” strategy with large supply metal lines.

V. CONCLUSION

This paper introduces a rad-hard design methodology for a logic cell library to be used to design integrated circuits for aerospace applications. In particular, we propose solutions to avoid or mitigate more important damaging effect due to radiations. Simulations results demonstrate a sufficient level of radiations hardness for logic cells. Especially, no SEU or SEL are observed for generated peak current up to 1.5 mA.

REFERENCES


