

Experimental Performance of a Highly-Innovative Low-Noise Charge-Sensitive Preamplifier With Integrated Range-Booster

A. Pullia,^{a,b} S. Capra^{a,b*}

^a *University of Milan, Dpt. Of Physics
Via Celoria 16, 20133 Milan, Italy*

^b *INFN of Milan
Via Celoria 16, 20133 Milan, Italy
E-mail: stefano.capra@unimi.it*

ABSTRACT: Integrated charge-sensitive preamplifiers suffer from a reduced available dynamic range respect to discrete-type equivalents. This is due to the limits on maximum supply voltages that modern scaled technologies can tolerate. In this work we present a low-noise low-power integrated charge-sensitive preamplifier (CSP) for solid-state detectors. This device is equipped with an integrated range-booster that can enhance the spectroscopic range of the preamplifier by more than one order of magnitude, enabling high-resolution spectroscopy even if the preamplifier is in deep saturation condition. If the input signals from the detector are under the natural saturation threshold (40 MeV), the preamplifier works in an usual linear way, producing at the output the typical exponential signals. With proper filtering a resolution of approximately 1 keV is achievable. When a large signal from the detector saturates the preamplifier, a sensing circuit detects the saturation and switches the operation mode of the CSP to the “fast-reset mode”. In this mode a constant and controlled current generator discharges the input node of the preamplifier until the normal operating point is reached. Meanwhile an auxiliary circuit similar to a TAC (Time-to-Amplitude converter) retrieves the energy of the signal that caused saturation. Although the natural dynamic range of the CSP is 40 MeV, the fast-reset mode enables for high-resolution spectroscopy (under 0.2% FWHM) up to several hundreds of MeV (700 MeV typically). One issue in this kind of circuits is the dependence of the energy measured with the TAC circuit on the baseline value of the CSP before the “fast-reset event” [5]. As a solution to this problem we propose a correction algorithm implemented inside the TAC block in the form of an analog circuit. On a test-bench a series of large 3 pC charge signals is injected in the input node of the preamplifier through a test capacitor. Before these events, residual charges ranging from 0 to 0.56 pC produce non-zero baseline voltages at the output of the CSP. The TAC with correction not only retrieves correctly the energy of the main event, but also rejects the baseline voltages, leaving the energy measurement unaffected. The fluctuations of the flat-top voltage in the signals produced by the auxiliary TAC circuit due to the different baseline voltages are under the 0.6% of the total signal amplitude.

KEYWORDS: Analogue electronic circuits, Electronic detector readout concepts (solid-state), Front-end electronics for detector readout, VLSI circuits.

* Corresponding author.

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1. Introduction

Modern segmented silicon detectors [1,2] can easily count some hundreds or more total channels. Such devices are generally operated inside the reaction chambers of nuclear physics experiments [3,4] and the readout electronics must comply with very strict parameters. Given the extremely high channel density, the operation in vacuum and the restricted available space for the FEE (Front-End Electronics), integrated solutions for the CSPs (Charge-Sensitive Preamplifiers) are mandatory. These solutions not only allow for very compact devices with high channel density, but are also characterized by lower power consumption in respect to their discrete-type equivalents.

VLSI (Very-Large-Scale Integrated) CSPs are generally very compact, with a channel pitch comparable to the one of the detector's segmentation and can be operated in vacuum due to their naturally low power consumption. Unfortunately scaled technologies have a very low voltage tolerance if compared with traditional discrete-type circuits. If the latter are powered with ± 12 V or ± 24 V power rails, it is not uncommon to find chips that cannot tolerate a power supply higher than 1-1.5 V. This results into a natural reduction of the dynamic energy range of integrated CSPs. For this and other design reasons, of which the description escapes from the purpose of this paper, it is common to design front-end analogue circuits in technologies with channel length not shorter than 180 – 350 nm, that can generally tolerate between 3.3 V and 5 V.

Besides the choice of a technology that complies with the dynamic range requirements (without forgetting the much more important ones related to electronic noise), some circuit solutions to overcome the natural limits of the dynamic range are mandatory.

In this work an integrated analogue circuit that implements a Time-Over-Threshold (ToT) algorithm is presented. This device can overcome the output voltage swing limits of an integrated CSP, extending its dynamic energy range one order of magnitude above its natural saturation level.

2. Circuit description

The main feature of the device described in this work is its ability to swiftly recover a charge-sensitive preamplifier in case of saturation, producing at the same time an analogue signal that contains the information about the charge released by the detector. This technique, called “fast-reset”, is based on the charge conservation principle and is well described in literature [5-9].

Generally when the detector releases a big charge signal (for example due to the impact of a heavy charged particle) and the CSP saturates, the output signal is distorted and the energy information is lost. Such saturation, considering the typical components' values used in the context of γ or particle spectroscopy, may last up to some milliseconds. During this dead-time the preamplifier is blind and all the incoming signals are lost.

The “fast-reset” circuit consists of a low-noise charge-sensitive preamplifier, a comparator configured as Schmitt trigger and a current generator. When the preamplifier is under the saturation threshold the comparator is in a logic “low” state and keeps the current generator disconnected from the input node of the preamplifier. The CSP thus produces at the output the conventional “exponential decay” signals that can be sampled with an ADC or sent to an analogue spectroscopy amplifier. In case of saturation, the Schmitt trigger connects the current generator to the input node of the preamplifier, restoring the CSP’s operating point. In this way, the dead-time is reduced from some milliseconds to just some microseconds.

The dead-time reduction is however only one aspect of the proposed circuit. Implementing a precisely tuned and constant current generator, the energy information can be retrieved measuring the time required to perform the reset cycle. Nevertheless, this technique suffers from the following issue: the fast-reset procedure collects and measures all the charge present on the input node of the CSP at the moment of saturation. This may include not only the charge released during the event that caused saturation, but also some residual charge from previous events.

In this work, an auxiliary structure that extends the conventional “fast-reset” device is presented. Its purpose is to produce, in case of saturation, an analogue signal with amplitude proportional to the charge released by the detector. This amplitude doesn’t depend on the residual charge on the input node, thanks to a baseline correction algorithm implemented in analogue form. The conceptual schematic of such device is depicted in Fig. 1.

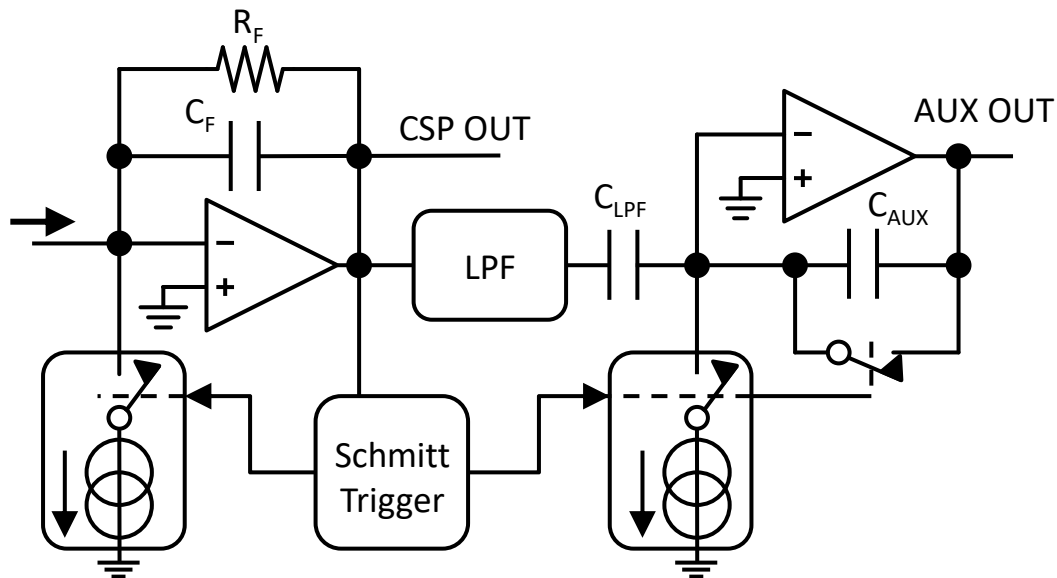


Figure 1. Schematic diagram of the integrated charge-sensitive preamplifier with fast-reset device and Time-To-Amplitude converter. The baseline correction algorithm is implemented in an analogue circuit.

The working principle of this auxiliary structure is the following. During the “fast-reset” cycle, the comparator activates, besides the current generator that acts on the CSP, a second current generator equal to the first one. In this way, the auxiliary structure integrates a current equal to the one collected from the input node of the preamplifier. Even so, this current is not the only one integrated by the second operational amplifier: there is also a contribute from the capacitance C_{LPF} driven by the Low-Pass Filter (LPF) block. The low-pass filter acts as an analogue memory that samples the output voltage of the preamplifier before the event that caused saturation. This voltage (V_0) contains the information about the residual charge on the input node before the event of interest. In fact, if such residual charge is equal to q_0 , the CSP output voltage before the event of interest is equal to $V_0 = -q_0/C_F$, where C_F is the CSP’s feedback capacitor. During the reset cycle the low-pass filter output voltage runs from the value V_0 (CSP output voltage before the reset event) to the value V_1 (CSP output voltage at the end of the reset event). The voltage of the auxiliary signal at the end of the reset process is equal to:

$$V_{AUX}(t_1) = \frac{1}{C_{AUX}} \cdot [I_{RESET} \cdot T - C_{LPF} \cdot (V_1 - V_0)]$$

Considering that C_{LPF} has the same value of C_F and that the voltage V_1 is an arbitrary constant that for the purposes of this paper can be considered equal to 0, the previous equation turns into the following:

$$V_{AUX}(t_1) = \frac{1}{C_{AUX}} \cdot [I_{RESET} \cdot T - C_F \cdot \left(-\frac{q_0}{C_F}\right)] = \frac{1}{C_{AUX}} \cdot [I_{RESET} \cdot T + q_0].$$

At the end of the reset process the voltage of the auxiliary structure is thus proportional to the total charge collected by the current generator minus the one already present on the input node before the event. In practice this voltage is proportional to the charge released by the detector during the event that caused saturation and doesn’t depend on the baseline voltage of the preamplifier.

This technique allows for amplitude spectroscopy even if the preamplifier is in deep saturation condition. The auxiliary signal can be sent directly to an ADC and doesn’t require additional filtering. The spectrum obtained with this technique, once properly calibrated, should be joined with the conventional under-threshold one to produce the complete spectrum. An ASIC preamplifier implementing this technique was designed in AMS 350 nm technology (see Fig. 2), realized and tested. The preliminary experimental results are reported in the next section.

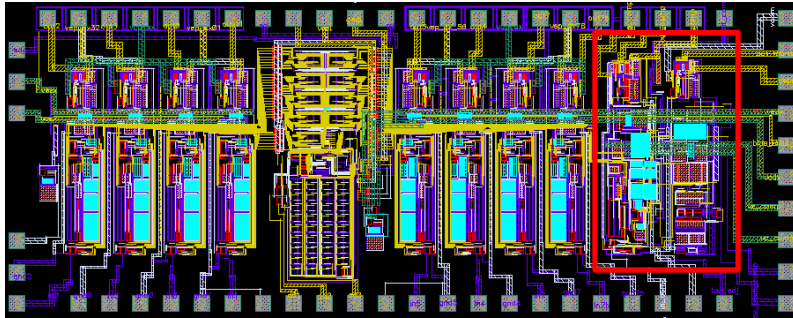


Figure 2. Layout of the chip designed in AMS 350 nm technology. The channel equipped with the innovative auxiliary structure described in this work is the one on the right (red rectangle). This channel is specifically designed for cathodic signals, while the other eight channels are designed to perform the readout of the anodic segments of a silicon pad detector. The area of the full chip is approximately 9 mm².

3. Experimental results

The chip was packaged in a PLCC88 carrier and mounted on a custom-designed PCB. The detector was simulated with a pulser connected to the input node of the preamplifier through a test capacitor of 1 pF. The reset threshold of the CSP is slightly under 40 MeV in silicon, that are roughly equivalent to 2 pC. Charge pulses from 2 pC to 10 pC were injected in the CSP with the pulser. The output waveforms of the CSP and signals produced by the auxiliary device were acquired with a 5 Gs/s, 500 MHz digital oscilloscope (see Fig. 3).

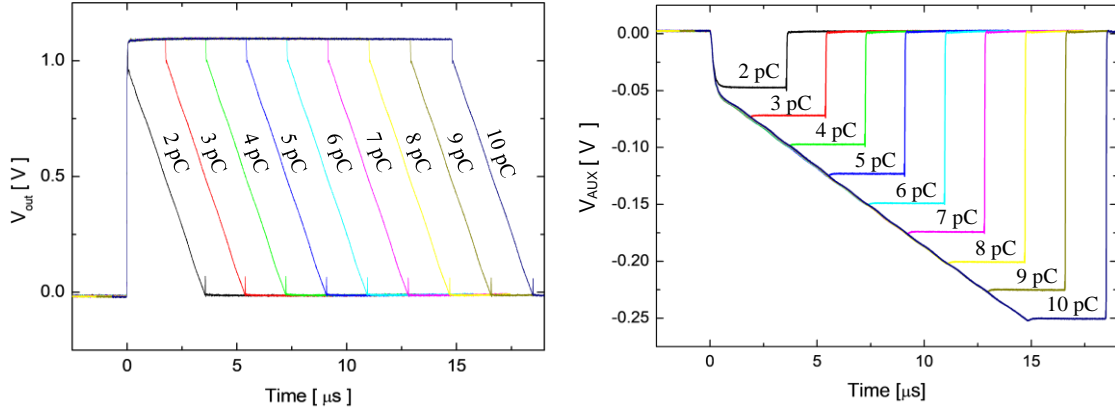


Figure 3. On the left: output signals coming from the charge-sensitive preamplifier after injection of test charge pulses from 2 pC to 10 pC. These charge pulses trigger the reset cycle. The shape of the output signals is similar to a rectangular trapezoid due to the effects of saturation and the constant current draw of the reset. On the right: analogue signals produced by the auxiliary TAC structure during the fast-reset events pictured in the figure on the left.

For each of the nine values of charge pulses between 2 pC and 10 pC, 100 signals from the auxiliary TAC device were acquired. The height of the signals was evaluated with a simple algorithm that performs an average over the signal flat-top. The nine spectrum peaks were analyzed giving the following results. The peak corresponding to 2 pC has the worst relative resolution (0.43% FWHM). The best-case relative resolution is equal to 0.13% FWHM, achievable from 7 pC onwards. The dynamic range of the auxiliary TAC device is determined by the power rails and the value of C_{TAC} . In this ASIC a C_{TAC} value of 20 pF and an available voltage swing of 2 V guarantee a dynamic energy range of 800 MeV. The baseline rejection capability of this circuit ensures that the amplitude of TAC signals produced by 3 pC test pulses is affected by a baseline fluctuation between 0 pC and 1 pC only by 0.6% of its total amplitude.

4. Conclusions

The preliminary results shown in this paper demonstrate the effectiveness of the proposed method. The relative resolutions obtained are suitable for high resolution particle spectrometry with silicon detectors. This technique is intended to be used only for large signals that induce the saturation of the CSP. A low-noise CSP is required in order to ensure a good resolution of the under-threshold part of the spectrum. For reference, please consider that the preamplifier integrated in the ASIC under study has a resolution of 1.1 keV FWHM with 1 pF of feedback

capacitance and 4 pF of detector capacitance. Further analysis of the circuit must be performed in order to fully characterize the device.

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