Characterization of an Associative Memory Chip in 28 nm CMOS Technology

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***Abstract*—This paper presents the characterization of the new Associative Memory chip (version 7) designed and fabricated in 28 nm CMOS. The design aims at: enhancing links from/to FPGAs; increasing bandwidth thanks to full custom LVDS transceivers; and reducing power consumption and silicon area by means of new memory cells designed with full-custom approach. The design was submitted in December 2016; the prototypes were fabricated and packaged in a 17 × 17 Ball Grid Array (BGA) standalone package. Prototype characterization confirms the chip functionality. The final chip will be assembled in a System In Package (SiP) together with a bare FPGA die.**

I. Introduction

A common challenge in the last decades is the fast and accurate handling of big data. Specific cases of study are the High Energy Physics (HEP) experiments, which require innovative devices to accurately reconstruct the particle tracks. The Fast TracKer (FTK) is a dedicated electronics system being integrated in the ATLAS experiment [1] at the Large Hadron Collider (LHC) [2] at CERN, for real-time reconstruction of the tracks of particles produced in the proton-proton collisions [3]. The FTK system strongly enhances the capability of the online event selection system of the ATLAS experiment, thus allowing the full exploitation of the physics capability of the LHC. The core of the system for the current FTK and of the future Hardware Tracker for the Trigger (HTT) [4] is a dedicated VLSI processor: the Associative Memory (AM) chip that provides highly parallelized and fast pattern recognition. After several prototypes designed, fabricated, and tested, in 2015 the first production chip was released: the AM06 chip [5], manufactured in $65\,\mathrm{nm}$ CMOS technology.

In the next years, centre-of-mass energy and intensity of the proton-proton collisions of the LHC will be significantly enhanced. Therefore, the new HTT system will dramatically change in size, power consumption and protocols. To simplify the commissioning at CERN, the new system will be based on Advanced Telecommunications Computing Architecture (ATCA) crates and will contain less boards, equipped with more complex AM chips with respect to the previous FTK system. This requires a new generation of AM chips, with higher processing capability, lower power consumption, and higher memory density. We estimate that the new AM chips have to be denser by a factor of 3 with respect to the previous version (AM06). To comply with memory density requirements, the new chip is designed in an advanced $28\,\mathrm{nm}$ CMOS technology.

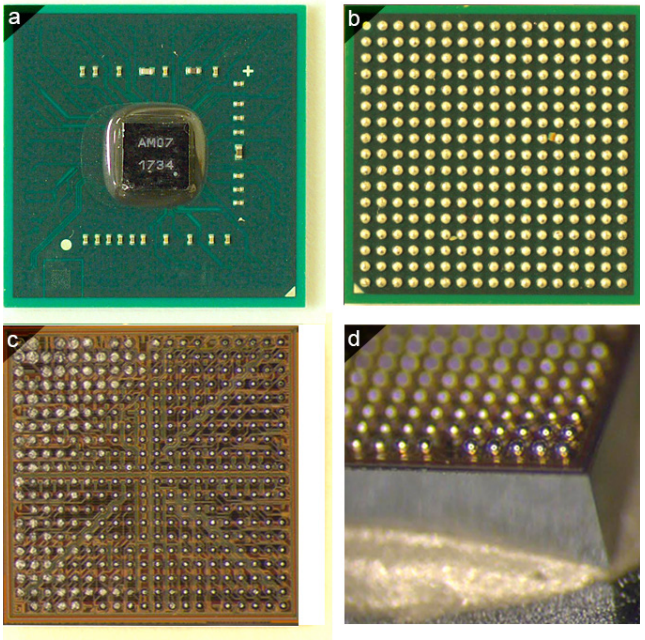

Fig. 1. Photograph of AM07: (a) flipped die mounted on the BGA package; (b) balls of the bottom of the BGA package; (c) bumps on the top of the die; (d) detail of bumps at a corner of the die.

Moreover, an interesting feature of the chip presented in the paper is the capability to be compatible with the elaboration of data for other disciplines: AM07 will be used as a component to develop an integrated system for pattern recognition, dedicated to image and DNA sequence analysis. The aim of AM07 is to demonstrate the functionality of two innovative memory cell designs [6] at the clock frequency of 200 MHz, in order to pioneer the design of future AMs for the ATLAS and CMS experiments at the LHC, and other DNA and image analysis applications.

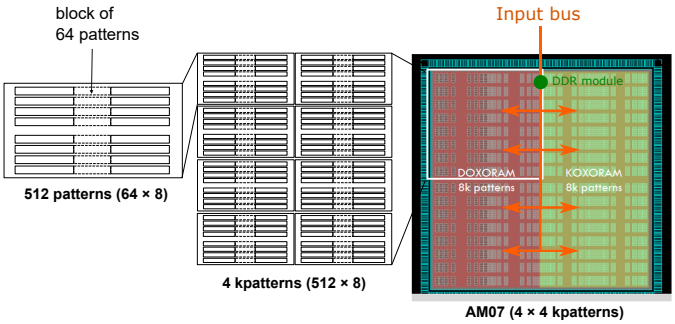

Fig. 2. Arrangement of the 16 kpatterns cell array.

II. Architecture

The AM07 die is flipped and mounted on a dedicated substrate that interconnects the signal and power nets. Fig. 1(a) shows the top view of the assembled chip, mounted on the substrate together with decoupling capacitors, to improve the power distribution network. The AM07 package counts 17 × 17 balls for PCB interconnections (Fig. 1(b)). The chip has 20 × 20 bumps for interconnections with the substrate, as shown in Figs. 1(c) and (d). The design size is $1.520\,\mu\text{m} \times 1.520\,\mu\text{m}$. At fabrication stage, the chip size is shrunken by a linear factor of 90%.

The AM07 is organized in arrays of associative memory cells integrating two innovative full-custom designs, called DOXORAM and KOXORAM [6], either based on the previous XORAM cell [7].

Fig. 2 shows the hierarchy of the memory banks: each word of data is composed by 18 bits, a pattern contains 8 words, and a bank of 16 × 1024 patterns is organized in four blocks (two DOXORAM blocks and two KOXORAM blocks), each containing 4 × 1024 patterns.

The array of 64-word blocks is organized in 64 rows × 18 bits. As depicted in Fig. 3, the Bit-Lines (BL) and the Search-Lines (SL) are 18 bit double buses which distribute the input data over the columns of the memory array.

A. Comparison mode

SLs are used to find a match of input data with pre-stored data. When an exact match is found in a block of 18 cells (a word), the associated Set-Reset latch (SR) is flagged to '1', and the match pattern in a row is stored in a segment of eight flip-flops (8FF). For each pattern of 8 words, the Quorum logic counts the number of FFs flagged to '1'. If the count exceeds a programmable threshold, the address of the row and the position of matching words within the pattern are read out. All these operations are performed in parallel.

B. Write mode

BLs are used to write input data into the memory cells. In the 'write mode', one of the patterns is activated by a Write-Line (WL) through a demultiplexer.

TABLE I
Propagated buses and working modes

STATE	propagated bus	mode
'00'	—	stand-by
'01'	BLs	write
'10'	SLs	comparison
'11'	BLs and SLs	write/comparison

C. Input data propagation

The input data are fed in parallel to each block via the Double Data Rate (DDR) module as shown in right side of Fig. 2. The propagation od input data can be controlled by means of an external signal (STATE), as shown in Table I. The input data propagation could be also disabled in the DDR module.

The AM07 chip can operate in the DDR data transfer mode. When the DDR mode is turned on, the input buses are sampled at both edges of the input clock.

D. Clock domains and signal registering

Two external clocks are used: CLKI, to synchronize the input buses, and CLKO, to synchronize the output buses. The full-custom memory arrays are clock-less and they are the interface between CLKI and CLKO, as shown in Fig. 4.

All input, control and output signals are registered by means of Delay Flip Flops (DFFs) at the I/O interface.

To reduce the VDD current peaks, one half of the input data are propagated among the chip on the positive edge of the CLKI, and one half on the negative edge.

III. Design flow and simulations

A mixed design approach has been used: the memory arrays and analog blocks are designed with full-custom approach; the more complex (in terms of logic) modules are designed with Electronic Design Automation (EDA) tools.

Analog simulations with corner analysis have been performed to validate the full-custom blocks. Cadence Tempus software has been used for Static Timing Analysis (STA), Universal Verification Methodology (UVM) and ncsim for back-annotation in digital simulations, and Cadence Voltus for IR drop analysis.

A. Static timing analysis and IR drop analysis

Simulations with Tempus have been performed in three worst cases: (1) slow-slow library models, 0 °C, core supply: 0.9 V, working frequency: 150 MHz; (2) fast-fast library models, 0 °C, core supply: 1.1 V, working frequency: 300 MHz; (3) typical library models, 27 °C and 85 °C, core supply: 1 V, working frequency: 300 MHz.

Fig. 5 shows the histograms of setup slack times. For all cases and simulations, results confirm that no negative slack time exists.

Voltus simulator has been used to analyze the IR drop on the power wires. Standard cells containing Decoupling CAPacitors (DCAP) have been placed to reduce the IR drop. The estimated internal capacitance is 23 nF. Fig. 7 shows a

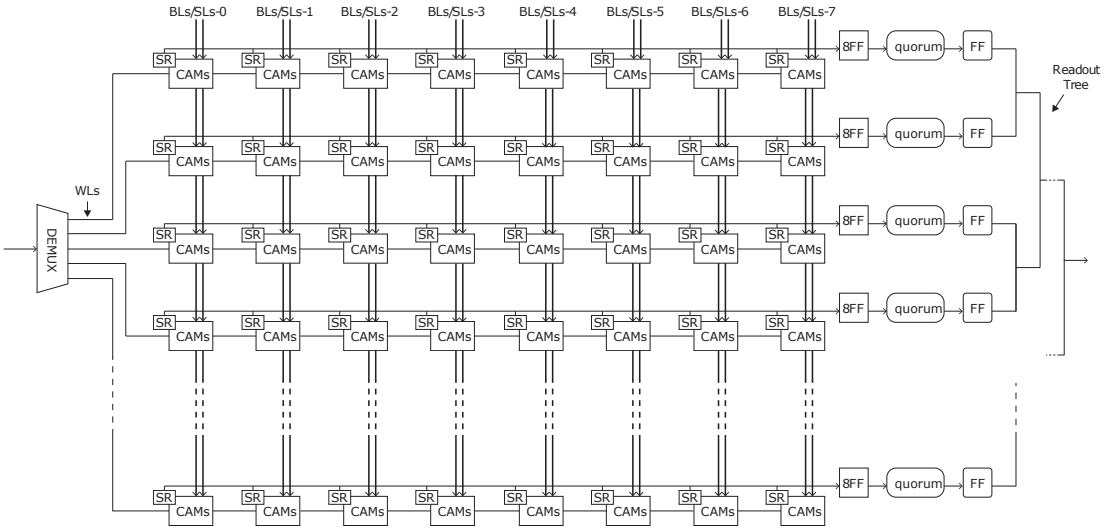

Fig. 3. Functional diagram of the 64-pattern-block.

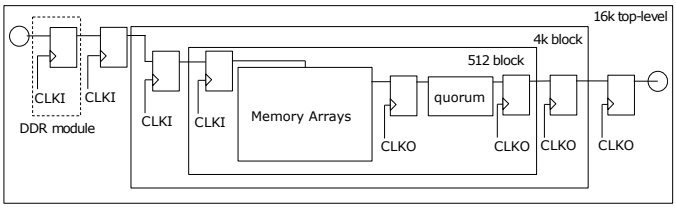

Fig. 4. Schematic diagram of the AM07 clock domains.

color map of the IR drop over the whole AM07 layout. The maximum value of the IR drop is $64\,\mathrm{mV}$.

IV. Characterization Results

The chip has been characterized in three sites (CERN, Milano, and Paris) by means of a dedicated PCB (EDA-03625) employing two Enclustra Mercury KX1, a low-jitter clock Generator (Si5380), a ZIF connector for the AM07, two Ethernet connectors, a JTAG connector and some SMA connectors for fast lanes. Fig. 6 shows the signal flow diagram. Fig. 8 shows the photograph of the characterization setup.

The chip is fully functional and can operate correctly up to 200 MHz. LVDS drivers and receivers have been measured with good results up to 1.1 Gbit/s. Power dissipation (TX+RX) is about 8 mW at 1 Gbit/s. The Built-In Self-Test (BIST) has been performed with different voltage supply conditions (Tab. II).

To measure the power consumption, the chip has been characterized in different conditions. Leakage current has been measured without clock signals in the idle state. Results are: 1.21 mA in Milano, and 4.1 mA in Paris. The current consumption due to the clock propagation from the external pin to the interface of every core (not propagating inside the memory banks) has been measured with clock signal, in idle state, and with all the cores disabled. Results are summarized in Table III, which reports the current consumption versus

TABLE II
SHMOO PLOT SHOWING THE WORKING FREQUENCY LIMIT IN MEGAHERTZ

I/O supply [V] \ Core supply [V]	0.65	0.75	0.85	0.95	1.00	1.05	1.10
2.0	fail	fail	105	184	245	245	245
1.9	fail	fail	105	184	245	245	245
1.8	fail	fail	105	184	245	245	245
1.7	fail	fail	105	184	245	245	245
1.6	fail	fail	105	184	245	245	245
1.5	fail	fail	105	184	245	245	245
1.4	fail	fail	105	184	245	245	245

TABLE III
CURRENT CONSUMPTION DUE TO THE CLOCK PROPAGATION FROM THE EXTERNAL PIN TO THE INTERFACE OF EVERY CORE

Frequency [MHz]	Current consumption [A] Paris	Milano
35.11	$5.89 \cdot 10^{-3}$	$2.63 \cdot 10^{-3}$
105.32	$1.08 \cdot 10^{-2}$	$7.90 \cdot 10^{-3}$
147.46	$1.40 \cdot 10^{-2}$	$1.08 \cdot 10^{-2}$
184.32	$1.68 \cdot 10^{-2}$	$1.40 \cdot 10^{-2}$
245.76	$2.08 \cdot 10^{-2}$	$1.80 \cdot 10^{-2}$

frequency. Further, the current consumption due to the whole propagation of clock signals has been measured by enabling the cores. The measured total current consumption is: 106 mA (in Milano) and 110 mA (in Paris). Finally, we measured KOXORAM and DOXORAM power consumption. Results at 184.32 MHz are as expected in the simulations: DOXORAM consumes 0.832 fJ/bit versus 0.91 fJ/bit in simulation, KOXORAM consumes 0.684 fJ/bit versus 0.69 fJ/bit in simulation. It is clear that we have a good agreement between measurements and simulation results ($\pm$ 10%).

V. Conclusion

The AM07 is a new Associative Memory chip designed in the $28\,\mathrm{nm}$ technology. Simulation and characterization results

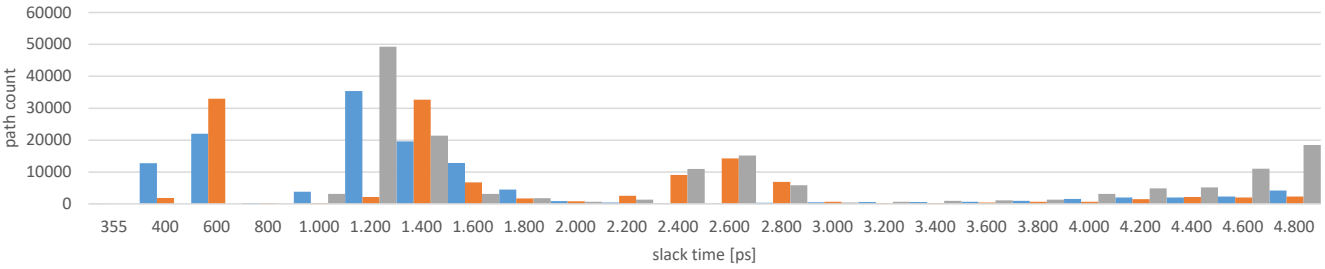

Fig. 5. Histograms of slack time obtained with STA: (blue) SS, 0 °C, 0.9 V; (orange) SS, 150 °C, 0.9 V; (grey) TYP, 25 °C, 1.0 V;

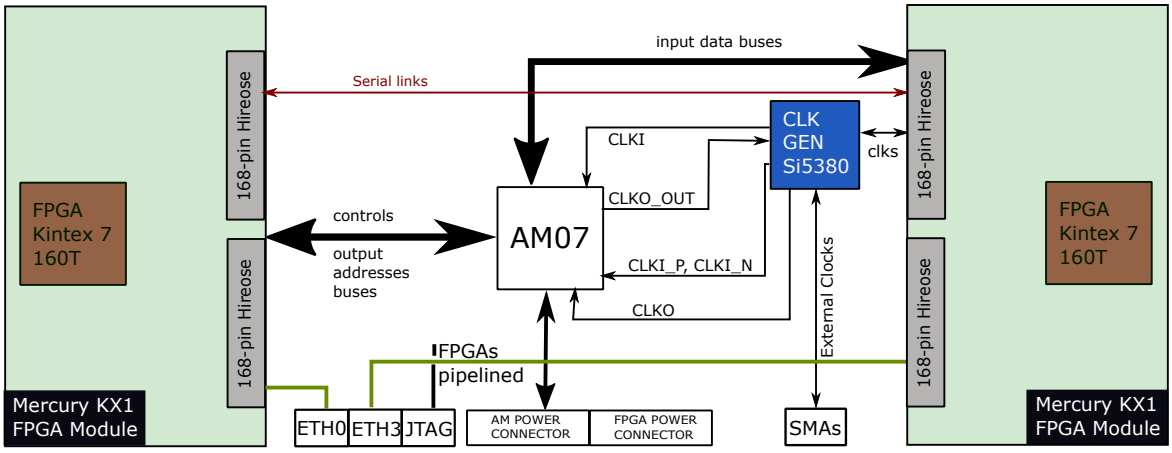

Fig. 6. Block diagram of characterization setup.

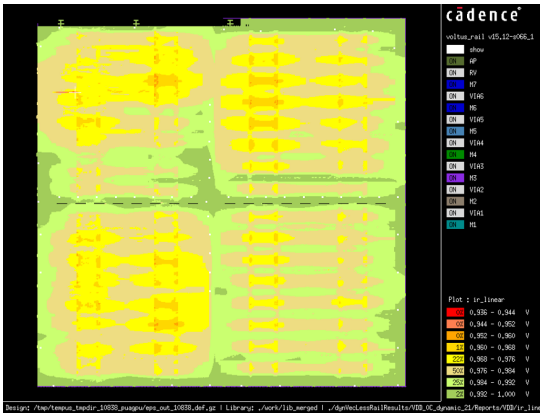

Fig. 7. Color map of IR drop over the AM07 layout; orange areas indicate larger IR drop.

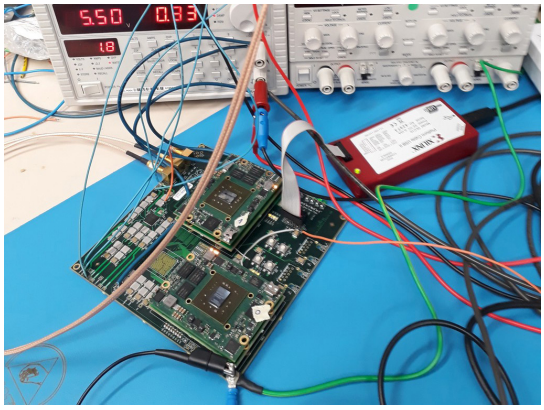

Fig. 8. Photograph of the characterization setup at CERN.

demonstrate that the chip is fully functional at 200 MHz. Compared to the AM06 chip, the AM07 exhibits a power consumption reduced by a factor of 1.7 and a density increased by a factor of 2.9. In the AM07 design, we have noticed that the automatically designed logic circuitry does not scale as predicted by the Moore's law. For this reason, in the future we plan to re-design the Quorum circuit with a full-custom approach, to reduce the overall area. With this approach, we aim to improve also the power consumption and the maximum operating frequency of the next chip.

Acknowledgments

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