A New XOR-Based Content Addressable Memory Architecture

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Abstract—In this paper we describe a Content Addressable Memory (CAM) architecture based on a new custom cell, called XORAM. The cell is composed by two main blocks: a 6T-SRAM, and a 4T-XOR logic gate. Each XORAM cell compares the input data on the bit line with the data stored in the 6T-SRAM cell. The output matching bit is obtained by performing a NOR operation between all bits of the XORAM cells storing the word. The proposed architecture is based on a fully-CMOS combinational logic, and it does not require any precharge operation or control and timing logic. A compact full-custom layout has been designed for a memory organized in 18-bit words, to reduce both area and power consumption. Compared with a conventional selective precharge match-line technique, the proposed circuit occupies less area. Simulation results demonstrate that power consumption is reduced by a factor of 8.

I. INTRODUCTION

A Content Addressable Memory (CAM) compares input data with stored data and returns the address of the matching data [1]. CAMs are useful for a large number of applications, like Look Up Tables (LUT) of Ethernet routers, computer assisted tomography, and for processor cache memories.

Our application is related to the enhancement of the trigger performance in the ATLAS experiment at CERN [2]. Input data coming from silicon detectors must be spatially correlated to find particle trajectories. This job can be done using a large array of CAMs to recognize particle tracks. To this purpose, we need a CAM array with 18-bit input data buses. The CAM should provide a list of particle trajectory addresses at its output. In a previous work, a CAM has been designed, based on selective precharge and current race scheme. This solution has been devised to reduce current consumption and to save power [3].

In this work, we present a new architecture of a “single word” (i.e., a block of 18 bit cells) which is made of two parts: (1) an XOR-SRAM (XORAM) block, and (2) an 18-input NOR gate. The first part is a new cell, called XORAM, which is composed by a 6-transistor SRAM (6T-SRAM) cell, and a 4-transistor XOR gate (4T-XOR). The SRAM internal nodes and the search Bit Line (BL) are connected to the 4T-XOR pass transistors to reduce the number of transistors. The XORAM cell can both store data, like a standard SRAM cell, and compare stored data with input data. The operation is controlled by a Write Line (WL) signal: when WL is high, store operation is enabled and the output is disabled; on the other hand, when WL has a low logic value, the comparison is enabled and the result is transferred to the output.

The comparison performed by the cells is a bit-wise operation. Since our target is to compare a 18-bit input data bus with 18 bits stored in the SRAM, we must generate a single-bit output signal which describes if the matching of the entire bus occurred. To this purpose, we use an 18-input NOR gate. The proposed solution is compared in area and in power consumption with the previous architecture based on selective precharge.

II. CONVENTIONAL CAM CELLS

Figs. 1 and 2 illustrate two single-bit CAM cells based on NAND architecture and NOR architecture, respectively [1]. The NAND and NOR cells are the most often used CAM

![Fig. 1. Schematic diagram of a NAND single-bit CAM cell.](image1)

![Fig. 2. Schematic diagram of a NOR single-bit CAM cell.](image2)
cells. However, other cells could be employed; a review CAM cells with different characteristics is presented in [4].

In order to obtain the match result for an \( n \)-bit word, \( n \) CAM cells must be employed. NAND- and NOR-based cells can be connected as shown in Figs. 3 and 4, respectively [1].

Both the NAND- and NOR-based \( n \)-bit word CAMs require a precharge phase (\( \text{pre} \)), to drive the match line at a high logic level through a PMOS transistor. Then, during the evaluation phase (\( \text{eval} \)), the match line is discharged when the \( n \)-bit word matching does not occur, either through an NMOS transistor driven by the evaluation signal (\( \text{eval} \)) in the NAND-based CAM in Fig. 3, or through one of the NOR cells in the NAND-based CAM in Fig. 4.

It is worth pointing out that the precharge is a current-consuming operation, since only one (or none at all) of the stored words will match the input pattern.

To reduce the power consumption, NAND- and NOR-based CAM cells can be combined together. An example is shown in Fig. 5, where the word comparison is done by means of a current source, 4 NAND CAM cells, 14 NOR CAM cells, and a set-reset flip-flop [3]. The current source charges the match line with a constant current value only if the data stored inside the cells match with the input data on the bit lines. On the contrary, if at least one of the NAND cells does not match the input data, it disconnects the match-line, thus preventing the output node to be charged. If a NOR cell does not match, a path from the match line to ground is activated, and consequently, the match line is discharged. In terms of node voltages, if all the cells match the data input, the match line is charged up to a high logic value; on the contrary, if at least one of cells does not match, the match line is not charged and the voltage is about 0 V.

III. THE NEW XORAM CELL

To overcome the problems mentioned above, a new CAM cell has been designed, based on the XOR Boolean function, instead of the NAND and NOR functions. Although a CAM cell based on the XOR (XNOR) Boolean function was proposed in 1985 [5], its use never become widespread. In the original paper by Kadota et al., the CAM cell implements the XNOR function, employing 4 NMOS pass transistors.

A better design can be achieved employing complementary pass transistors to realize the XOR function. The new solution aims at a suitable trade-off between the number of transistors, the robustness of the architecture, and a reduced power consumption. The new cell, called XORAM, consists of a 6T
Fig. 5. Schematic of the NAND-NOR-based 18-bit word CAM.

SRAM cell merged with a 6T-XOR gate. Since the SRAM cell provides both the bit (A) and the inverted bit (A), the XOR gate can be made using only 4 MOS transistors, thus obtaining the schematic diagram shown in Fig. 6. The single bit cell output (OUT) is equal to zero when the stored bit (A) matches the bit-line (BL), and is equal to one when they are different.

Fig. 7 shows the layout of the XORAM cell, designed in a 65 nm CMOS technology.

IV. THE 18-BIT WORD CAM

As said before, the output (O) of the 18-bit CAM must have a high logic value when all input bits match the stored data, and a low logic value if at least one bit does not match. This operation can be performed by a simple 18-input NOR logic gate, made of three stages: (1) six 3-input NOR cells, (2) two 3-input NAND cells, and (3) one 3-input NOR cell, as shown in Fig. 8.

To avoid spurious glitches at the output during write operation, the write signal (WL) is used as an additional input to the last stage of the 18-input NOR gate.
V. Simulation Results

The layout of an 18-bit CAM has been designed and simulated after parasitic extraction. Simulation results confirm that write and compare operations can be done up to a frequency of 1 GHz. However, the printed circuit board designed for the track recognition system works at a frequency which cannot exceed 100 MHz. For this reason, simulations were performed with a 100 MHz clock frequency. Fig. 9 shows the simulation result of the 18-bit CAM over 64 clock periods in typical mean (TM) conditions: the pattern stored during clock cycle 0 is recognized during the eighth clock cycle, when the output bit (in the third plot) goes high.

Table I summarizes the results of corner analysis, showing the output delay, the average current and the peak value of the current drawn from the $V_{DD}$ supply. Simulations were performed using transistors parameters for worst speed (WS), worst power (WP), worst one (WO) and worst zero (WZ) conditions, using the appropriate extreme values for the temperature $T$ and the voltage supply $V_{DD}$, as shown in the table.

In typical conditions, the average current required by the 18-bit XORAM-based CAM is 0.7 µA during read operation (at 100 MHz). The largest current consumption occurs with worst power MOS parameters, when the average current is 1.3 µA.

Compared to the previous NAND-NOR-based architecture requiring an average current of 6 µA, the proposed scheme achieves a current reduction by a factor of 8 in typical case.

VI. Conclusion

This paper has presented a XOR-based CAM cell, which requires a simple fully-CMOS combinational logic to decode the word matching. By avoiding precharge phase and current race schemes, the proposed circuit can be operated at frequencies up to 1 GHz, and its current consumption is lower than the consumption of a NAND-NOR-based CAM. For these reasons, the proposed XORAM cell is a good candidate for the design of a large CAM array.

**Table I**

Simulation Results at 100 MHz: Delay Time, Average Current and Peak Current in Different Conditions

| $T$ (℃) | $V_{DD}$ (V) | $t_{clk,match}$ (ps) | avg(|$i_{DD}$|) (nA) | peak(|$i_{DD}$|) (µA) |
|---------|--------------|-----------------------|----------------------|------------------------|
| TM      | 27 1.20      | 928                   | 707.6                | 637.3                  |
| WS      | 15 1.08      | 1741                  | 650.1                | 340.1                  |
| WS      | −50 1.32     | 928                   | 768.8                | 744.9                  |
| WP      | 15 1.08      | 909                   | 1310.0               | 604.5                  |
| WP      | −50 1.32     | 576                   | 836.0                | 1163.0                 |
| WO      | 15 1.08      | 1177                  | 743.3                | 259.6                  |
| WO      | −50 1.32     | 687                   | 788.0                | 901.7                  |
| WZ      | 15 1.08      | 1358                  | 851.3                | 429.6                  |
| WZ      | −50 1.32     | 760                   | 779.0                | 903.0                  |

References


