Impact of Package Parasitics on Crosstalk in Mixed-Signal ICs

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ABSTRACT

This paper presents an approach for the analysis and the experimental evaluation of crosstalk effects due to current pulses drawn from voltage supplies in mixed analog-digital CMOS integrated circuits. A realistic model of bonding and package parasitics has been derived to study digital switching noise injected through bonding interconnections. Simulations results indicate that disturbances due to switching currents in digital blocks propagate through the substrate and affect analog voltages, thus degrading circuit performance. Test structures have been integrated into a test chip mounted with different technologies, in order to compare the measurements on test chips. Measurements confirm simulation results. Chip-on-board mounting technology has better performance with respect to chip-in-package, due to the reduction of parasitic elements.

Keywords: digital switching noise, mixed analog-digital ICs, crosstalk

1. INTRODUCTION

Mixed analog-digital integrated circuits are affected by digital switching noise, which can be a limiting factor for overall system performance.[1] It is well known that noise propagation through the substrate and the interconnections interfere with the analog section of the circuit, limiting the accuracy of analog operations.[2] Thus, it is necessary to study crosstalk mechanisms in order to understand the propagation path towards analog blocks, and to design suitable protection structures.

First of all, a realistic model of interconnection parasitics must be adopted for simulations. Package effects cannot be neglected in an accurate mixed-signal IC design. Indeed, parameters associated to the package severely affect the stability of bias voltages; in particular, bondwire and pin parasitic resistance, inductance and capacitance form an *RLC* network which can cause the internal supply voltages to be significantly different from external voltages. Moreover, mutual inductance and cross-capacitance between bondwires cause electromagnetic coupling between digital and analog supplies. Therefore, the advantage of kelvin ground for substrate bias vanishes, as disturbances due to digital switching currents propagate through mutual inductances and cross-capacitances.

From these considerations, it is apparent that an accurate analysis of a mixed-signal circuit must account for parasitics. To this end, we have derived a realistic model in which, for each pin, we considered parasitic coupling with the nearest four wires on both sides. This results in a SPICE subcircuit used to perform time-domain simulations.

Then, a fast but accurate analysis of current consumption during logic transitions is required, to evaluate the noise due to the switching activity of digital cells.[3] Digital simulation tools are mostly optimized for simulation

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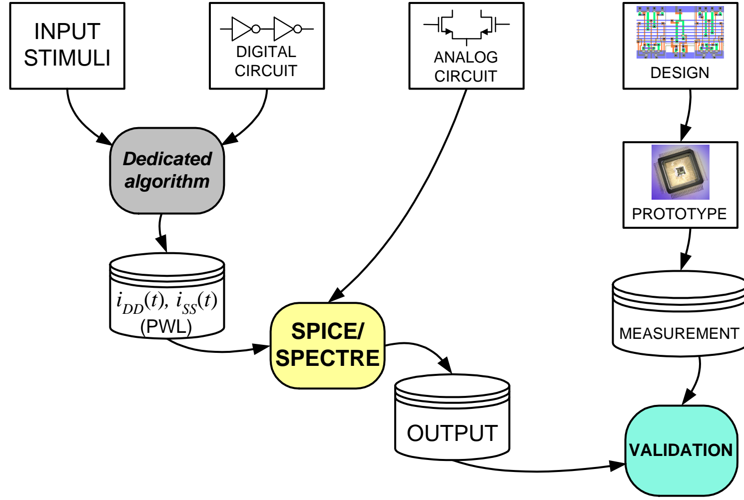


Figure 1. Flow diagram of the proposed approach.

speed and for "average" power consumption. On the other hand, analog circuit-level simulators (e.g. SPICE or SPECTRE) are quite inefficient for the analysis of large digital circuits. Therefore, for mixed analog-digital circuits, to speed up simulation time, we propose a method based on the separate analysis of the digital and the analog section, as illustrated in Fig. 1. We have developed a dedicated simulation algorithm in C++, to analyze current waveforms in digital circuits by using time-continuous functions, instead of sample sequences, to represent signals. The algorithm saves a piece-wise linear (PWL) description of current waveforms, that can be used as an input for subsequent circuit-level simulation of the analog section of a mixed-signal circuit.[4]

Simulation results demonstrate that parasitics can severely degrade mixed-signal IC performance. To validate the simulation results obtained with our method, we have simulated and designed a test chip, described in Sect. 2. The test chip has been fabricated and mounted both into a JLCC24 package and by using chip-on-board technology.

Simulation results and experimental measurements on chip samples are presented in Sects. 3 and 4, respectively.

2. TEST CHIP DESCRIPTION

To investigate crosstalk effects, a test chip has been designed in a 0.13 μm CMOS technology with high-resistivity p-type substrate, twin wells, and n-isolation layer that can be used for shielding purposes. Fig. 2 shows a vertical section of MOS devices with and without the n-isolation layer.

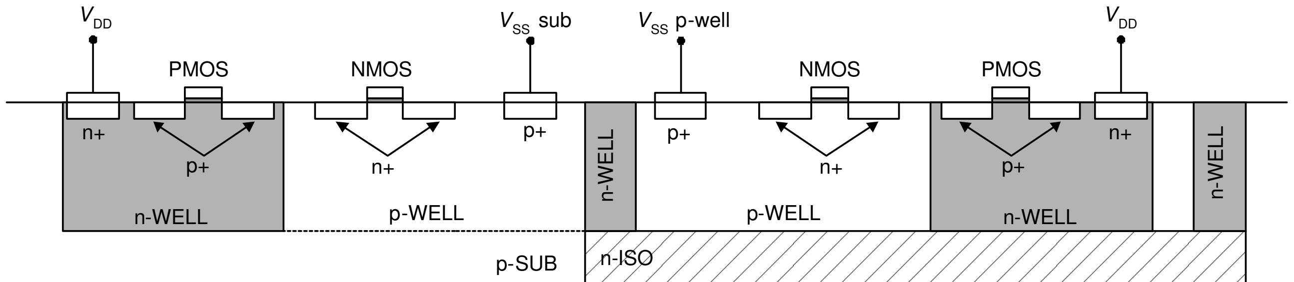


Figure 2. Section view of NMOS and PMOS devices in the used technology.

Local p-wells are isolated from the global p-substrate by the n-isolation layer (buried n-iso contacted with lateral n-wells), as shown in the rightmost side of Fig. 2. The isolated p-well is contacted to a ground node (V_{SS} p-well) different from the substrate (V_{SS} sub).

As shown in the leftmost side of Fig. 2, p-wells designed outside the n-isolation layer are connected each other through the common substrate.

The designed test chip includes digital noise injecting blocks integrated together with analog noise collecting structures.

Fig. 3 illustrates a schematic diagram of digital structures. The noise injecting structures are a ring oscillator with a frequency externally controlled by using a proper bias current I_{REF}, and a tapered inverter chain driven by an external clock. The ring oscillator works at low frequencies (about 1 MHz) to allows the noise injection spikes to be correctly distinguished. Both structures drive a capacitance $C_{\mathrm{inj}} = 5$ pF, which behaves as a large clock net in a synchronous digital circuit.

Fig. 4 shows the analog structures used for noise collection. They are four open-drain MOS transistors, with an external gate bias voltage. The MOS transistor drain is connected to a supply voltage (V_{DD} or ground) through an external resistance R_{EXT}, to properly bias the transistor. Two complementary MOS transistors (A

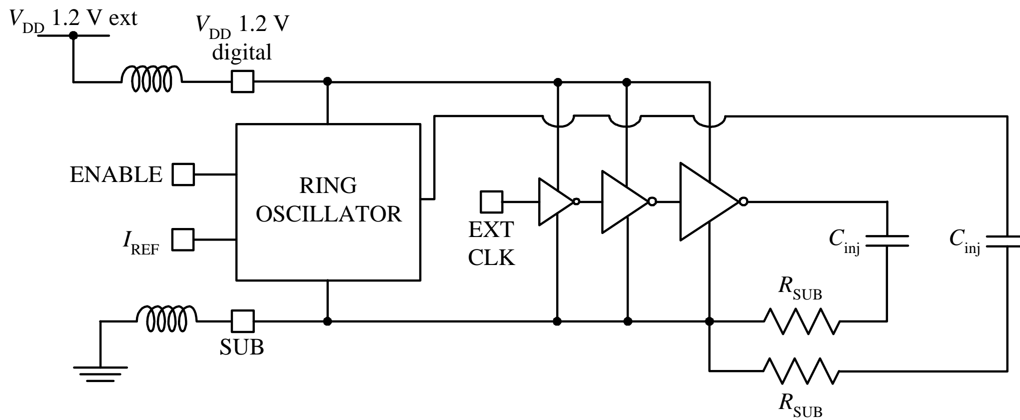


Figure 3. Schematic diagram of the digital injector structures of the test chip.

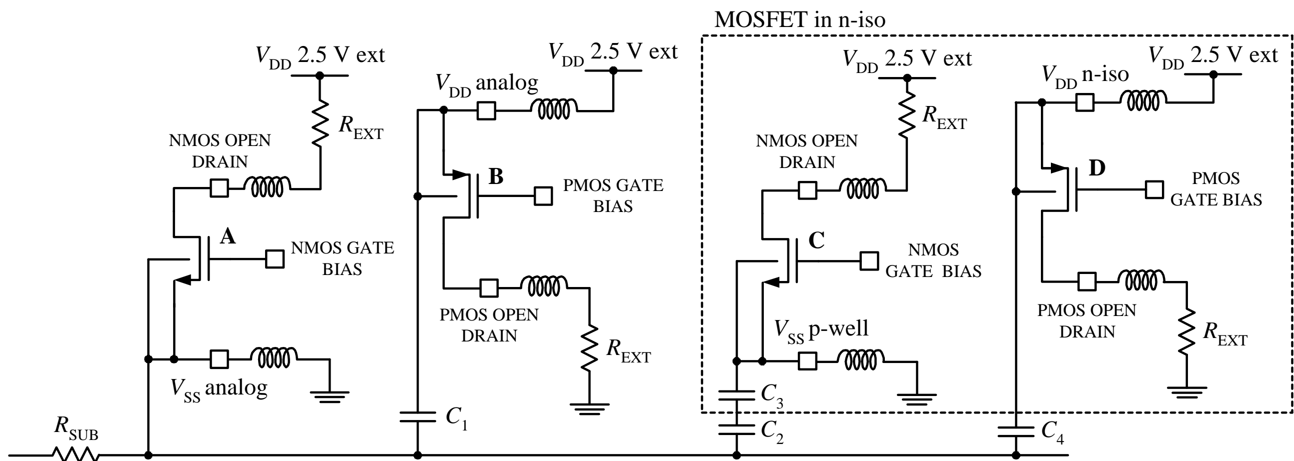


Figure 4. Schematic diagram of the analog noise collector structures of the test chip.

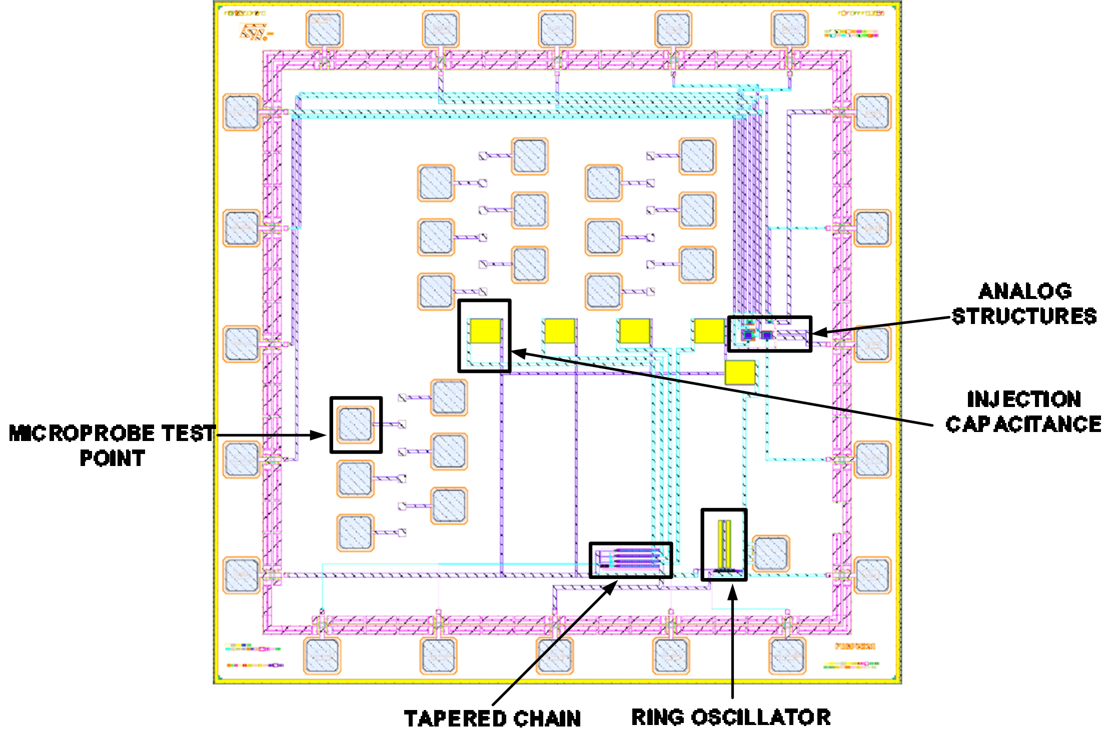


Figure 5. Layout of the test chip.

and B) are placed over the chip global substrate, while the other two transistors (C and D) are in local wells within the n-isolation layer. Fig. 4 shows also the most important parasitic elements, which contribute to digital switching noise propagation: series inductances (L), capacitances between substrate and wells (C_1, C_2, C_3, and C_4), and substrate resistance (R_{sub}).

Fig. 5 shows the layout of the test chip.

3. ANALYSIS AND SIMULATION RESULTS

To evaluate effects of bonding and package parasitic elements, a suitable model has been developed. Fig. 6 illustrates a simplified model of bonding and package parasitics for two adjacent wires.[5] The instantaneous current i_{DD} due to the digital switching of logic gates produces a voltage drop, which affects the on-chip digital supply V_{DD}, and propagates to the adjacent wires through both capacitive coupling, due to the capacitance C between wires, and inductive coupling, due to the mutual inductance represented by K. Therefore, the analog on-chip voltage $v(t)$ is no more equal to the external voltage v_{s}, but turns out to be a function of the voltage v_{s} and of the digital switching current i_{DD} and its derivative:

$$v(t) = f\left(v_{\text{s}}, i_{\text{DD}}, \frac{di_{\text{DD}}}{dt}\right) . \tag{1}$$

Values of parasitic elements (extracted for a ceramic JLCC24 package with 20 bondwires) are: inductance $L = 1$ nH, resistance $R = 50$ mΩ, ground capacitance $C_{\text{GND}} = 5$ fF, capacitance between wires $C = 30$ fF, mutual inductance coupling factor $K = 0.2$.

Current drawn by digital blocks produces a voltage drop across off-chip interconnect parasitics, which affects the chip substrate. As a consequence, the substrate bias voltage is not kept at a constant value and displays the

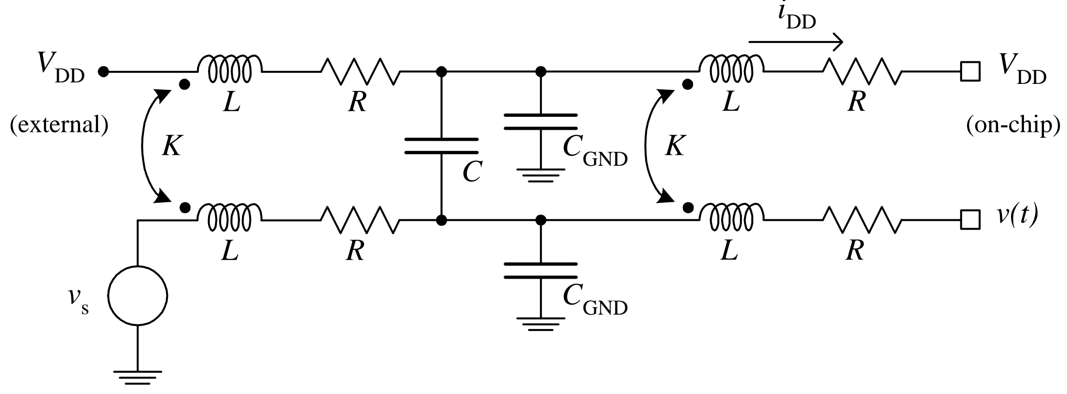


Figure 6. Equivalent circuit for digital switching noise.

"ground bounce" effect, as shown in the plot of Fig. 7, which was obtained by simulating the circuit when the inverter chain is working.

To evaluate the effect of the ground bounce on the output of an MOS transistor,[5] we consider the drain current in the saturation region, given by:

$$i_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \tag{2}$$

with obvious meaning of symbols. A variation in the source-to-substrate voltage v_{SB} causes a variation in the transistor threshold voltage, since

$$V_{th} = V_{t0} + \gamma\left(\sqrt{v_{SB} + \phi_0} - \sqrt{\phi_0}\right) \tag{3}$$

where V_{t0} is the threshold voltage for $v_{SB} = 0$, γ is the 'body effect' coefficient (typically, $\gamma \approx 0.5\ \mathrm{V}^{1/2}$), and ϕ_0

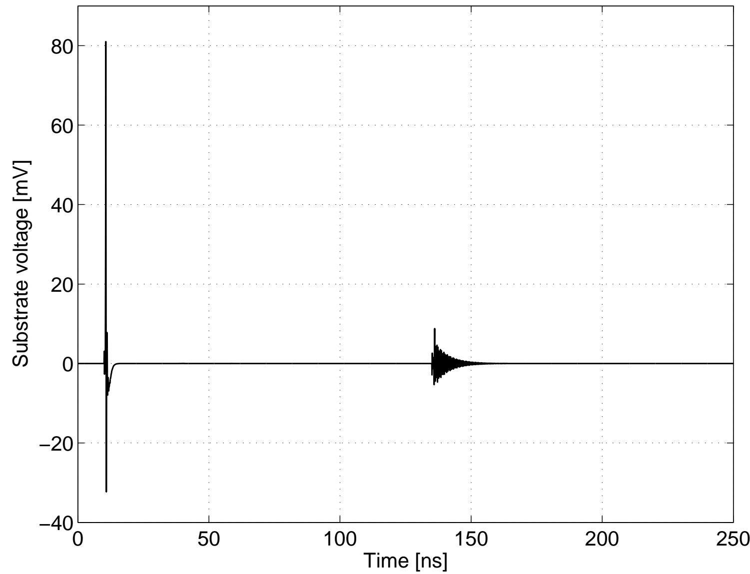


Figure 7. Substrate voltage affected by ground bounce due to digital current and bondwire parasitics (simulation).

is the 'surface potential' (typically, $\phi_0 \approx 0.6$ V).[6] The drop voltage across the resistor $R_{\rm EXT}$ is:

$$v_{\rm EXT} = -R_{\rm EXT} i_{\rm D} = -R_{\rm EXT} \frac{1}{2} \mu C_{\rm ox} \frac{W}{L} \cdot \left(V_{\rm GS} - V_{\rm t0} + \gamma \left(\sqrt{v_{\rm SB} + \phi_0} - \sqrt{\phi_0} \right) \right)^2 \tag{4}$$

If the substrate noise has a small amplitude, from small signal analysis we obtain:

$$v_{\rm ext} = -R_{\rm EXT} i_{\rm d} = -R_{\rm EXT} \cdot g_{\rm mb} v_{\rm sb} \tag{5}$$

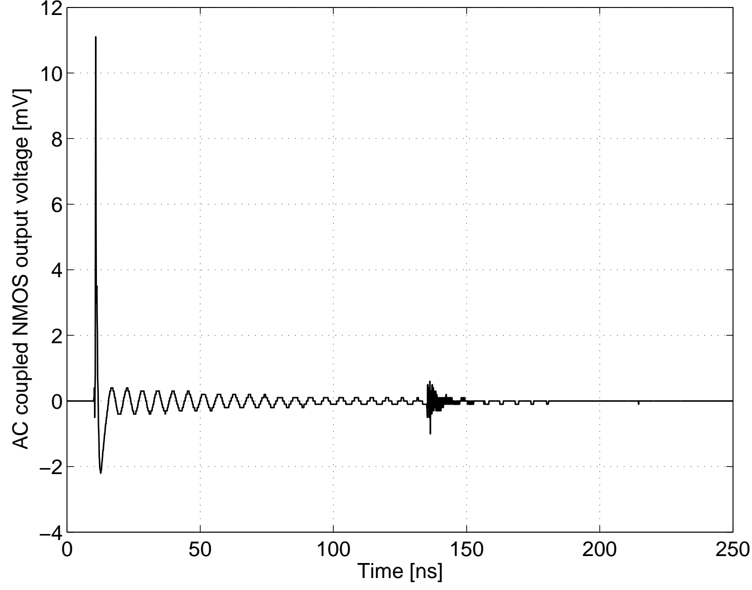


Figure 8. Simulated output voltage of the NMOS transistor, with bondwire parasitics.

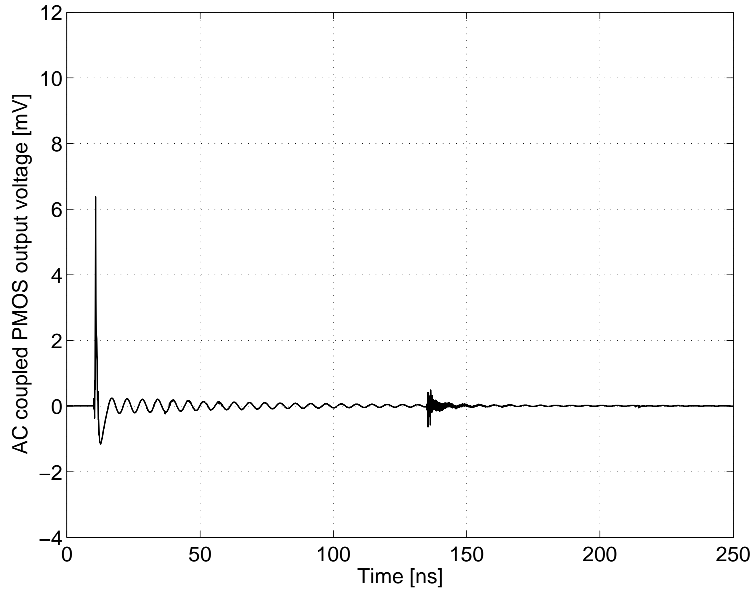


Figure 9. Simulated output voltage of the PMOS transistor, with bondwire parasitics.

In this equation, v_{ext}, i_{d} and v_{sb} are the small signal components of v_{EXT}, i_{D} and v_{SB}, respectively, and g_{mb} is the bulk transconductance, given by

$$g_{\mathrm{mb}} = \gamma \cdot g_{\mathrm{m}} / (2\sqrt{V_{\mathrm{SB}} + \phi_0}) \tag{6}$$

where V_{SB} is the quiescent source-to-substrate voltage.

The MOS transistors have a conductance parameter $K = 1.1$ mA/V^2, and they are biased with a drain current $I_{\mathrm{D}} = 1$ mA. From these figures, we obtain a small signal transconductance $g_{\mathrm{m}} = 2\sqrt{KI_{\mathrm{D}}} = 2.1$ mA/V, and a bulk transconductance $g_{\mathrm{mb}} = 0.3g_{\mathrm{m}} = 0.63$ mA/V.

Figs. 8 and 9 show the simulated output voltages for MOS transistor labeled with A (NMOS device) and B (PMOS device) in Fig. 4, respectively. The output voltages are affected by disturbances with a peak value of 11 mV for the NMOS device, and 6 mV for the PMOS device. From (5), we can note that the ground bounce affects the local substrate of the NMOS device more than the local substrate of the PMOS device. This is due to the shielding effect of the n-well around the PMOS device.

4. MEASUREMENT RESULTS

The fabricated test chip has been mounted into a JLCC24 package, as shown in Fig. 10. The length of bonding wires is 1 mm, which leads to a parasitic inductance of about 1 nH.

The test chip has been assembled also by using the chip-on-board technique. The length of off-chip interconnections is similar to the chip-in-package, thus leading to similar values for parasitic inductances due to bondwires and board; the chip-on-board assembly technique avoids additional parasitic elements due to the package.

Tests chips, assembled as described above, were fed with a 4-MHz clock signal provided through an external clock generator (shown in Fig. 11), driving the tapered inverter chain in Fig. 3. The output voltages at the drain node of MOS transistors were captured through a digitizing oscilloscope working with 2 GS/s of equivalent sampling rate.

Figs. 12, 13, 14 and 15 show the time-domain switching noise at the transistor outputs. In particular, Figs. 12 and 13 show the output voltages of NMOS transistors outside and inside the n-isolation layer, respectively, while Figs. 14 and 15 show the output voltages of PMOS transistors outside and inside the n-isolation layer, respectively.

Measured results are in agreement with simulated values. We observe that the output noise is lower for NMOS devices, as expected.

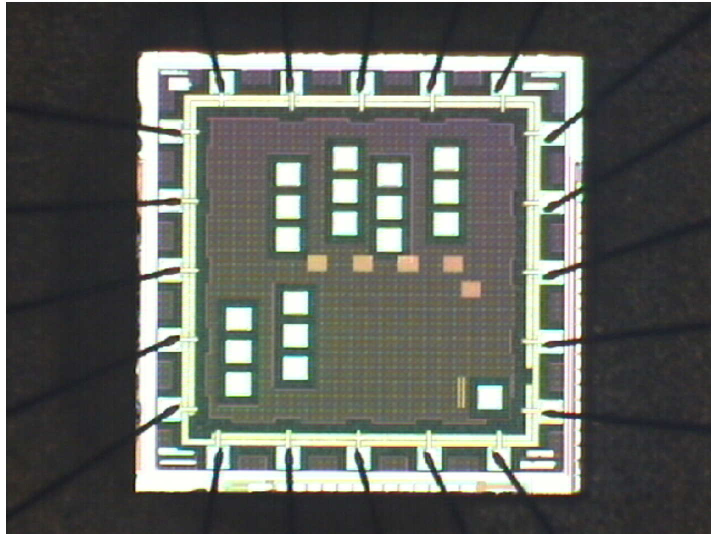


Figure 10. Microphotograph of the test chip.

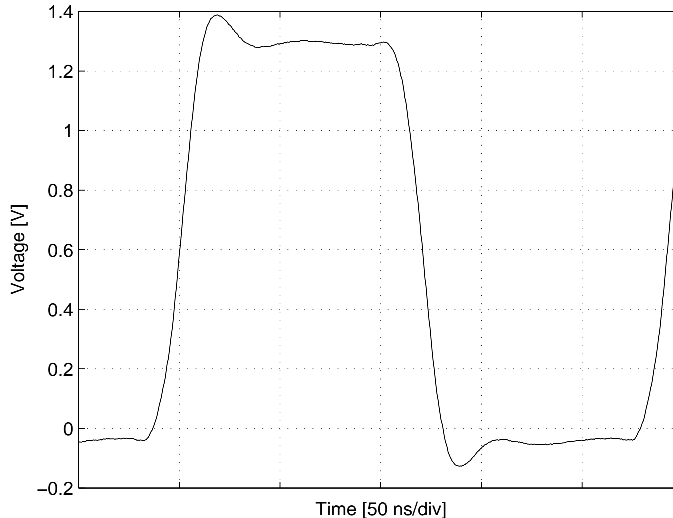


Figure 11. External clock applied to the tapered inverter chain.

Table 1 summarizes the the measured noise values (peak-to-peak and rms) for both test chips.

By comparing the above figures, we can note that the n-isolation layer improves crosstalk immunity of NMOS devices. On the other hand, PMOS transistors do not benefit by the insertion of the n-isolation layer. Indeed, PMOS devices are shielded by the n-well, as shown in Fig. 2: for this reason, the additional n-isolation layer does not lead to remarkable improvements.

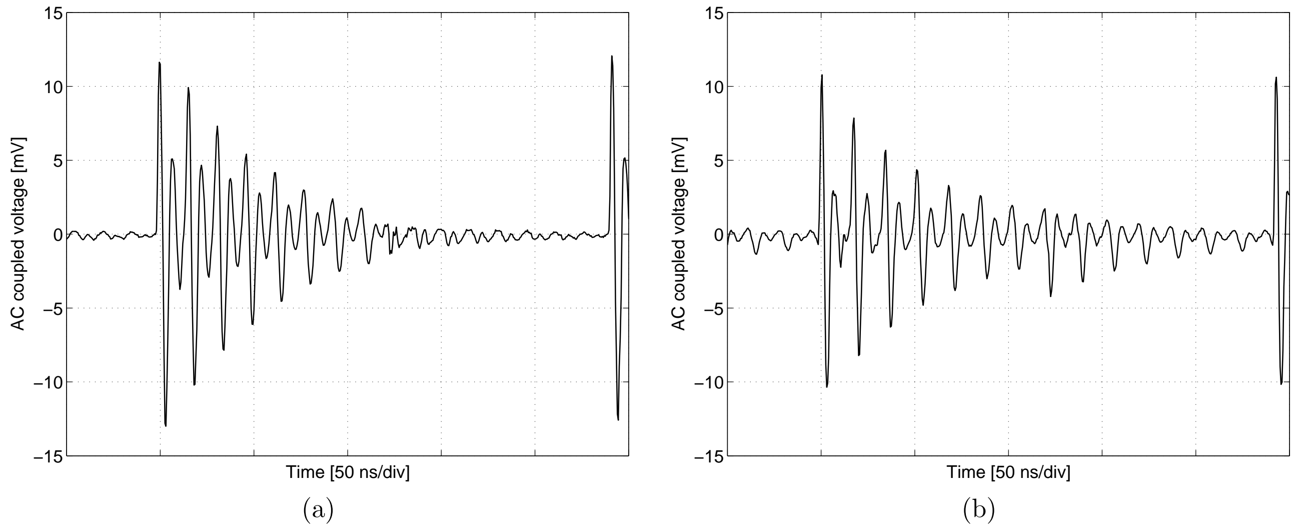
Moreover, the chip-on-board has a lower value of peak-to-peak noise voltage than the chip-in-package, thanks to the reduction of parasitic inductances.

5. CONCLUSION

This paper has discussed a simplified model for the analysis of the effects of digital switching noise on analog circuits. A CMOS test chip has been designed, fabricated, and mounted with different techniques to compare simulated with experimental results. A good agreement between simulated and measured data was demonstrated. Experimental evidence indicates that chip-on-board assembly technique has better performance than chip-in-package mounting, due to reduction of parasitics. Careful layout techniques can also help to reduce crosstalk effects. Results demonstrate that NMOS transistors in analog subcircuits can be effectively shielded with n-isolation layer, to reduce the amount of collected digital switching noise.

Table 1. Measured rms values of AC coupled disturbances at the transistors output.

	chip-in-package output noise voltage		chip-on-board output noise voltage	
layout configuration	peak-to-peak	rms	peak-to-peak	rms
NMOS outside n-iso layer	25.47 mV	2.284 mV	21.51 mV	1.870 mV
NMOS inside n-iso layer	19.26 mV	1.378 mV	18.40 mV	1.618 mV
PMOS outside n-iso layer	9.20 mV	0.641 mV	5.04 mV	0.405 mV
PMOS inside n-iso layer	10.01 mV	0.434 mV	7.12 mV	0.504 mV



(a) (b)

Figure 12. Output of the NMOS transistor outside n-isolation: (a) chip-in-package; (b) chip-on-board

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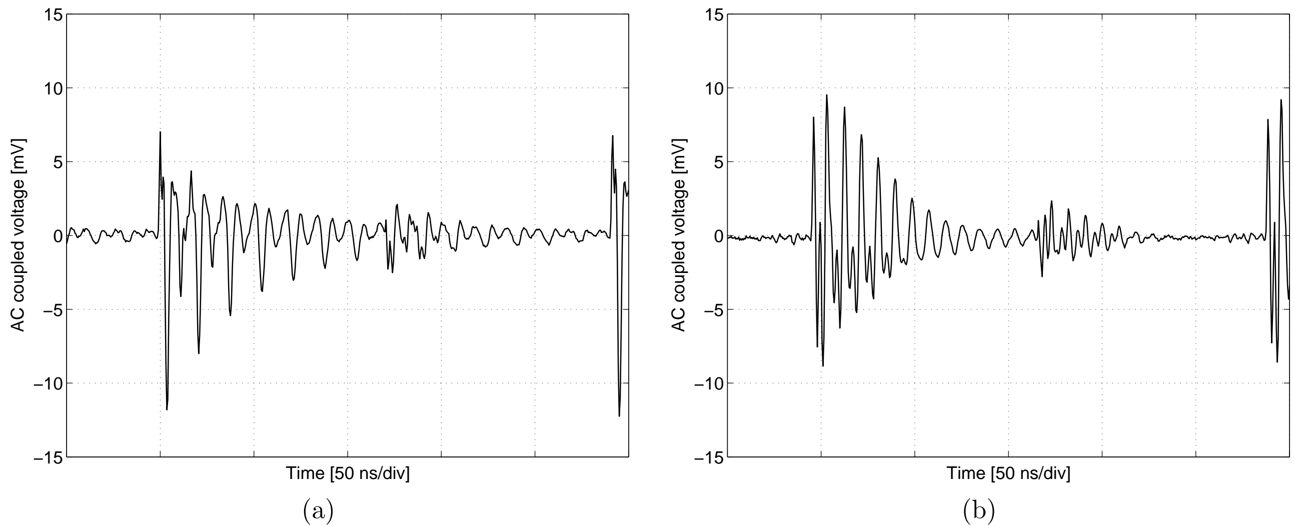

(a) (b)

Figure 13. Output of the NMOS transistor inside n-isolation: (a) chip-in-package; (b) chip-on-board.

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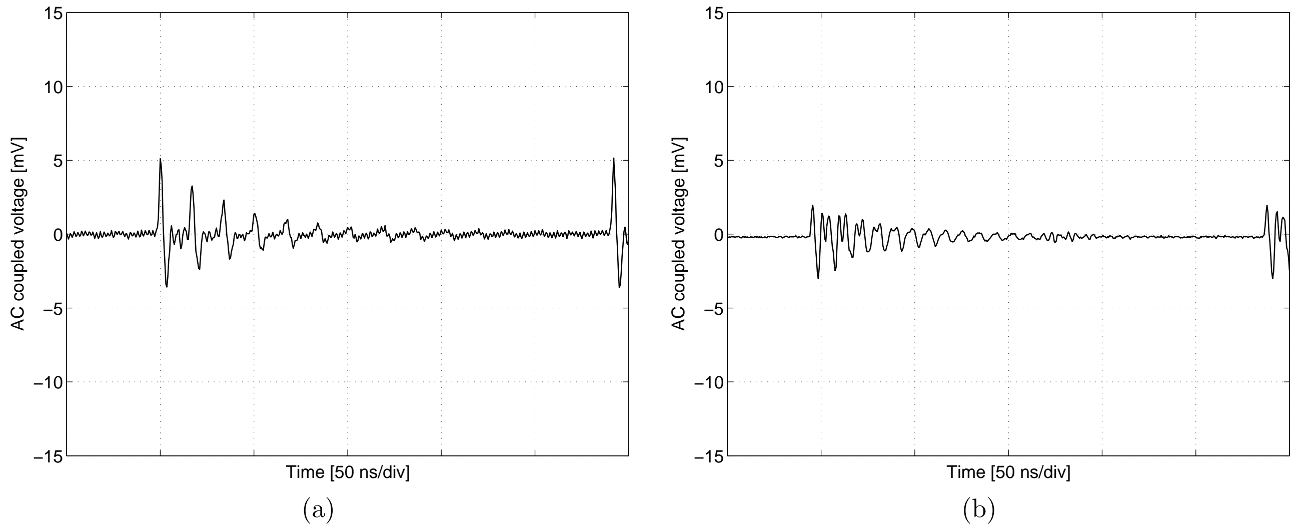

Figure 14. Output of the PMOS transistor outside n-isolation: (a) chip-in-package; (b) chip-on-board

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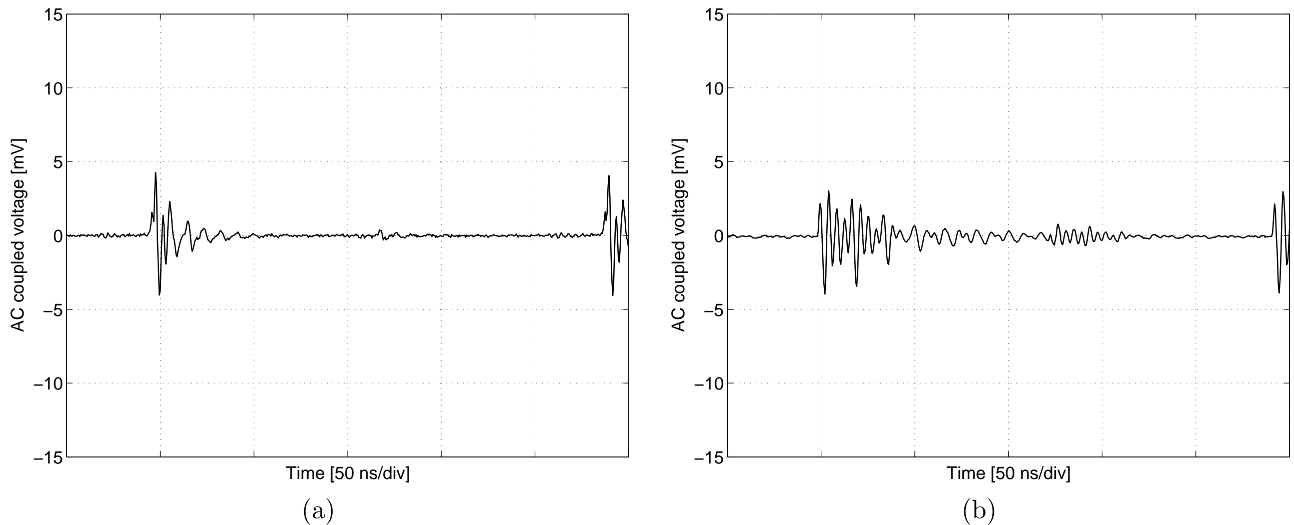

Figure 15. Output of the PMOS transistor inside n-isolation: (a) chip-in-package; (b) chip-on-board.

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