Model and verification of triple-well shielding on substrate noise in mixed-signal CMOS ICs

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Abstract

In this work, the effect of triple-well shielding in mixed-signal integrated circuits is studied. A test chip is presented that contains structures intended for investigation on substrate noise coupling. This paper shows a subset of the measurements that we carried out and attempts to give a rationale for them.

1. Introduction

In mixed-signal systems, noise from digital logic can severely limit performance of the analog section, which interfaces the digital processing core with the external world [1]. Coupling from switching digital nodes and power supplies to analog devices through the common substrate produces a variation in the threshold voltage of the MOS transistor biased in the active region. This effect must be carefully evaluated at early design stages, to allow the designer to select a robust architecture for the analog blocks. Suitable models have been presented for substrate noise analysis in submicron CMOS technology with epitaxial layer [2]. In this paper, the effect of a buried n-well is studied. Measurements on a test chip illustrate the effects of triple-well shielding on NMOS and PMOS devices, and design guidelines are derived from experimental evidence.

2. Test chip and board

We designed a test chip in triple-well CMOS technology in order to investigate the effects of substrate noise in mixed-signal integrated circuits. The chip contains digital blocks, aiming at noise generation, and analog blocks intended for noise collection. Both the analog and the digital part have been integrated twice: shielded by the triple well, and unshielded. This allows several combinations of shielding to be tested. The floorplan of the chip is shown in Fig. 1.

In this paper, we consider a noise-generating block made of a multi-layer capacitor whose bottom plate is tied to the substrate. It allows noise pulses to be injected into the substrate if, for example, a clock is fed to its top plate. This capacitor simulates noise injection from the clock, as in the case of a real digital circuit. The analog blocks are simple transistors in common-source configuration. They collect noise through both the body effect and the effect of parasitics.

In order to achieve better frequency responses and reduce the non-ideal effects introduced by a complex board layout, we decided to embrace a one-measurement-one-board philosophy.

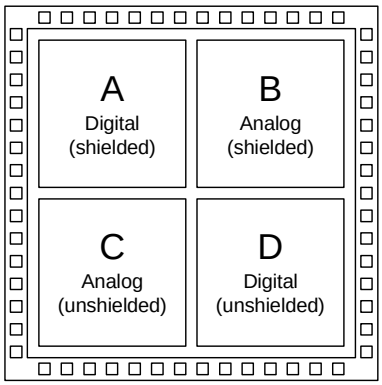

Fig. 1. Floorplan of the chip.

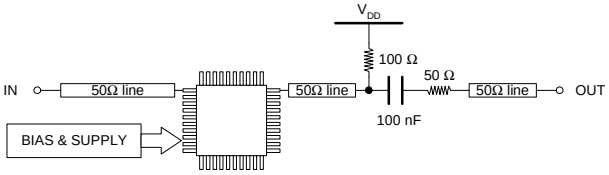

Fig. 2. Board diagram for the NMOS case.

Each board consists of four blocks (see Fig. 2):

1. the chip being measured;
2. some biasing circuitry plus the power supplies;
3. the input 50-Ω transmission line;
4. the output matched transmission line.

The input signal flows through a 50-Ω transmission line and is reflected back by the mismatched load (i.e., the 1-pF noise-injecting capacitor plus pin and bonding parasitics). In no way can the load be matched over a wide band (i.e., from dc to a few gigahertz). Therefore, the reflection coefficient Γ should be kept into account somehow.

As to the output, the signal path is perfectly matched in the frequency range of interest (i.e., from a few megahertz to a few gigahertz) because each transmission line sees a 50-Ω load at its end. The 100-Ω resistance, along with the bias voltage applied to the gate, sets the bias point and, hence, the gain of the noise-collecting transistor. A 6-dB loss (constant with frequency) exists due to the resistive divider constituted by the 50-Ω series

resistance and the 50-Ω matching load introduced by the equipment connected to the board.

3. Measurements

Fig. 3 plots measured peak-to-peak values of the collected noise versus input clock rise times. As expected, the peak-to-peak value decreases when the transition time of the clock is increased. Fig. 4 plots RMS noise values versus input clock rise times. This plot was calculated rather than directly measured.

Although Fig. 3 represents peak-to-peak values and Fig. 4 plots RMS data, there only exist a scaling factor between them, as long as the output noise pulses do not change their shape. The agreement between the two figures is good, which confirms the frequency measurements are accurate.

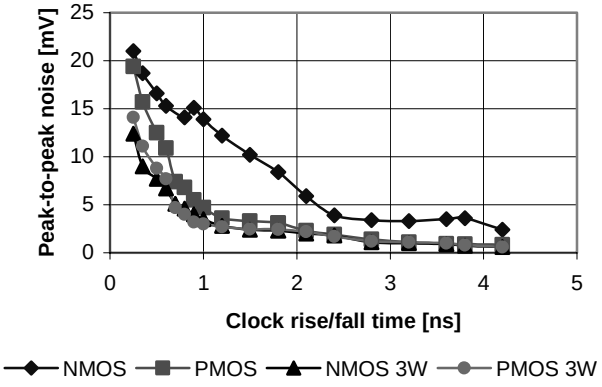

Fig. 3. Measured peak-to-peak noise versus input clock rise time.

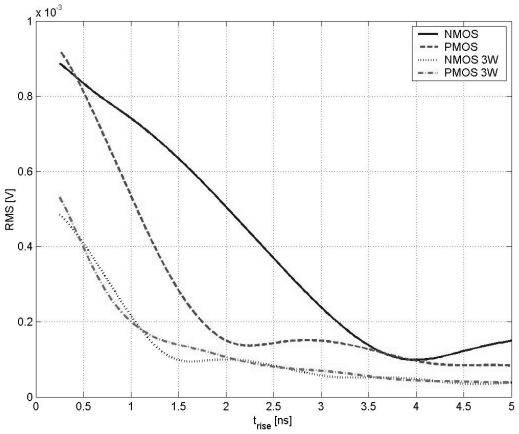

Fig. 4. Noise RMS values versus clock rise time (calculated from s_{21} data).

Fig. 5 and 6 show frequency domain measurements. As illustrated earlier, the boards do not introduce a significant amount of frequency distortion below 2 GHz. Therefore, up to that frequency the plots can be considered reliable enough.

4. Analysis and guidelines

To better understand the results, we will now analyze some simple models, to explain the above plots and to derive a few guidelines for the design.

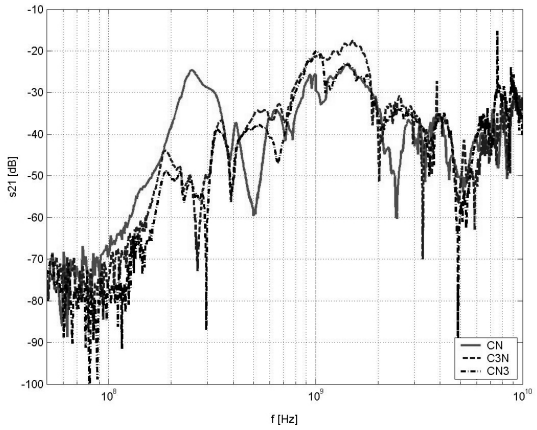

Fig. 5. Noise collection through an NMOS: unshielded (CN); shielded capacitor and unshielded NMOS (C3N); unshielded capacitor and shielded NMOS (CN3).

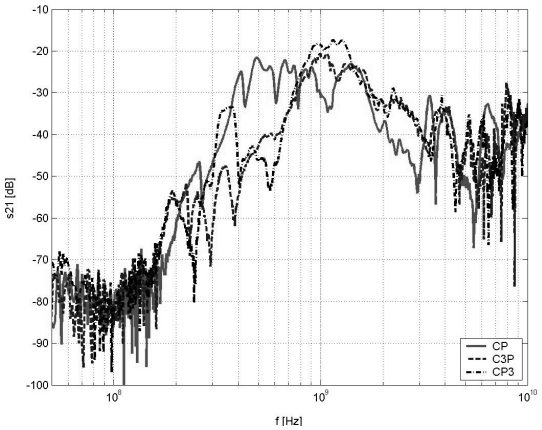

Fig. 6. Noise collection through a PMOS: unshielded (CP); shielded capacitor and unshielded PMOS (C3P); unshielded capacitor and shielded PMOS (CP3).

Noise coupling is a very complex phenomenon that requires distributed models in order to be fully described. However, in order to provide a clear rationale for what happens due to substrate noise coupling in integrated circuits, a few simplifications are of great help.

First of all, we must keep in mind that, with this kind of technology, the p+ substrate can be modeled as a single node. Due to the substrate biasing area spread all across the chip, it is as if there were a resistance (R_{pol}) between the substrate itself and ground. Fig. 7 represents the case of the unshielded noise injector. The lower plate of capacitor C is coupled to the substrate through a p+ substrate contact within a pwell. Beneath the pwell, which has a negligible resistance, the epitaxial layer (which has a resistance R_{epi}) connects the substrate contact area to the p+ substrate itself.

Similarly, on the collecting side, noise has to flow through another layer of epitaxial silicon (see, for example, Fig. 10, which will be commented in deep detail later). Since R_{pol} can be considered much lower then R_{epi}, injection and collection can be modeled separately. In other words, the Thévenin equivalent

generator for the noise injector has an output impedance lower than R_{pol} in modulus, while the equivalent input impedance of the collecting part is at least R_{epi}. This means the two parts can be considered, to a first approximation, as if decoupled, and the two models can be kept separated.

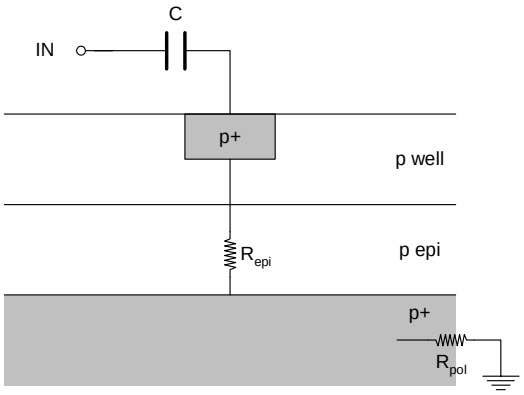

Fig. 7. Model valid in case of unshielded injection through the capacitor.

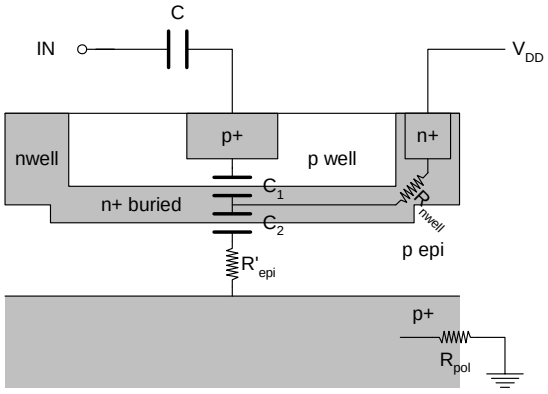

Fig. 8. Model valid in case of shielded injection through the capacitor.

Fig. 7 and Fig. 8 show two simple models for noise injection through a capacitor in the unshielded and the shielded case, respectively. The unshielded case is very straightforward. The shielded case is a little more complex. The two capacitances C_1 and C_2 model the two pn junctions at the top and the bottom side, respectively, of the n+ buried layer. The R_{nwell} resistance represents the path from the n+ buried layer to the power supply. The R'_{epi} resistance represents the resistance of the epitaxial layer, which in this case is slightly lower than in the unshielded case because the epi layer is thinner when an n+ buried layer is present. The shielded case is made of two cascaded CR networks, plus the final resistive divider composed of R'_{epi} and R_{pol}. Again, since R_{nwell} is much lower than R'_{epi}, the two CR networks can be considered decoupled.

For the unshielded case we may write:

$$\frac{V_{BULK}}{V_{IN}} = \frac{sC\left(R_{epi}+R_{pol}\right)}{1+sC\left(R_{epi}+R_{pol}\right)}\frac{R_{pol}}{R_{epi}+R_{pol}} \qquad (1)$$

For the shielded case, remembering the CR network decoupling hypothesis, we have:

$$\frac{V_{BULK}}{V_{IN}} = \frac{sC'R_{nwell}}{1+sC'R_{nwell}}\frac{sC_2\left(R'_{epi}+R_{pol}\right)}{1+sC_2\left(R'_{epi}+R_{pol}\right)}\frac{R_{pol}}{R'_{epi}+R_{pol}} \qquad (2)$$

where $C' = \frac{CC_1}{C+C_1}$ is lower than C.

Fig. 9 sketches the two frequency responses, obtained with the assumptions:

$$\begin{cases} \dfrac{R_{pol}}{R_{epi}+R_{pol}} < \dfrac{R_{pol}}{R'_{epi}+R_{pol}} \\ C'R_{nwell} < C\left(R_{epi}+R_{pol}\right) \end{cases} \qquad (3)$$

Nothing can be said in principle about the exact location of the remaining pole, as C_2 cannot be predicted without information about areas and doping values.

In any case, since the curve for the shielded case is a second-order one, there will always exist a frequency value below which the response to the shielded injection has a magnitude lower than the response to the unshielded injection. The exact location where the two responses intersect depends on the specific technological parameters and must be evaluated on a case-by-case basis.

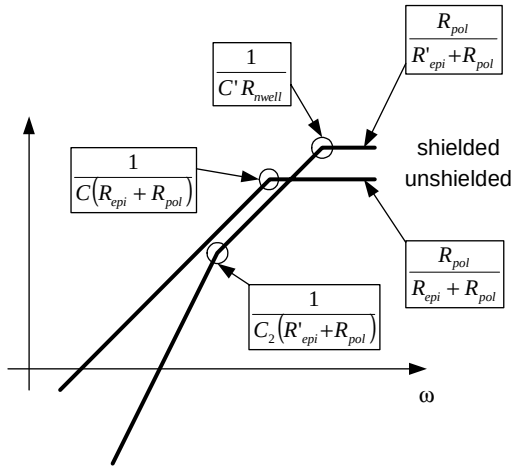

Fig. 9. Frequency responses for the two cases of injection.

A first guideline that derives from the above considerations is that shielding the digital structures is a good idea in order to reduce the amount of injected noise (indeed, the resistive divider (R_{pol} / R_{epi}+R_{pol}) provides a lower attenuation for the unshielded case). Of course, this ceases to be true for high frequencies. Therefore, depending on the particular range of frequencies at which the noise is injected, it may or it may not prove convenient to shield the digital structures. If the intersection point occurs at a high enough frequency, then the digital blocks should be shielded. Otherwise, shielding will be of little help, if any. In our case, Fig. 5 seems to suggest that the frequency at which the curves of Fig. 9 become flat lies around 300 MHz.

We will now focus our attention on noise collection. Fig. 10 to 13 show simple models for the four cases of noise collection studied with the test chip under consideration: NMOS, NMOS3W, PMOS and PMOS3W ("3W" means "shielded through triple well isolation").

Thanks to the simplifications made above, to a first approximation, noise collection can be seen as decoupled from injection because R_{epi} >> R_{pol}. Therefore, for the purpose of studying noise collection, we can assume that the bulk node of the integrated circuit acts as an ideal

voltage generator. In other words, we can simply assume that a given amount of noise lies in the substrate and propagates towards the surface through the epitaxial layer (R_{epi}). It is then quite easy to develop some intuitive considerations regarding the amount of shielding provided by each of the mentioned configurations.

If we compare the NMOS and the NMOS3W case, we immediately notice the two series capacitances provided by the two junctions of the n+ buried layer. These will attenuate noise at low frequencies. At high frequencies, nothing would change without the presence of the two additional resistances R_{nwell} and R_{pwell}. The effect of these two resistances is to reduce the amount of noise collected. At very high frequencies, however, the fact that R'_{epi} is lower than R_{epi} can have an adverse effect on shielding. Anyway, we can conclude that the NMOS3W case is much better than the NMOS case provided the frequency is not too high. The exact frequency values where the poles are located depend on specific technological parameters and, therefore, will vary with the application.

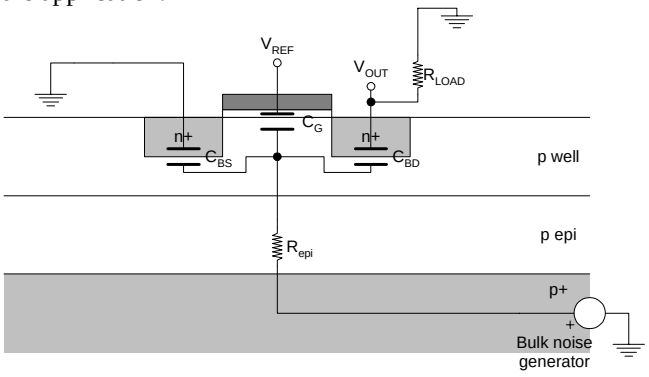

Fig. 10. Model for the unshielded NMOS.

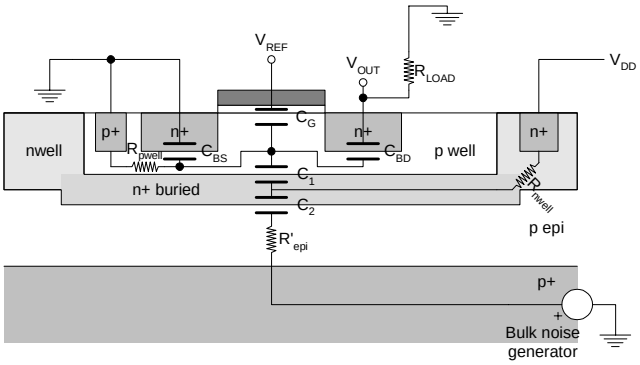

Fig. 11. Model for the shielded NMOS (NMOS3W).

The situation is completely different in the PMOS case. Comparing the PMOS case with the PMOS3W case, we immediately notice three differences:

1. the R_{nwell} resistance in the shielded case can be lower;
2. R'_{epi} is lower than R_{epi};
3. C_2 is much higher in the shielded case, due to the high doping of the n+ buried layer.

Point 1 has the effect of reducing the amount of collected noise, while points 2 and 3 have the opposite effect. Therefore, it is not clear whether the PMOS case is worse or better than the PMOS3W case. On the contrary, evidence seems to suggest that the shielded case is worse. In fact, looking at Fig. 6, the magnitude of the response for the PMOS3W case is higher than that of the simple PMOS case on a fairly large range of frequencies. Keeping in mind that, in that frequency range, injection is certainly lower (see Fig. 9), we can conclude that the PMOS3W case must be much worse than the PMOS case and that triple-well shielding is harmful for PMOS transistors. This is another important guideline that can be derived from the above measurements.

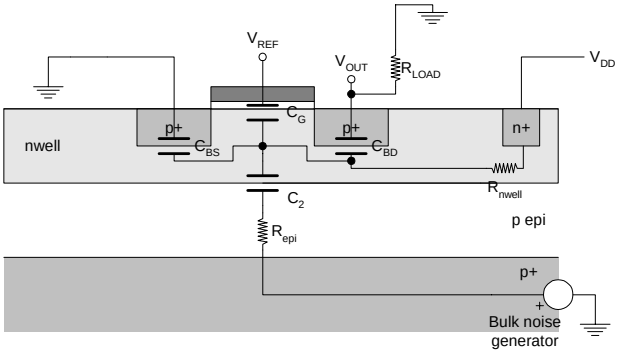

Fig. 12. Model for the unshielded PMOS.

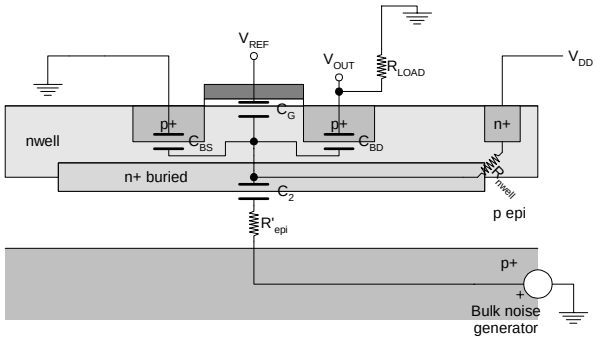

Fig. 13. Model for the shielded PMOS (PMOS3W).

5. Conclusion

In this work, some results on substrate noise coupling in triple-well CMOS ICs are reported, along with an interpretation of the measurements. It is shown that triple-well shielding is effective provided the frequency range of interest is not too large.

6. Acknowledgements

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7. References

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