Design of Rad-Hard SRAM Cells: 
A Comparative Study

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Abstract—This paper presents the design of three static RAM cells, designed to be radiation hard. The memory cells are designed with three different approaches and layout styles. Three memory arrays, each of them made with a different cell, were designed and simulated to optimize the transistor sizes. The layout of the cells has been drawn, and parasitic elements were extracted to analyze their impact on circuit performance. Simulation results demonstrate that the three cells are functional in all worst case corners. The sensitivity of each cell to single events has been estimated using a fault injection technique. A silicon prototype employing the first cell has been fabricated and characterized.

I. INTRODUCTION

During the last decades, the design of SRAM cell for space applications has changed [1]. Starting from the first satellite failure in 1963 due to damaging radiation effects, the interaction between radiation and electronic devices for aerospace applications has been carefully studied.

To improve the resistance to radiation, several solutions have been proposed. In the seventies, main solutions were based on the use of old fabrication technologies and of metal shields around electronic devices. Currently, solutions consist in improving manufacturing process and/or in improving designs: Radiation Hardening-By-Process (RHBP) and Radiation Hardening-By-Design (RHBD).

Today, the technical literature proposes solutions which are able to mitigate radiations. Solutions can be found at different levels of representation: at architectural level, at circuit level, and at layout level.

Radiation induces two types of effects: cumulative effects and single event effects. Cumulative effects are due to long time exposure to radiations, while single event effects are due to a single particle colliding into a sensitive node. Cumulative effects depend on the exposure time to radiation, and are predictable. On the contrary, single event effects are unpredictable and can be studied only on a statistical basis.

This paper presents an approach to improve radiation hardness of SRAM cells designed with the 6-transistor (6T) conventional architecture shown in Fig. 1.

The paper is organized as follows. Section II gives a review of the design techniques used. Section III illustrates the three different SRAM cells designed, and Section IV describes the structure of the cell array. Section V presents the results of fault injection simulations used to validate the design, and preliminary measurements obtained from the first silicon prototype.

II. RADIATION HARDENING-BY-DESIGN TECHNIQUES

In CMOS technology, the total dose produces charge trapping within the oxide. The most important cumulative effect is due to positive charges trapped in the region of transition from the thin gate oxide to the thick field oxide. Positive charges attract electrons near the lateral edges of MOS transistor gates, resulting in a leakage current which can be noticeable when an n-channel MOS transistor is in cut-off state. On the contrary, p-channel MOS transistors do not suffer from positive charge trapping, since the attracted electrons do not contribute to conduction.

A common solution to mitigate such effects is based on the design of circuit layout using n-channel Edge Less Transistors (ELTs), i.e., MOS transistors with edgeless shapes [2], [3]. Fig. 2 illustrates the layout of three MOS transistors, both with conventional shape (a), and with edgeless shape (b), (c). It is worth noting that ELTs can be designed either with overlapping source, as in Fig. 2(b), or with overlapping gate, as in Fig. 2(c). This choice can be exploited to obtain a given W/L ratio between two ELTs. From Fig. 2, it is easy to see that ELTs require an area larger than conventional MOS transistors.

To mitigate single event effects, some solutions have been developed. Single Event Upsets (SEUs) are mitigated by placing a Miller capacitor between the two
III. SRAM Cells

The 6T static RAM cells were designed in a commercial 180 nm CMOS technology, using three different strategies: (i) by designing all n-channel transistors with edgeless shape (ELT); (ii) by designing both ELTs and conventional transistors; and (iii) by designing only transistors with conventional shape. It is worth pointing out that both cell area and radiation hardness decrease from (i) to (iii). Therefore, a suitable trade-off between area and radiation hardness should be achieved.

Three SRAM cells have been designed, each cell design following one of the previously described strategies:

- **RadTrapH**, with 2 conventional p-channel MOS transistors and 4 n-channel ELTs. The two pass transistors are n-channel MOSFETs. This cell is the largest among the three designs, and occupies an area of 16.58 \( \mu m^2 \). It has been designed to meet the requirements of high energy physics experiments.
- **RadTrapS**, with 4 conventional MOS transistors (in the latch), and 2 n-channel ELTs as pass transistors. This cell has an area of 12.39 \( \mu m^2 \), and has been designed to meet the requirements of most space applications. The use of conventional n-channel MOS transistors leads to an increase of leakage current in the latches, due to the total dose.
- **RadTrapB**, with 6 conventional MOS transistors. The two pass transistors are p-channel MOSFETs. This cell has a surface area of 7.11 \( \mu m^2 \), and has been designed to meet the basic requirements of radiation tolerance. To save area, this cell has been designed without the Miller capacitance.

Fig. 3 shows the schematic diagram of the first two cells: RadTrapH and RadTrapS, where the word-line signal (WL) drives two n-channel ELTs. The schematic diagram of the cell RadTrapB is similar to the cell in Fig. 1, the only difference being the word-line signal (WL) driving two p-channel MOS transistors.

Fig. 4 shows the layout of the designed cells. All the cell layouts can be mirrored vertically and horizontally, in order to obtain a compact 4 \times 4 block which shares supply voltages, bit lines, and word lines. Instances of the 4 \times 4 block are replicated to obtain the SRAM array.

To validate the design of the SRAM cells, simulations have been performed to verify that the memory array works correctly in all design corners.

After the layout design, the first step is the extraction of parasitic components, in order to perform post-layout simulations.

Simulation of large cell arrays can be a hard problem. As a large array contains a huge number of components (transistors, parasitic capacitances, parasitic resistances), a huge number of equations must be solved to simulate the circuit, and a circuit simulator may require a long time to converge to the correct solution. For this reason, we have used a model reduction approach to simulate a large cell array, such as the 64 kbit block, in a reasonably short time. After the extraction of parasitic components, we have defined dummy cells containing only passive elements, i.e., parasitic resistances and capacitances. Following the same methodology, parasitic resistance and capacitance values have been extracted for an entire bit-line and for an entire word-line. By using dummy cells, a dummy matrix can be defined, which describes accurately all the parasitic elements in the circuit, while containing a limited number of components. In this way, a circuit simulator
reaches the convergence in few minutes. In particular, to simulate the 64 kbit block, the dummy matrix has three different levels of approximation: (i) the cells addressed during the simulation; (ii) the dummy cells arranged to create an RC net which replaces the selected and adjacent bit-lines and word-lines; (iii) the dummy word-lines and dummy bit-lines replacing the non-selected word-lines and bit-lines. Fig. 5 shows a diagram of the dummy matrix. Four complete SRAM cells are placed in the positions (1, 1), (1, 254), (254, 1) and (254, 254) within the array, and a frame of dummy cells surrounds a core composed by dummy word-lines and dummy bit-lines. By simulating the memory array, we optimized transistor sizes. Table I shows the sizes of transistors. It is worth noting that the width and length values of ELTs are “average” values extracted from the layout, taking into account the effects of gate corners in Figs. 2(b) and 2(c).

Simulation results confirm that the three cells are functional in all worst case corners.

IV. SRAM Block Array

The simplest solution to obtain a memory chip of 1 Mbit consists in splitting it into eight blocks of 128 kbit, each block storing one bit of a byte. This solution ensures that logically adjacent data (bits of the same byte) do not correspond to physically adjacent locations (cells of the array), thus avoiding Multiple Bit Upsets (MBUs) due to single events. All 128 kbit blocks must have the same size, i.e., the same number of rows and columns.

A block of 128 kbit can be obtained with an array made of 512 lines and 256 columns, or 256 lines and 512 columns.

From parasitic extraction, we have seen that an array with 512 rows leads to bit-lines having a capacitance so high that a bit-line precharged at the opposite logic value could write the selected cell in reading mode. On the other hand, in an array with 512 columns, word-lines exhibit a large delay due to RC distributed effects.

To avoid those problems, the number of both word-lines and bit-lines should not exceed 256. Therefore, it is necessary to split a 128 kbit block in two sub-blocks, each of them having 64 kbit. This solution can be achieved by placing the column decoders between two 64 kbit arrays, as shown in Fig. 6.

V. Simulation and Measurement Results

Time domain circuit simulations were performed on the back-annotated schematic diagram using Spectre.
TABLE I
SRAM Cell Transistor Size, Capacitance, Write Access Time, and SEU Threshold LET

<table>
<thead>
<tr>
<th>Cell</th>
<th>Latch transistor sizes</th>
<th>Pass transistor</th>
<th>Miller capacitance</th>
<th>Write access</th>
<th>Threshold LET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PMOS</td>
<td>NMOS</td>
<td>type and size</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RadTrapH</td>
<td>W = 2.267 (\mu)m</td>
<td>W = 1.820 (\mu)m</td>
<td>NMOS W = 1.689 (\mu)m</td>
<td>7.6 F</td>
<td>424 ps</td>
</tr>
<tr>
<td></td>
<td>L = 0.181 (\mu)m</td>
<td>L = 0.229 (\mu)m</td>
<td>L = 0.303 (\mu)m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RadTrapS</td>
<td>W = 1.865 (\mu)m</td>
<td>W = 1.719 (\mu)m</td>
<td>NMOS W = 1.591 (\mu)m</td>
<td>4.8 F</td>
<td>424 ps</td>
</tr>
<tr>
<td></td>
<td>L = 0.228 (\mu)m</td>
<td>L = 0.186 (\mu)m</td>
<td>L = 0.340 (\mu)m</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RadTrapB</td>
<td>W = 0.270 (\mu)m</td>
<td>W = 0.220 (\mu)m</td>
<td>PMOS W = 0.750 (\mu)m</td>
<td>0.8 F</td>
<td>530 ps</td>
</tr>
<tr>
<td></td>
<td>L = 0.180 (\mu)m</td>
<td>L = 0.180 (\mu)m</td>
<td>L = 0.180 (\mu)m</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 6. Two arrays of 128 kbit cells: (a) 512 rows and 256 columns, with decoders on two sides; (b) two sub-arrays, each of them having 256 rows and 256 columns, with the column decoder in the middle.

Simulation results show that the cell arrays work in read mode and in write mode in all worst case corners.

According to design criteria, we expect that RadTrapH cell is immune to TID, due to the use of edgeless MOS transistors in the layout design. An IC prototype employing the cell RadTrapH has been fabricated in a commercial 180 nm CMOS technology, and is already available. Radiation tests demonstrate that prototype samples are functional after a total radiation dose of 4 Mrad. The radiation hardness with respect to single event effects has been estimated through preliminary tests employing heavy ions. The IC prototype has an overall threshold Linear Energy Transfer (LET) of 4.85 MeV·cm\(^2\)/mg, and a cross-section saturation of 3.75 ·10\(^{-8}\) cm\(^2\). We expect that cell RadTrapL is able to sustain a total dose of 1 Mrad, while cell RadTrapL should be functional until 500 krad.

We have also simulated the SRAM cells using a fault injection technique, in order to estimate the radiation hardness of the designed SRAM cells. Fault injection has been performed using FISAR, a dedicated tool that accounts for circuit layout [6]. Fault injection simulation results confirm a good level of radiation hardness. Results of FISAR simulations are reported in the last column of Table I. As expected, the cell RadTrapH is the most resistant to single events, due to the larger capacitance value within the latch.

VI. Conclusion

Three different rad-hard SRAM cells have been designed, both with conventional MOS transistors and with edgeless transistors. By means of simulations, the three designs have been optimized, aiming at different levels of immunity to radiation.

An array employing the first memory cell has already been prototyped. Sample chips employing the first cell are available, and preliminary test results demonstrate an excellent hardness level with respect to the total radiation dose. The second memory cell has been employed for a test chip which is currently under prototyping. The third memory cell is being used in a new project recently started.

REFERENCES


