Design of an Ultra-Fast Low-Noise Charge-Sensitive Microprobe for Semiconductor Detectors

A. Pullia, E. Frontini, and S. Capra

***Abstract*–A low-noise wide-bandwidth charge-sensitive micro-probe is being developed, able to capture the charge signals of semiconductor detectors. The micro-probe works on a single terminated coaxial cable of whatever length, whose quality is crucial to achieving a good dynamic performance. The cable carries both the power supply (DC signal component) and the event pulses (AC signal component). No power-supply filtering capacitor is required. The micro-probe is particularly compact, consisting of a few devices, including a GΩ surface-mount resistor. Both a discrete-component and an ASIC version are under development. The ASIC version is designed in a 0.35 um 5V CMOS technology and is expected to be fully functional also at cryogenic temperatures. The area occupancy is 0.14 mm^2 bonding pads included. Thanks to such a large degree of integration the micro-probe can be placed very close to the detector electrode and is particularly light, compact and hence suited for hostile environments and for applications where a high radio-purity of the front-end is required, like in rare-decay research in underground laboratories. The rise time of the integrated version, as obtained from experimental results, is ≤ 2ns with a detector capacitance of 16pF. The energy range is beyond 20 MeV, and the power consumption is ~35 mW per channel. The gain stage includes an innovative low-frequency filtering device to provide a bias point to the system even if there are no constant voltage references such as conventional power rails. To achieve this result, CMOS transistors in underthreshold condition are used in combination with adequate capacitors in order to stabilize the source-to-gate voltage of the current generators. The first chip with various micro-probe versions is being tested.**

I. Introduction

THE presented micro-probe is an unusual and innovative charge-sensitive preamplifier [1]. What distinguishes it from common CSPs [2]-[13] is its lack of a proper power rail. It features only one output, on which both the power supply and the output signal coexist. The micro-probe preamplifier is a miniaturized circuit which can capture charge signals. Thanks to its high degree of integration, it can be placed very close to the probe tip. This is an important aspect, since it is well known that the parasitic capacitance referred to the input node of a charge-sensitive preamplifier has a negative influence on the noise performance. The output connection is provided by a shielded cable, whose quality it crucial to ensure best behavior of the preamplifier. The first design of the circuit consisted of an integrated N-MOS input transistor, a discrete J-FET in a cascode configuration, one or two discrete BJTs for the gain stage and a bunch of passive components. The version currently under development is a more integrated one. It is realized in AMS C35 technology and uses the 5V module of such technology. The output voltage swing ensures wide dynamic range, both for electron and hole signals. In a typical configuration the linearity is assured for 30MeV hole signals and 20 MeV electron signals. The only external component is the feedback resistor, although some promising studies about high-value integrated resistors are being carried out [14]. We realized also a prototype with a 100MΩ integrated poly-silicon feedback resistor, which will be tested soon. This preamplifier is characterized by a wide bandwidth and is particularly suited for managing fast signals. The microprobe could be used as front-end for ionizing radiation/particle spectroscopy with e.g. single-crystal diamond detectors, pixelated CdTe/CZT, silicon, silicon-carbide, and other semiconductor detectors. The whole preamplifier consists only of few components and does not even require filtering capacitors. For these reasons it could be used in those contexts where high radio-purity is required, such as in the underground laboratories for rare-decay research [15]. The probe can be connected to the detector both in AC or DC configuration. Since there are no constant voltage references in the circuit, the most important part of the preamplifier is the bias network. It implements an innovative ultra-low-frequency filtering mechanism which provides current/voltage references suitable for the purpose. It is based on MOS transistors biased in under-threshold conditions which act as high-value resistors. The DC operating point is derived from the threshold voltage of the input transistor. However it can be tuned acting on two simple resistors. Future implementations will provide the possibility to adjust this parameter according to the experimenter's needs, in order to maximize the positive or the negative dynamic range. The chip was submitted to the foundry in late 2013. We started the testing phase in the second half of 2014. In this paper the preliminary results will be presented. The component count is so low that the area occupation on silicon is dominated by the bonding pads. The micro-probe is depicted in Fig. 1 for the cases of DC or AC coupling to the detector. The remote receiver constitutes a fundamental block of the circuit, but, since it deserves a particular analysis, it will be discussed in another work.

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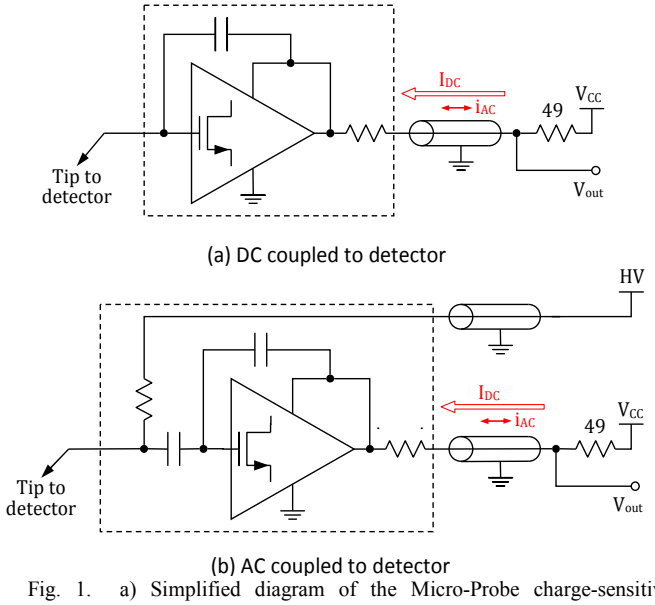

Fig. 1. a) Simplified diagram of the Micro-Probe charge-sensitive preamplifier coupled to the detector in DC configuration. b) Simplified diagram of the Micro-Probe charge-sensitive preamplifier coupled to the detector in DC configuration. Please notice that the coaxial cable carries both the DC bias current and the AC output signal. The far-end receiver is omitted for clarity.

II. Circuit Description

Fig. 2 shows the core of the micro-probe preamplifier. The whole circuit consists of just four active components, excluding the bias network. The highest voltage in the circuit is the output voltage itself. The lowest voltage is ground, to which is connected also the bulk of the chip. T_1 is the input transistor. The signal it generates is collected by T_2, which works in cascode configuration in order to minimize the effects of the parasitic gate-drain capacitance of T_1. T_4 is a current generator which determines the bias point of T_1. T_4 acts also as active load for the current generated by T_1. The output of this first stage is connected to the gate of T_3, which can be considered both the gain and the output stage of the preamplifier. It is quite unusual to implement such a structure with a non-constant power rail. The main constraint for its functionality is that T_4 must generate a constant current independently on the value of Vout. This means that the voltage difference between the source and the gate of T_4 must be kept constant. Besides that, T_2 acts as a good cascode transistor only if its gate voltage does not fluctuate. Generally it's quite difficult to achieve this task without a reference voltage. The solution to these two main problems is found in the bias network, shown in Fig. 3. We obtain the voltage difference between the source and the gate of T_4 from the bias point of T_5, connected as a trans-diode. The current it generates is defined by R_3. The gate voltage of T_5, referred to Vout, is filtered with T_8 and C_1. The capacitors are realized with a standard poly-silicon module. It is really important to connect C_1 as shown in Fig. 4. If we connected C_1 upside down we would obtain poor filtering performance. In fact the parasitic capacitance between the lower poly-silicon plate and bulk would induce voltage fluctuations on the gate of T_4 due to capacitive voltage partition between Vout and ground.

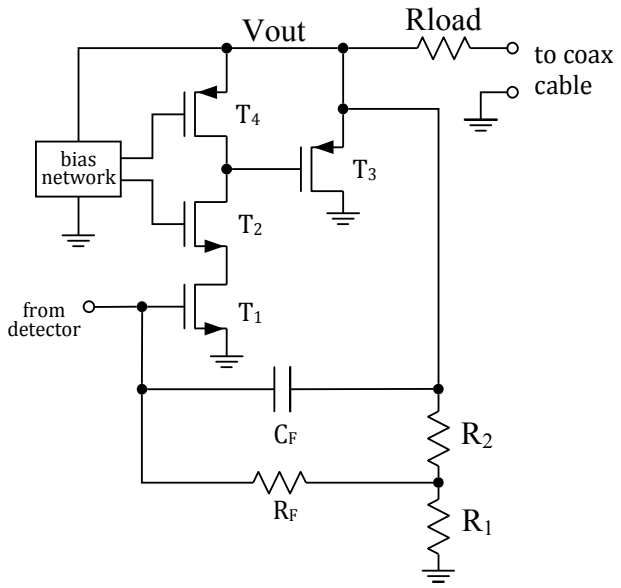

Fig. 2. Simplified schematic diagram of the ASIC version of the Micro-Probe charge-sensitive preamplifier. All components are integrated except for the feedback resistor R_F which is kept external. However a test version was produced with an integrated polysilicon 100MΩ resistor.

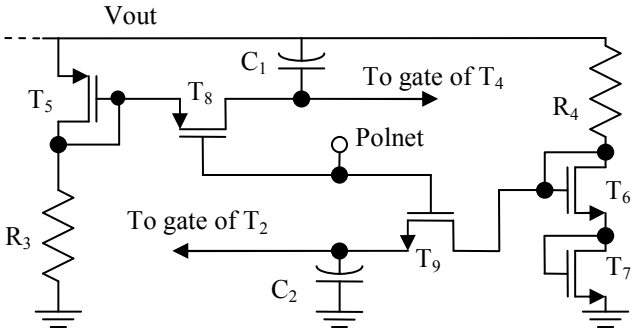

Fig. 3. Simplified schematic of the bias network. The Polnet control allows adjustment of the bias point of T_8 and T_9 with an external voltage. This line is protected with adequate ESD structures, since it's directly referred to T_8 and T_9 gate contacts.

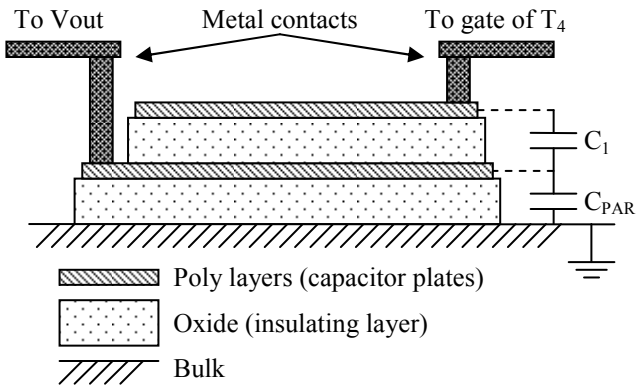

Fig. 4. Cross-section of capacitor C_1. It is realized with a standard foundry cell made of two poly-silicon layers. It is worth noting that the main capacitor is coupled to bulk with a relative large parasitic one. The correct connection of C_1 is as shown. Switching the electrodes of C_1 would yield poor filtering performances, due to a voltage partition between Vout and ground.

On the other hand the connection of C_2 as in Fig. 3 ensures the optimization of the ratio between its value and area. In this case the parasitic coupling to bulk of the lower plate is used to boost the value of the capacitor module. In fact we want the gate of T_2 to have a fixed voltage respect to ground. Thanks to the voltage defined by the Polnet node, T_8 and T_9 work in under-threshold condition, acting as high-value resistors. The time constants defined by T_8C_1 and T_9C_2 ensure good stability of the absolute references generated. Thanks to such references the microprobe works properly even without a conventional power rail. At the moment Polnet is set from outside the chip with a resistive voltage divider between Vout and ground. This choice is related to the possibility to test the behavior of T_8 and T_9 with different gate voltages and temperatures. In the final version of the device this voltage will be provided internally without external connections.

The total load of the circuit is the sum of Rload and the 49Ω resistor on the far side of the coaxial cable. Since the risetime of the circuit in most configurations is in the ns range, signal termination at the far end of the coaxial cable is mandatory. For DC bias reasons Rload is chosen to be 220Ω. The receiver impedance should be as close as possible to 50Ω in order to avoid signal reflections. The static power consumption is ~35mW. The ability to drive directly a coaxial cable connected to a far-end receiver constitutes a great feature of the device, which provides by itself the connection between the front-end and the back-end electronics. The DC operating point of the circuit is obtained projecting the threshold voltage of T_1 with the two resistors R_1 and R_2. The voltage of Vout in static conditions is determined by (1).

$$V_{out,DC} = V_{TH,T1} \cdot \left(\frac{R_1+R_2}{R_2}\right) \qquad (1)$$

This is obtained with the particular connection of the feedback resistor shown in Fig. 3. This configuration unfortunately has the drawback of increasing the time constant of the preamplifier. This generally is equal to $R_F C_F$, but in this case its value is

$$\tau = R_F C_F \left(\frac{R_2}{R_1+R_2}\right) \qquad (2)$$

A well-stabilized and filtered power rail must be provided on the receiver side in order to obtain best noise performances.

III. Dynamic Properties

The slim design introduces very few high-frequency parasitic poles, so that the circuit can work without compensation. This allows a very wide bandwidth and thus a fast transition time. In Fig. 5, 6 and 7 the micro-probe response signal is represented for test pulses of different risetime. The chosen detector capacitance is 15pF. Please note that the small voltage bounces 10-15ns after the main pulse are due to improper signal termination on the receiver side and do not depend on the preamplifier itself. The ringing is acceptable for most applications. Response signals for even faster test pulses will be provided in the near future.

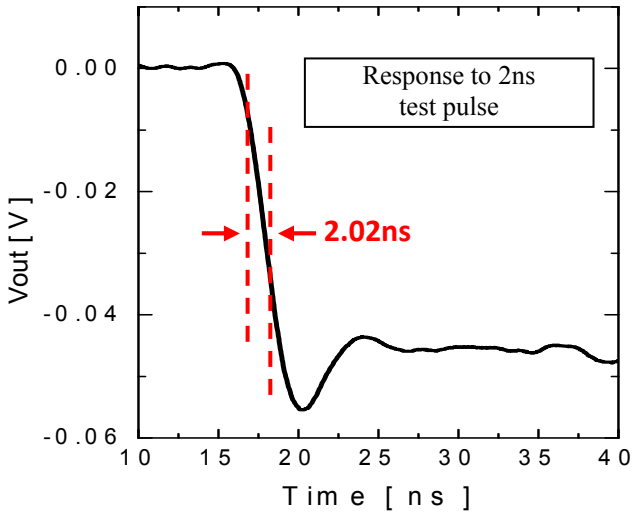

Fig. 5. Output signal of the micro-probe preamplifier in response to a test pulse of 2ns risetime. C_{DET}=15pF. The DC voltage is neglected.

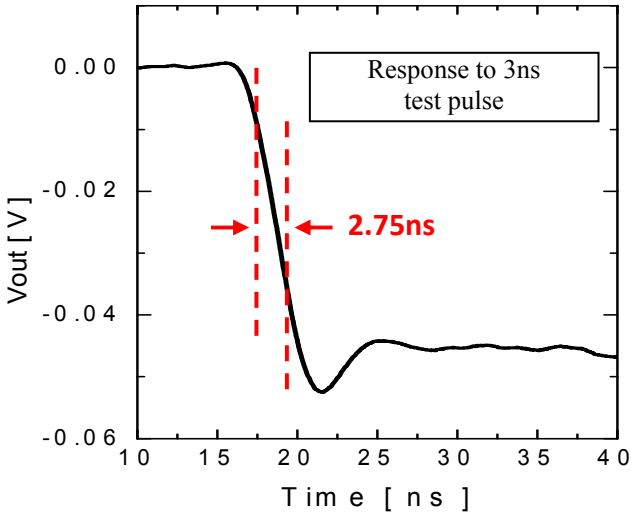

Fig. 6. Output signal of the micro-probe preamplifier in response to a test pulse of 2ns risetime. C_{DET}=15pF. The DC voltage is neglected.

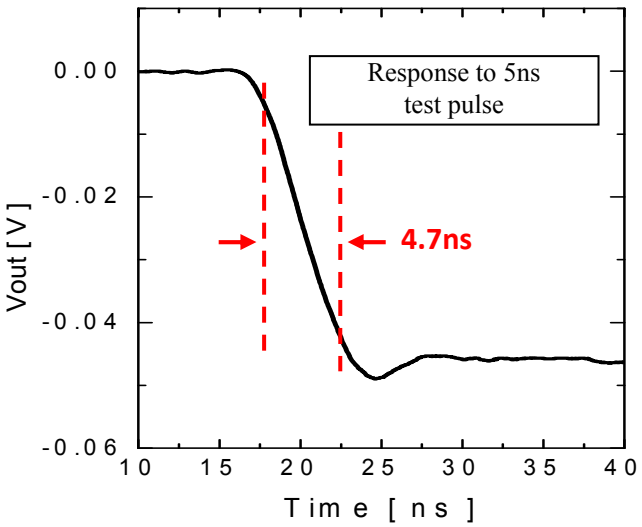

Fig. 7. Output signal of the micro-probe preamplifier in response to a test pulse of 2ns risetime. C_{DET}=15pF. The DC voltage is neglected.

The structure of the circuit provides a wide voltage swing at the output. This ensures very good linearity over a wide dynamic range. In Fig. 8 we can see the output signals of the micro-probe for test pulses of different energy. In Fig. 9 the linear fit of the signal amplitudes shows an excellent linearity over 20MeV range. We emulate the charge production of a germanium detector with a pulser and a test capacitor.

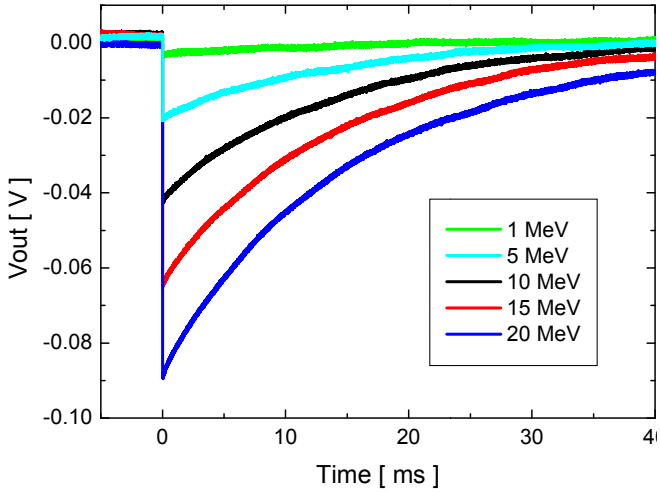

Fig. 8. Output signals of the ASIC micro-probe for test pulses of different amplitudes. The energies are referred to the typical charge production of germanium detectors. C_{DET}=15pF.

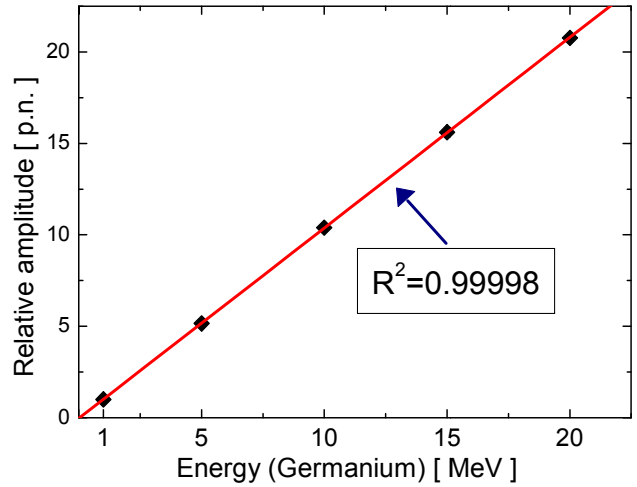

Fig. 9. Linear fit of the amplitudes of the signals plotted in Fig. 3. The value of R^2 shows an excellent linearity over a 20MeV range.

IV. Layout

In Fig. 10 the layout of the micro-probe is shown. The area is only ~0.14mm^2, bonding pads included. The circuit is very compact and shows a high degree of integration. The bonding pads were placed on a single row because the micro-probe was realized as a part of a bigger test chip. The shape of the layout was aimed to the optimization of the area occupancy. In the bottom of the figure C_1 is clearly visible. Its area is so large because higher capacitance values yield better filtering results in the biasing of T_4.

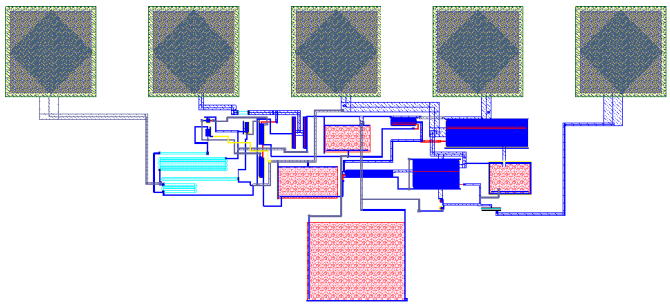

Fig. 10. Layout of the micro-probe. The design was submitted to the foundry in late 2013. Experimental test started in the second half of 2014.

V. Conclusions

The results of the first experimental tests of an innovative charge-sensitive micro-probe were presented. The wide bandwidth allows this preamplifier to resolve fast detector signals in the nanosecond range. The experimental linearity performance is in agreement with computer simulations. More tests will be performed in the near future, especially from the noise point of view. On the same test chip a micro-probe version with integrated 100MΩ feedback resistor was also realized. That version does not require any external component and is particularly promising for those applications where a high radio-purity degree is required. The next step will be the design and realization of a proper far-end receiver to optimize the dynamic and noise performances of this preamplifier.

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