EXPERIMENTAL PERFORMANCE OF THE I^2C INTEGRATED MULTICHANNEL CHARGE-SENSITIVE PREAMPLIFIER OF TRACE

S. Capra, D. Mengoni, R. J. Aliaga, A. Gadea, A. Pullia

***Abstract* – The latest experimental results of the multichannel CSP ASIC for TRACE detector are shown. The device, submitted to the foundry in the middle of 2014 and received at the end of the same year has been installed on a dedicated pcb and tested using a pulser. The device features four channels specifically designed for hole signals and one channel for electron signals. The power consumption is around 10 mW per channel as required by the specifications of TRACE. The main design goals are low noise and fast rise time. With proper shaping of the signals this device is capable of producing energy spectra with resolution of approximatively 1keV. The rise time of the leading edge of the signals is fast enough to perform pulse-shape analysis of the waveforms. The key feature of this device is the possibility to switch some internal components as desired through an I^2C bus. In this way some critical parameters, such as bandwidth and gain of the preamplifier, can be adjusted and optimized according to experimental needs.**

I. INTRODUCTION

TRACE is an array of Silicon pad detectors in a telescopic configuration for nuclear physics experiment with radioactive ion beams [1]. Any single detector consists of 60 square pads, arranged in 5 rows and 12 columns. The width of the pad is 4 mm. The telescopic configuration enables the experimenter to discriminate the impinging particles using an E/ΔE method. The less energetic particles tend to be stopped by the first thinner layer of silicon. In these cases it is impossible to apply the E/ΔE method for particle recognition. In order to extend the discrimination capabilities of TRACE in the low energy range down to the limit of 5-10 keV, pulse-shape analysis is performed. This technique requires analysis of the current profile of the detector pulses. Different particles yield slower or faster signals. The typical width of the current pulses is in the order of 10 ns for the thinner ΔE layer. Diamond detectors have a fast risetime in the order of 1ns and require a different kind of CSP [2]. This means that charge-sensitive preamplifiers must provide signals fast enough to preserve that information. In the foreseen experimental setup a large count of channels are packed inside the relatively small volume of the scattering chamber and the front-end electronics works in vacuum [3]. Not only the form-factor but also the power dissipation constraints force the designer to opt for integrated solutions. We designed and realized an integrated multichannel charge-sensitive preamplifier suited for this application. Its main features are low power consumption, low noise and fast rise time. A host of critical circuit parameters can be adjusted through an I^2C bus, choosing from a set of predefined values. In this way the preamplifier can be arranged to work properly with different detector capacitances, ensuring best rise time with little or no ringing in a wide range of different conditions.

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S. Capra is with the Physics Department of University of Milano and INFN of Milano, Italy (email: stefano.capra@unimi.it)

D. Mengoni is with the Department of Physics and Astronomy, University of Padova, Padova, Italy and INFN, Padova, Italy.

R. J. Aliaga and A. Gadea are with the Instituto de Física Corpuscular · Department of Experimental Physics, Paterna, Valencia, Spain.

A. Pullia is with the Department of Physics, University of Milano, Italy, and INFN of Milano, Italy (email: alberto.pullia@mi.infn.it).

II. TECHNICAL DETAILS

The multichannel CSP ASIC [4] comprises four channels optimized for hole signals and one channel specifically designed for electron signals. They can be powered independently as required by experimental conditions. The chip is realized in AMS 0.35 um technology. It is well known that scaled technologies can tolerate progressively smaller power supplies. This can be helpful in terms of reduced power dissipation, but has some well-known drawbacks. Lower power supplies yield lower output voltage swing of the ASIC preamplifiers and thus limit their dynamic range, which is smaller than that the one of discrete preamplifiers [5-10]. For this reason the 5V module of the technology was chosen instead of the normal 3.3V one. This choice, together with a smart design of the preamplifier, ensures a wide dynamic range without linearity issues. The low-impedance output stage is able to drive a 50Ω coaxial cable without appreciable distortion for signals up to 2V peak-to-peak. Depending on the value of feedback capacitance set through the I^2C interface this voltage limit corresponds to different energy values. For a typical value of 1pF linearity is ensured within a ~33MeV range for germanium detectors and ~41MeV for silicon ones. Another aspect that required great effort was minimization of the noise. Optimization of the input stage is key in this respect because it typically introduces the dominant contribution to the overall noise of the circuit. In order to minimize the equivalent noise charge high-transconductance input transistors must be used. Transconductance is increased as channel width is increased and channel length is reduced. Unfortunately the 1/f series noise goes as the inverse of the area. This means that the best noise performance is achieved with a trade-off between smaller and larger lengths of the input transistors. The solution proposed is able with proper pulse shaping to achieve the ENC performance of 128 electrons r.m.s. with 4pF detector capacitance and typical preamplifier configuration. It is well known that power and speed always share a trade-off relationship. The device is able to provide signals with leading-edge faster than 10ns, with an experimental power consumption of just 10mW per channel.

III. I^2C ENGINE

The main advantage of implementing a digital interface inside an integrated CSP is the possibility to adjust critical parameters of the circuit without adding external components. With our design the experimenter can choose between four different values of both bandwidth and gain. The bandwidth depends on the selected value of the Miller compensation capacitance. The maximum value is 5pF. The gain depends on the selected value of the feedback capacitance. This one can be 0.2, 0.5, 0.7 and 1pF. The ability to adjust the bandwidth is important when connecting the preamplifier to detectors with different capacitance. This value influences the open-loop gain of the system and thus has great impact on stability. If the experimenter can vary the bandwidth according to his needs he can optimize the rise time avoiding instability problems and ringing. Wider bandwidth configurations yield faster leading edges but could introduce ringing in the fast transients. Reduced bandwidth configurations are safer from this point of view but could spoil the preamplifier performance if pulse-shape analysis is required. It's up to the experimenter to choose the best configuration on a case-by-case basis. Other parameters that are adjusted through the I^2C bus are the bias current of the input stages and the speed of the fast-reset device [11], [12]. This one is an innovative anti-saturation mechanism. Large signals from the detector tend to saturate the output stage of the preamplifier. A comparator detects this condition and activates a constant and controlled current generator. This one draws charge at a constant rate from the input node of the preamplifier until the 0V baseline at the output is restored. It was shown in previous works that the time-over-threshold analysis of the comparator signals can be used to estimate the event energy even in case of deep saturation of the preamplifier. This is possible because even in case of saturation the physical charge provided by the detector is conserved on the input node of the preamplifier. We can deduce the amount of such charge looking at the time required by a constant current to fully draw it away. This technique can be used to extend the spectroscopic dynamic range of the preamplifier connected to the back of the detectors while it will be used just to reduce dead-time in the hole channels connected to the front pads.

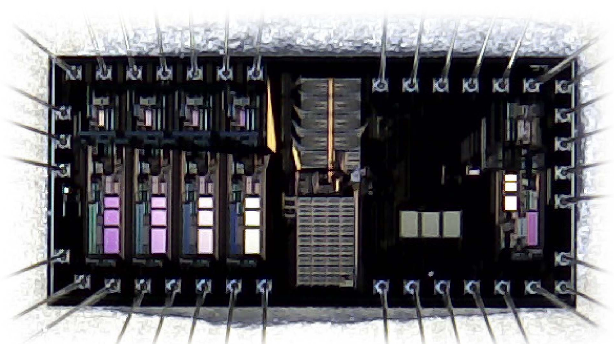

Fig. 1 – Photograph of the 3.3mm x 1.5mm chip wire-bonded in the cavity of a PLCC44 carrier. This image was taken with a magnifying camera connected to a PC through USB communication. The four blocks on the left are the hole channels, the block on the right is the electron one and the structure in the middle is the I^2C engine.

IV. Conclusions

A multichannel integrated charge-sensitive preamplifier was realized and experimentally characterized. The chip, wire bonded in a PLCC44 carrier was installed on a dedicated PCB and fully tested. Experimental tests ensure the compatibility of this device with the requirements of the FEE of TRACE. Future developments will provide additional functionalities, such as the possibility to trigger the reset procedure from a remote device and, if possible, some further enhancements in terms of power consumption. We have also developed a particular time-to-amplitude converter that produces analog signals with amplitude proportional to the energy measured with the fast-reset process. Those signals do not require any kind of shaping and can be sent directly to an ADC [13-15].

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