Conceptual design of the TRACE detector readout using a compact, dead time-less analog memory ASIC

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ABSTRACT

The new TRacking Array for light Charged particle Ejectiles (TRACE) detector system requires monitorization and sampling of all pulses in a large number of channels with very strict space and power consumption restrictions for the front-end electronics and cabling. Its readout system is to be based on analog memory ASICs with 64 channels each that sample a 1 μs window of the waveform of any valid pulses at 200 MHz while discarding any other signals and are read out at 50 MHz with external ADC digitization. For this purpose, a new, compact analog memory architecture is described that allows pulse capture with zero dead time in any channel while vastly reducing the total number of storage cells, particularly for large amounts of input channels. This is accomplished by partitioning the typical Switched Capacitor Array structure into two pipelined, asymmetric stages and introducing FIFO queue-like control circuitry for captured data, achieving total independence between the capture and readout operations.

1. Introduction

The TRacking Array for light Charged particle Ejectiles (TRACE) [1,2] is a new telescope detector system for the discrimination of particles and light ions in fusion evaporation and direct nuclear reactions, designed to work in combination with a large gamma tracking array like AGATA [3]. Each detector cell is a $\Delta E-E$ telescope consisting of a double silicon layer with respective thicknesses of 200 μm and 1 mm, forming a 12×5 array of pads with a 4×4 mm^2 pitch, and a resistivity of 20 kΩ/cm. Identification of different ions and particles relies on both $\Delta E-E$ discrimination and Pulse Shape Analysis (PSA) [4] based on the sampling of all detector pulses generated at the silicon pads. The first experimental tests have already taken place with temporary readout electronics using commercial DAQ modules and only a limited number of detector channels [5]. It has been established that acquisition windows of 1 μs at 200 MHz sampling frequency or higher are required for PSA [6] as imposed by the fast signals induced by light particles [7].

The final readout system for TRACE requires monitorization of all detector channels and sampling all generated pulses, which may appear in any channel; specifically, one front channel per silicon pad with hole signals is required for particle discrimination, plus one back channel per layer with electron signals that will be used mainly for spectroscopy. An event rate in the range of tens of kHz is expected, and an energy resolution below 1% at 5 MeV is to be obtained at room temperature. The complete front-end circuitry for each detector needs to fit in a 25×50 mm^2 circuit board, with a similar size as the detector itself. This imposes very strict space and power consumption restrictions for the front-end electronics and cabling. A total of 122 channels (120 front and 2 back) need to be read out per detector and captured information should be transmitted serially in order to keep cabling to a minimum. At the same

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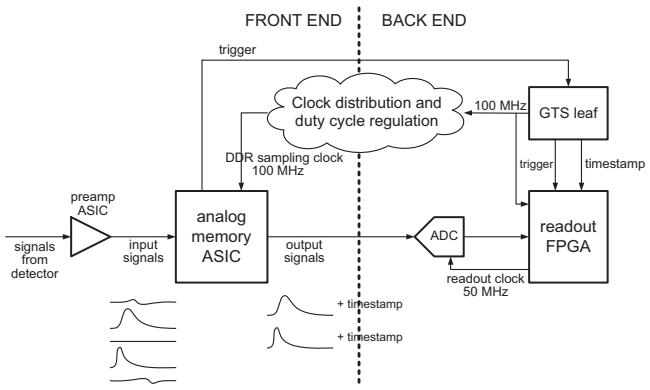

Fig. 1. Simplified schematic outlining the location and role of the analog memory ASIC and its interface with other system components.

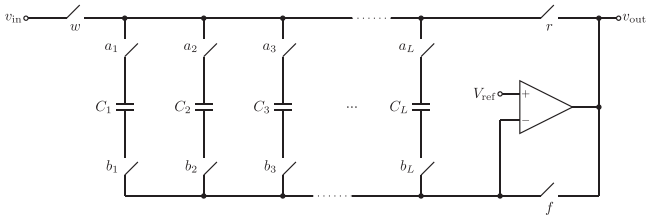

Fig. 2. Selected implementation of a single SCA channel using a common operational amplifier. Odd and even capacitor switches are controlled by alternating clock edges for double sampling rate.

time, heat sinking is limited by the small dimensions of the vacuum reaction chamber, and a maximum power budget around 20 mW per channel is estimated.

The aforementioned specifications strongly favor the implementation of zero-suppression and serialization at the front-end while avoiding power-hungry free running digitizers. A triggerless readout scheme has been devised that relies on an analog memory ASIC with self-triggered channels for the sampling of detector pulses and their later retransmission at a slower pace. For this purpose, a novel analog memory architecture based on multiple Switched Capacitor Array (SCA) stages is presented that has been specifically designed to minimize detector dead time and area occupation per channel. This paper describes the general readout scheme, the conceptual design of the analog memory ASIC, and its current design status.

2. TRACE readout scheme

The proposed readout scheme is depicted in Fig. 1 and involves two types of ASIC for the front-end electronics. The ASIC dies will be directly wire-bonded to the front-end PCBs for minimal area requirements.

The first ASIC type, described in [8,9], includes charge-sensitive preamplifiers designed for low power and low area occupation by requiring only one external component per channel. Their operating point settings can be individually tuned through an I^2C interface for maximum bandwidth, in order to comply with PSA requirements. Smart fast-reset circuitry is included for each channel that allows fast capacitor discharge in case of saturation by connecting a constant current sink. Moreover, this discharge mechanism allows an extension of the dynamic range for energy estimation on the back channels beyond saturation by implementing Time-over-Threshold (ToT) measurement [10]; time-to-amplitude converters have been added to these channels for direct amplitude spectroscopy.

The second ASIC model is an analog memory circuit whose purpose is to detect any pulse signal coming from the preamplifiers and sample its waveform while discarding any other signals. Up to 32 samples are to be captured before the actual pulse edge for baseline estimation, plus 192 samples corresponding to the pulse waveform, for a total capture window of 1.12 μs at a 200 MHz sampling rate. Moreover, for the back channel, the final, stable output from the time-to-amplitude converter needs to be sampled as it provides the energy measurement in case of saturation. Captured signals are timestamped and transmitted serially to the back-end by means of a single analog output; they are digitized remotely and processed by a FPGA that controls the readout process at 50 MHz.

The analog memory ASIC is also responsible for communication with the Global Trigger and Synchronization (GTS) subsystem to be used in conjunction with AGATA [11]. In particular, trigger request signals have to be issued for every detected pulse, and the sampling clock is generated from the 100 MHz clock given by the GTS leaf by means of a common clock distribution network that provides phase-aligned, 50% duty cycle clocks to the analog memory ASICs for all detectors. Both clock edges are used for sampling. Each ASIC contains a local 36-bit timestamp counter for pulse tagging, and counters from different ASICs may be aligned by resetting them at the same time. A synchronization procedure is foreseen in order to match the internal ASIC timestamp counter with the global timestamp counter in the GTS infrastructure.

For the preamplifier ASICs, multichannel prototypes with four front channels plus one back channel have already been fabricated in 0.35 μm CMOS technology and are pending experimental validation, and future versions with up to 12 channels are planned. The analog memory ASICs are currently under design using 0.18 μm CMOS technology for reduced power consumption and area; the final design is planned to host 64 input channels, so that two of them would be required per detector element. Their architecture is described in detail in the next section.

3. Analog memory ASIC

The architecture and principle of operation of the analog memory ASIC is based on the use of SCAs for the fast analog sampling of transient signals that are stored as charge in internal capacitors and can be later read out at a slower pace. These devices have been used as low-power substitutes for flash ADCs for the past 25 years; some of the most representative examples are described in Refs. [12–19]. SCA channels are the basic building blocks of the presented ASIC architecture, so a general description is included here first.

3.1. Switched Capacitor Array channels

The particular SCA channel structure employed in this ASIC is depicted in Fig. 2, based on the use of a common operational amplifier to assist in writing and reading operations. The input signal is connected through a switch w to a common bus from which a number L of storage cells hang, each containing a capacitor and a pair of control switches. With switches w and f closed and r open, cell C_i is written by closing switches a_i and b_i, so that the bottom plate of C_i is biased at a reference voltage V_{ref} and the capacitor gets charged and tracks the input signal. When switches a_i and b_i are opened, the capacitor holds the analog signal value at opening time. Switches in consecutive cells are closed and opened sequentially with a write frequency f_w following a circular buffer logic in such a way that, at any given time, the array cell capacitors are holding successive samples of the input signal corresponding to a time window of length L/f_w.

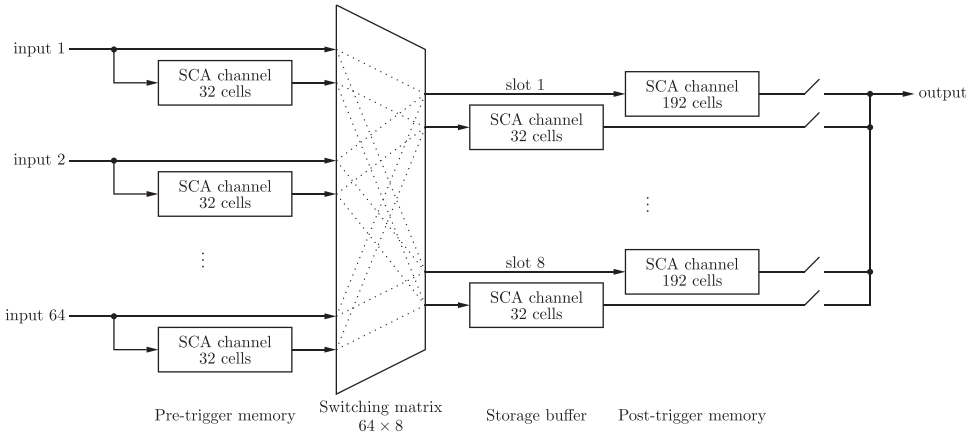

Fig. 3. Pipelined SCA architecture with separate channels for pre-trigger (left) and post-trigger (right) memory connected through a switching matrix. An additional channel in the right section acts as a storage buffer for the pre-trigger memory.

This continuous writing operation is stopped when a trigger condition is met for the channel and all switches are opened. A readout process may then begin after closing switch r, where switch pairs a_i and b_i are sequentially closed in order to dump the stored voltage values into the bus and to the output with a read frequency f_r. These values are then sampled using an external ADC. The SCA channel is locked for writing until readout has been completed, so as to avoid overwriting the capacitor contents. In most analog memory designs, this induces a dead time in the channel which may be very long compared to the pulse acquisition window, since f_r is typically much lower than f_w. The next section will describe a way to circumvent this issue.

The settling time of the amplifiers driving the writing process, in particular the preamplifier driving the bus input signal, must be low enough that the input voltage may effectively be stored in the capacitor during the time interval when the write switches remain closed. In order to ease the specifications on settling time and increase the tracking window, switches from consecutive capacitor cells are driven by the positive and negative edges of the sampling clock, respectively, so that the sets of odd and even cells are equivalent to two parallel subsections sampling the incoming signal at a 100 MHz rate with a phase difference of π, effectively providing a 200 MHz sampling rate.

3.2. Pipelined asymmetric SCA

Typical analog memory circuits merely replicate the single channel structure described above for every input channel. A different approach is adopted here: the SCA is pipelined into two sequential, asymmetric stages connected through a full-mesh switching matrix. The general scheme is shown in Fig. 3, where the circuit has been divided into a first memory stage with a 32-cell SCA channel intended for pre-trigger samples for each ASIC input, and a second stage with 8 slots, each containing a 192-cell SCA channel for post-trigger samples and an auxiliary 32-cell SCA channel intended as a storage buffer for the samples in the first stage.

Initially, the second SCA stage is idle, and each channel in the first stage is continuously sampling the associated input signal, so that it contains the last 32 samples at any given moment. Whenever an input channel is triggered, the corresponding channel i in the first stage is write-locked and its samples are held; a free slot j in the second stage is then assigned and both are connected together through the switching matrix. At this moment, the input signal is connected to the write bus of the 192-cell SCA, so pulse capture continues there. At the same time, the contents of channel i are sequentially read and copied to the 32-cell buffer in slot j, so that the data transfer is complete before capture of the 192 post-trigger samples ends. At this point, the input channel is immediately ready to start sampling again; therefore, no dead time is introduced. The whole captured pulse is stored in slot j, and it remains locked until it is read out sequentially. The logic for assignment of free slots and their readout makes them behave like a FIFO queue.

The main advantage of this architecture is the reduced number of total memory cells. A total of 224 samples are captured for every detected pulse; a full SCA with a typical structure would therefore need $64 \times 224 = 14\,436$ cells. However, the pipelined asymmetric SCA structure only requires $64 \times 32 + 8 \times 224 = 3840$ cells, resulting in an approximate 4-fold reduction in area occupation for storage. This is accomplished by sharing storage resources among all input channels. The reduction factor depends on the dimensioning of the whole memory and is better for more asymmetric designs.

A second advantage is the lack of readout-related dead time for single channels, which is a novel feature to the best of the authors' knowledge. The analog memory ASIC exhibits dead time only in the case when the output queue is completely full; in that case, all input channels are locked. Nevertheless, a relatively low event rate is expected in TRACE, making this an unlikely situation whose probability may be estimated and used for dimensioning.

This architecture also presents some disadvantages compared to the use of full channels for every input. One of them is a slight loss of flexibility, in that the maximum amount of pre-trigger samples and of simultaneously stored pulses is lower. Another one is the fact that pre-trigger and post-trigger samples are processed along separate paths with different responses; specifically, pre-trigger samples undergo an extra copy operation when being transferred from the first into the second stage, whereby additional noise is introduced. The signal-to-noise ratio for these samples may therefore be slightly lower than for the post-trigger section. However, pre-trigger samples will be mainly used for estimation of constant voltage levels (either baseline or ToT output from back channels) so the impact of this SNR difference will be largely diminished. In any case, both signal paths need to be characterized separately, which adds complexity to the calibration procedure.

3.3. Input stages

A schematic of the input stage for each ASIC channel is depicted in Fig. 4. It consists in an inverting amplifier with gain $-R_2/R_1$ that adapts the signal range between the preamplifier output and the SCA; R_2 is internal to the ASIC and fixed but R_1 is external and can

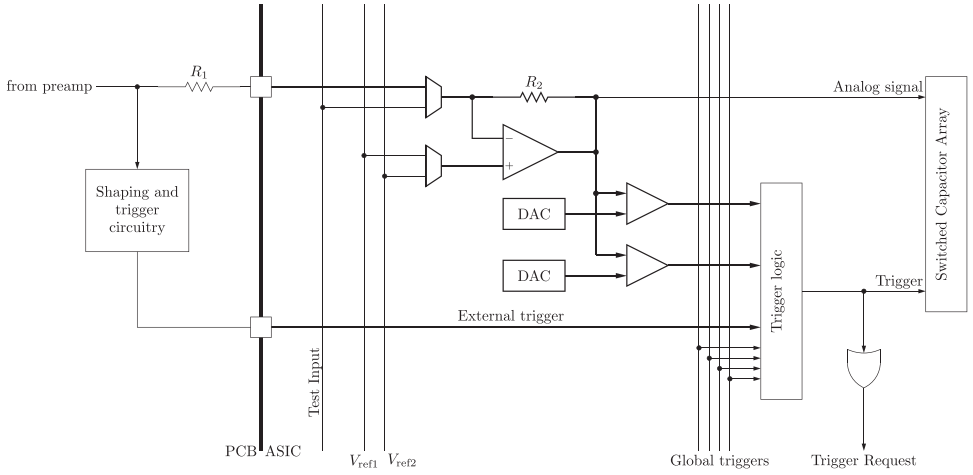

Fig. 4. Diagram of the input stage for each analog memory channel.

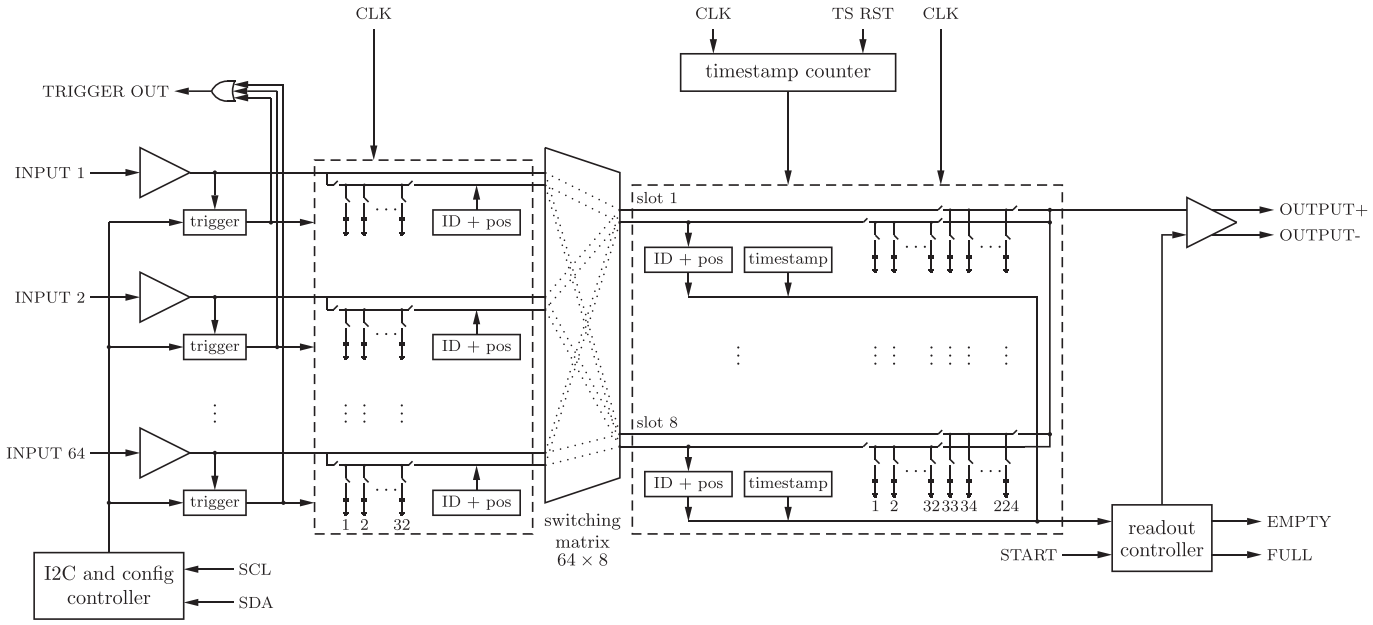

Fig. 5. Simplified block diagram depicting the main components within the analog memory ASIC.

be used to adjust the gain. The inclusion of at least one external component is required for isolation, since preamplifier pulses exhibit a dynamic range of 2.6 V which is already higher than the 1.8 V power supply for the ASIC. A global test input is included for calibration purposes that needs its own external resistor.

In addition, the front and back channels provide pulses with different polarity. In order to support them interchangeably, the amplifier input is biased at one of two global programmable reference voltages that provide the adequate operating point for both possible polarities. This introduces a small quiescent current through the resistors whenever V_{ref} and the preamplifier baseline differ, and thus power consumption in the absence of activity; this current can be eliminated by proper tuning of the supply voltages if desired.

Several trigger modes are available and can be configured individually for each channel. The standard trigger condition is leading edge discrimination, i.e. the detector pulse rising edge crossing a fixed, programmable voltage threshold, as sensed by a comparator. Hysteresis is implemented by inhibiting further triggers until a second comparator detects the pulse signal crossing a lower voltage on its way down, in order to avoid false triggers due to noise on the falling edge. A global trigger request output signal is activated whenever one of the channels is triggered.

Other trigger conditions are provided by four global, external trigger signals, the sensitivity to which can be programmed independently for each channel in order to implement additional functionality such as synchronization, calibration and triggering from the preamplifiers' fast-reset logic. For the first ASIC prototype, a separate external trigger will be included for a few test channels in order to test different shaping and trigger circuitry using discrete components on the test PCB. This feature cannot be implemented for all channels due to the large resulting amount of pins.

3.4. ASIC configuration and readout

The block diagram of the whole analog memory ASIC is outlined in Fig. 5, with simplified depictions of the input stage and SCA channels. An I^2C interface is included for control and configuration. Global configuration registers for reference voltages

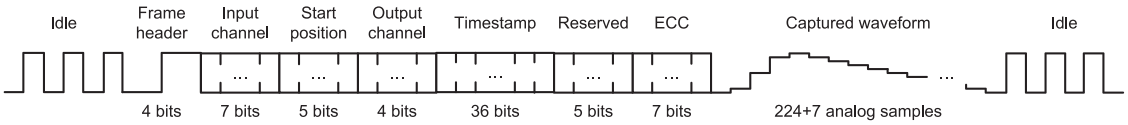

Fig. 6. Event frame format.

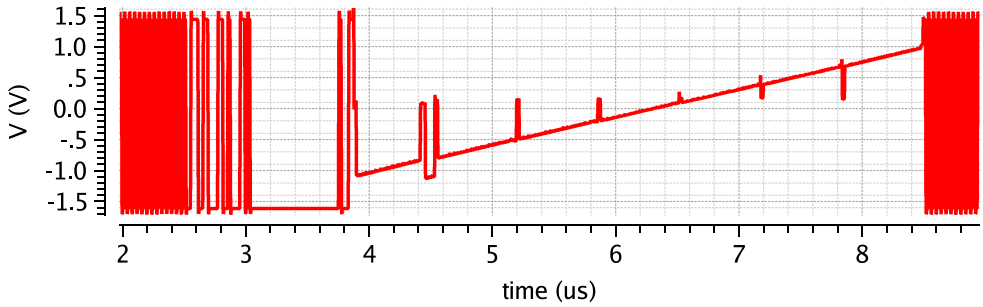

Fig. 7. Simulated waveform of an output frame containing a captured linear ramp waveform. The digital data and analog sample sections are clearly visible between the idle states where a 25 MHz clock is being transmitted. In the analog part, wait cycles are present every 32 samples. In the pre-trigger part, two samples are lost due to the operation of cell precharge circuitry, and the chronological order of the others is shifted; the position of the lost samples and shift value is given by the "start position" field in the frame data.

are present, as well as readable status registers with counters for trigger requests and pulses lost due to full queue. In addition, each input channel contains several local configuration registers including reference voltage selection, sensitivity to triggers, leading edge trigger polarity, and DAC threshold values. Input stages connected to back channels for ToT spectroscopy are configured to be triggered by the external trigger signals provided by the preamplifiers. One channel per ASIC will be devoted to synchronization and configured to be triggered externally by the GTS; the captured timestamp will then be used for alignment with the global GTS timestamp.

Each slot in the output queue contains the SCA channels for sample storage and additional digital registers: for the pulse timestamp, which is immediately latched on trigger, and for identification of the corresponding input SCA channel and sampling cell position at the time of trigger; these two values are transferred serially from the pre-trigger channel after the captured samples.

A dedicated interface is used for the readout of captured events. Readout is timed with a read clock at $f_r = 50$ MHz that is derived from the sampling clock. Event data are output as analog differential signals through an integrated differential amplifier and a line driver external to the ASIC. Data are digitized by an external ADC at the back-end, and include both analog waveform samples and the digital data encoded as analog values.

Event data are organized in the frame format outlined in Fig. 6, that must be decoded by the receiving FPGA after digitization. During idle mode, i.e. when no pulse information being transmitted, an alternating sequence of zeros and ones is output continuously in order to allow the receiver to tune the ADC sampling point as close as possible to the next edge for improved accuracy. A 4-bit header indicates the start of a new event frame. 64 bits of digital data include the timestamp and identification of the queue slot, input channel and cell position where the trigger was issued; these data are enough to completely identify events and their full source and path through the ASIC for calibration correction. In particular, the pulse timestamps must be used to determine whether different pulses belong to the same event, because event reception latency is not deterministic due to the FIFO queue; in any case, they are used for complete event building including data from other detector arrays, e.g. AGATA. A 7-bit Hamming Error-Correcting Code (ECC) is computed by the readout controller and included in the frame that allows correction of single bit errors and detection of double bit errors. Finally, the 224 captured samples are serially transmitted, with 7 wait cycles in between due to the internal organization of the SCAs in 32-cell sections. Complete transmission of a single event takes 5.98 μs.

3.5. Simulation

At the moment, the pre-layout version of the circuit is completely finished and final versions of all blocks of the analog memory ASIC have already been designed. This includes final schematics for all analog and mixed-signal parts including amplifiers, analog switches, storage cells and clock distribution elements, and synthesizable, optimized HDL code for fully digital blocks, i.e. the timestamp counter, input and output channel controllers, readout controller, and I^2C configuration engine.

Distributed, full-custom circuitry has been used as much as possible for digital control of the SCA channels and the switching matrix, in order to reduce the size and complexity of the digital blocks, to limit the impact of control signal routing on area and noise, and to better manage the timing of switch control signals by generating them locally with full-custom circuits. In particular, SCA channel control is based on embedded shift registers with regenerative one-hot encoding of the active cell position, and switching matrix control is based on the propagation of active and full slot flags through input channels, where local trigger signals act on them to activate matrix crosspoints and detect pulses lost to a full output queue.

The complete circuit has been simulated using the final pre-layout circuits for analog and mixed-signal parts and RTL code for digital control blocks. A storage capacitor value $C = 270$ fF has been chosen as a trade-off between noise specifications, slew rate requirements and timing performance. Parasitic capacitances are one of the key factors limiting the performance of the circuit, so the parasitics of interconnections have been estimated and included in the simulations. Simulated performance parameters are not expected to be very accurate, but enough to validate the design. Current simulations predict a signal bandwidth over 60 MHz, non-linearity below 1 mV and noise slightly below 12 ENOB in the worst case (i.e. the pre-trigger samples) on output samples with a dynamic range of ± 1.2 V.

Fig. 7 shows the simulated waveform of an output frame corresponding to the capture of a linear ramp, at the input of the external line driver; the different fields in the frame are visible in the figure.

Assessment of the digital control circuitry has been done in a separate, digital testbench in order to validate the timing performance of their synthesized and mapped and routed versions.

4. Summary and outlook

The conceptual design of the readout scheme for the TRACE detector has been presented, based on two ASICs implementing an array of charge preamplifiers and an analog memory circuit, respectively. In particular, a novel analog memory architecture is proposed wherein the typical SCA structure is split into two pipelined, asymmetric stages and captured data are stored in an analog FIFO queue, dramatically reducing its area requirements and removing readout-related dead time. While both circuits have been designed with the readout of TRACE in mind, they are also meant to be generic enough that they can be employed for other detectors or applications.

Prototypes for the charge preamplifiers are already available and awaiting test, while the analog memory ASIC is currently in the final design stage and samples are expected at the end of 2015. The final pre-layout version of the ASIC has been simulated and the viability of the proposed architecture has been validated. Noise performance close to 12 ENOB is currently being predicted with a power consumption below 10 mW per channel and expected area requirements around 12–15 mm^2 for 64 channels.

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