Nuclear Inst. and Methods in Physics Research, A 936 (2019) 288–289

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

An innovative radiation hardened CAM architecture ☆

O. Anagnostou [a], V. Liberali [b,c], M. Mews [a], S. Shojaii [a,c,*]

[a] The University of Melbourne, Australia
[b] Università degli Studi di Milano, Italy
[c] INFN — Sezione di Milano, Italy

ARTICLE INFO

Keywords:
Radiation hardening
CMOS technology
Integrated circuits

ABSTRACT

An innovative Content Addressable Memory (CAM) cell with radiation hardened (RH) architecture is presented. The RH-CAM is designed using a commercial 28 nm CMOS technology. The circuit has been simulated in worst-case conditions, and the effects due to single particles have been analyzed by injecting a current pulse into a circuit node. The proposed architecture is suitable for real-time pattern recognition tasks in harsh environments, such as front-end electronics in the ATLAS experiment at the Large Hadron Collider (LHC) and in space applications.

Contents

1. Introduction

The "Associative Memory" (AM) chip is an integrated circuit used in the FastTracKer (FTK) system of the ATLAS experiment at CERN. The AM-chip is a large digital chip dedicated to real-time pattern recognition using Content Addressable Memory (CAM) architecture [1]. The last version (AM06) has been designed in 65 nm CMOS [2], and employs a CAM cell called "XORAM", which combines a conventional 6T SRAM with a XOR gate [3]. The FTK system does not operate close to the particle beam, so radiation tolerance is not required, and the AM chip is not radiation hard.

A radiation hardened version of the CAM cell would be suitable for harsh environments, such as space and high-energy physics detectors. Radiation effects can be divided into two main categories: total dose effects, i.e., cumulative effects from long-term exposure, and Single Event Effects (SEE) that are due to the interaction with a single particle. The 28 nm CMOS technology is intrinsically tolerant to total dose effects; however, it is prone to SEE. A single particle can produce a "soft error", which may change the logic value stored in a memory cell, thus causing a Single Event Upset (SEU) which corrupts the information stored. Radiation hardening against SEU is addressed in next sections of the paper.

2. Radiation hardened CAM architecture

To avoid SEU effects in the CAM, we use circuit-level design techniques, which do not require modifications to the fabrication process. Fig. 1 shows the schematic diagram of the new CAM cell. It is composed of two main parts.

Single bit memory cell: The conventional SRAM is replaced by a **Dual Interlocked Storage Cell (DICE)** [4], to increase the tolerance to SEU. The DICE contains duplicated data: nodes D and D1 in Fig. 1 are *'homologous'* nodes, as they have the same logic value (nodes Dn and Dn1 are the homologous pair at the opposite logic value). To change the value of the stored bit, both the homologous nodes must be driven to the same logic value. Let us consider a single event affecting node D1 (at 0). The voltage at node D1 rises, thus switching on the transistor M4 and switching off the transistor M7. The voltage at node Dn decreases, while the node Dn1 is in high impedance and operates as a dynamic memory element. If the DICE is not affected by other single events, it will recover the original state after the transient. Therefore, the DICE withstands the single event and maintains the stored bit [5]. In the layout, the homologous nodes of the DICE have been physically separated, to prevent a SEE from affecting both of them simultaneously (Fig. 2).

* Corresponding author at: The University of Melbourne, Australia.
E-mail address: shojaii@unimelb.edu.au (S. Shojaii).

https://doi.org/10.1016/j.nima.2018.11.054
Received 29 June 2018; Received in revised form 16 October 2018; Accepted 12 November 2018
Available online 6 December 2018
0168-9002/

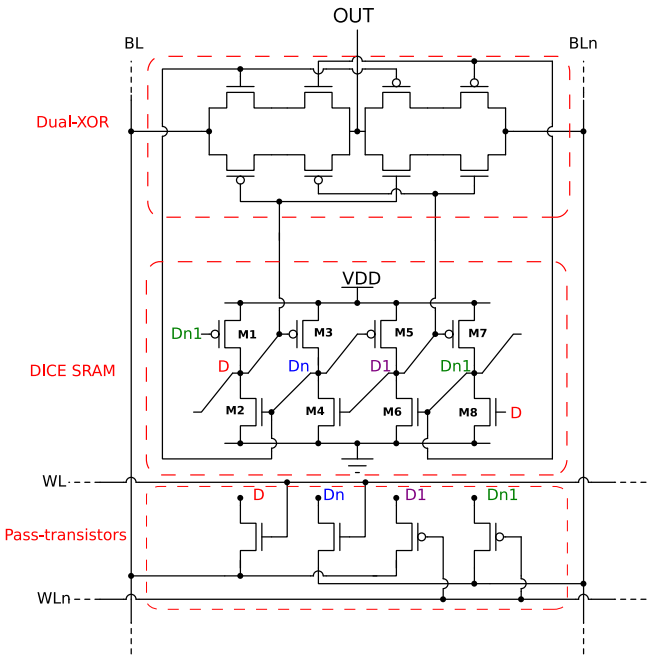

Fig. 1. Schematic of the radiation hardened CAM (RH-CAM).

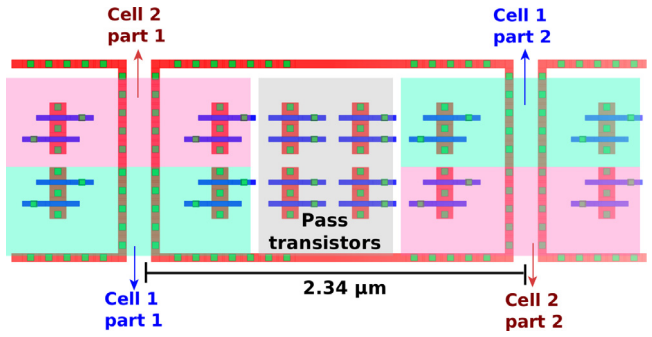

Fig. 2. Layout of the radiation hardened CAM (RH-CAM) in 28 nm CMOS.

Dual-XOR logic: In the original cell, if a particle affects one of the four transistors of the XOR gate, the OUT signal will show an incorrect comparison result. In the proposed cell, the dual-XOR gate compares the input logic value that comes from BL and BLn with both the duplicated bits, and the output goes to 0 only if the input data matches both the homologous bits.

Therefore, any transient effect on the dual-XOR logic and on the DICE SRAM in stand-by is mitigated and does not affect the result.

3. Simulation of single event effects

The tolerance of the DICE against single events decreases when the memory array is accessed for write or read operations. To select one cell for writing or reading, the whole line of the array must be selected (WL = 1), and all the cells belonging to the line become sensitive to SEU.

To avoid spurious writing, all the bit lines are equalized, i.e., they are pre-charged to an intermediate voltage ($V_{DD}/2$). Then the pass transistors are turned on, and bit lines are connected to all the four nodes of the DICE. In this condition, a single event may corrupt the stored bit. If the SEE affects node D1, then the transistor M4 is switched on and the transistor M7 is switched off (as in the previous example). However, the node Dn1 is not in high impedance, because it is connected by the pass transistor to the bit line. The node Dn1 is discharged to $V_{DD}/2$, and also

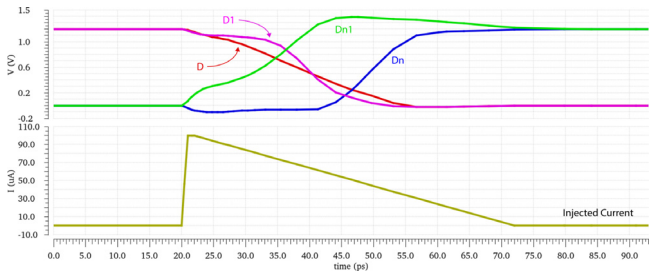

Fig. 3. DICE simulation injecting 100 µA on node D1.

the nodes D and Dn are driven by the pass transistors towards $V_{DD}/2$. If the duration of the single event is long enough, the DICE exhibits a bit-flip.

We can prevent the SEU by increasing the size of transistors, to improve the dynamic memory behavior when nodes are in high impedance. By increasing the capacitance of internal nodes, a larger charge is required for the SEU.

To simulate the effect of an incident particle on sensitive nodes, we perform a circuit simulation with current injection. Let us consider an application where incident particles are protons with energy ranging from 1 MeV to 200 MeV. The linear energy transfer (LET) of protons in silicon ranges from 0.18 MeV·cm^2/mg to 3.6 keV·cm^2/mg. As the average energy required to generate an Electron–Hole Pair (EHP) in silicon is 3.6 eV, the maximum value of the charge generated along the proton track is 1.86 fC/µm (for 1-MeV protons). If a single transistor is affected by the charge generated along 1.5 µm of the proton path, then the charge collected is 2.8 fC. We assume that the charge gives a triangular current pulse, with a duration of $\Delta t = 50$ ps.

The RH-CAM cell (in Fig. 1) has the internal node pair D and D1 set at 0, and the node pair Dn and Dn1 set at 1. A triangular current pulse is injected into the node D1, to simulate a SEE on transistor M6 (Fig. 3, bottom).

From circuit simulations, we have seen that a DICE with minimum size transistors (W = 100 nm, L = 30 nm for PMOS and NMOS transistors) is affected by a single event and exhibits a SEU when WL = 1. By increasing the transistor width to W = 400 nm, the cell does not exhibit a SEU.

4. Conclusion

A novel Radiation Hardened CAM (RH-CAM) architecture is presented. Circuit design techniques are employed to achieve high tolerance to SEE. Simulation results confirm the robustness of the designed cell in stand-by. The SEU tolerance in read/write mode can be increased by increasing the size of transistors.

An array of RH-CAM cells can be used in read-out electronics in extreme applications such as real-time pattern recognition tasks in the ATLAS experiment. It has the advantages of being programmable while operational by changing the stored data which is used for comparison with input data.

References

[1] ATLAS Collaboration, IOP J. Instrum. 3 (2008) S08003.
[2] A. Annovi, et al., IOP J. Instrum. 12 (2017) C04013.
[3] L. Frontini, et al., A new XOR-based Content Addressable Memory architecture, in: Proc. ICECS, Seville, 2012.
[4] T. Calin, et al., IEEE Trans. Nucl. Sci. 43 (1996) 2874.
[5] S. Shojaii, et al., A radiation hardened static RAM for high-energy physics experiments, in: Proc. MIEL, Belgrade, 2014.