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A fast hardware tracker for the ATLAS trigger system

J. Anderson [f], A. Andreani [m,n], A. Andreazza [m,n], A. Annovi [b], M. Atkinson [e], B. Auerbach [f], M. Beretta [b], V. Bevacqua [a,c], R. Blair [f], G. Blazey [q], M. Bogdan [d], A. Boveia [d], F. Canelli [d,j], A. Castegnaro [b], V. Cavaliere [e], F. Cervigni [o,p], P. Chang [e], Y. Cheng [c], M. Citterio [m], F. Crescioli [a,c], M. Dell'Orso [a,c], G. Drake [f], M. Dunford [d], L. Fabbri [o,p], A. Favareto [m,n], M. Franchini [o,l], S. Geer [j], P. Giannetti [a], F. Giannuzzi [o,p], F. Giorgi [o], S. Gruenendahl [j], H.L. Li [d], J. Hoff [j], T. Iizawa [h], A. Kapliy [d], M. Kasten [e], Y.K. Kim [d,j], N. Kimura [h], A. Lanza [k], F. Lasagni [o,p], V. Liberali [m,n], T. Liu [j], D. Magalotti [o,p], A. McCarn [e], C. Melachrinos [d], C. Meroni [m], T. Mitani [h], P. Murat [j], A. Negri [k,l], M. Neubauer [e], Y. Okumura [d,j], J. Olsen [j], B. Penning [d,j], M. Piendibene [a,c], J. Proudfoot [f], C. Roda [a,c], I. Sacco [a,c], Y. Sakurai [h], C. Sbarra [o], M. Shochet [d], A. Stabile [m,n], J. Tang [d], F. Tang [d], L. Tompkins [d], R. Tripiccione [g], J. Tuggle [d], S. Valentinetti [o,p], V. Vercesi [k], M. Verzocchi [j], M. Villa [o,p], G. Volpi [b,d,*], J. Webster [d], K. Yorita [h], J. Zhang [f], A. Zoccoli [o,p,i,r,1]

[a] Sezione di Pisa, INFN, Pisa, Italy
[b] Laboratori Nazionali, INFN, Frascati, Italy
[c] Department of Physics, University, Pisa, Italy
[d] Department of Physics and Enrico Fermi Institute, University, Chicago, IL, USA
[e] Department of Physics, University of Illinois at Urbana-Champaign, Urbana, IL, USA
[f] Argonne National Laboratory, Argonne, IL, USA
[g] Department of Physics, University of Ferrara, Ferrara, Italy
[h] Department of Physics, Waseda University, Waseda, Japan
[i] Department of Physics, University of Harvard, Harvard, MA, USA
[j] Fermi National Accelerator Laboratory, Fermilab, Batavia, IL, USA
[k] Sezione di Pavia, INFN, Pavia, Italy
[l] Department of Physics, University of Pavia, Pavia, Italy
[m] Sezione di Milano INFN, Milan, Italy
[n] Department of Physics, University of Milan, Milan, Italy
[o] Sezione di Bologna INFN, Bologna Italy
[p] Department of Physics, University of Bologna, Bologna, Italy
[q] Northern Illinois University, USA
[r] Department of Physics, University of Perugia, Perugia Italy

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ABSTRACT

The Fast Tracker (FTK) processor is an approved ATLAS upgrade that will reconstruct tracks using the full silicon tracker at Level-1 rate (up to 100 KHz). FTK uses a completely parallel approach to read the silicon tracker information, execute the pattern matching and reconstruct the tracks. This approach, according to detailed simulation results, allows full tracking with nearly offline resolution within an execution time of 100 μs. A central component of the system is the associative memories (AM); these special devices reduce the pattern matching combinatoric problem, providing identification of coarse resolution track candidates. The system consists of a pipeline of several components with the goal to organize and filter the data for the AM, then to reconstruct and filter the final tracks. This document presents an overview of the system and reports the status of the different elements of the system.

1. Introduction

As the Large Hadron Collider (LHC) luminosity is ramped up to 3×10^{34} cm^{-2} s^{-1} and beyond, the high rates, multiplicities, and energies of particles seen by the detectors will pose a unique

* Corresponding author at: Laboratori Nazionali, INFN, Frascati, Italy.
E-mail address: guido.volpi@lnf.infn.it (G. Volpi).

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challenge. The current three-level trigger, designed to allow a rate reduction from 40 MHz to about 400 Hz [1], has to evolve to fit in these constraints. The Fast Tracker (FTK) is an upgrade to the current ATLAS trigger system that will operate at full Level-1 output rates, providing high-quality tracks reconstructed in the entire inner detector by the start of processing in the Level-2 trigger. This frees execution time in the Level-2 farm for more complex selection algorithms, allowing interesting events to be selected with higher efficiency while rejecting uninteresting events. FTK solves the combinatorial challenge inherent to tracking by exploiting the massive parallelism of associative memories that can compare inner detector hits to billions of precalculated patterns simultaneously.

The tracking problem within the matched patterns, referred as roads, is further simplified by transforming the helix parameters and the quality estimator calculations into a set of scalar products in the form

$$p_i = \sum_j C_{ij} x_j + q_i$$

where x_j are the hit coordinates in each detector layer, C_{ij} and q_i are precalculated terms, p_i can be either helix parameters or χ^2 components. Using this transformation fast DSPs in modern commercial FPGAs can perform the calculation in a very efficient and parallel way.

2. FTK architecture

The FTK system will receive a copy of the data from Read-Out Drivers (ROD) of the ATLAS pixel and strip detectors. This functionality was not present in the original HOLA card, responsible for the ROD output; a specific dual-output HOLA card was developed for FTK: it has two independent streams, one for the standard DAQ stream and the second for FTK. All the 270 HOLA cards required to install FTK have been produced and tested. The testing procedure was particularly detailed and important because these cards are used by the general DAQ; indeed a failure will prevent normal ATLAS operations. During the 2012 winter shutdown 32 HOLA cards were installed and included in the normal operations.

The data collected by the HOLAs will be collected by the Data Formatter (DF). The DF organizes the data to be used by the FTK system. It maps the silicon Inner Detector (ID) modules to 64 $\eta-\phi$ independent towers. The DF also organizes the data for use by the remaining boards in the system. In particular, the DF sends to the AM chip the data from 8 out of the 11 layers that a track can cross. The data from the other three layers are sent to the Second Stage Boards (SSB). Technically, the DF boards will be installed in ATCA crates, using a full-mesh backplane. This architecture was chosen because of the data sharing flexibility in ATCA. For the inter-shelf communication an optical fiber will be used.

A special role is played by the input mezzanine card installed in the DF boards: the FTK input mezzanine (FTK_IM). This mezzanine card receives as input the S-link fibers connected to the HOLA cards and runs a clustering algorithm. The clustering algorithm is crucial in the pixel layer to identify the clusters and calculate the centroids; the execution speed is crucial and the selection of the final FPGA is in progress. The SCT data are already clustered by the front-end chip, however for instrumental reasons clusters can be split at chip boundaries; a refinement of SCT clusters will improve system performance.

The data collected by the DF will be sent to the real processing units, composed by the AM board and an auxiliary card (AUX) installed on the VME backplane. Technically the AUX card receives the clusters and converts each to coarse resolution hit for pattern recognition (superstrip or SS). The SS information is routed within the AM board to 128 AMChip04 chips [2] and matched to patterns, about 10 millions per board. The found roads will then be sent back to the AUX where all the full resolution clusters will be retrieved and combined to build candidate tracks with 1 hit per layer. For each candidate a χ^2 is calculated and the bad tracks are rejected. This task is performed in an FPGA with an average fit rate of 1 track per ns.

The good tracks in the AUX cards are sent to SSB and extrapolated. If hits are found around the extrapolated coordinates these are added to the track; if the there are not hits, the track is discarded. This procedure rejects fakes and increases the quality of the tracks. The final tracks are sent to the FLIC (FTK to Level 2 Interface Crate), collected and prepared for the ATLAS HLT processing farm.

3. Expected performance

Using a detailed emulation of the system it has been possible to evaluate the expected performance of the system up to 3×10^{34} cm^{-2} s^{-1}, verifying that FTK is able to compute the helix parameters for all tracks in an event, apply quality cuts in less than 100 μs, with nearly offline quality. This quality allows us to implement selection algorithms based on tracks, like high-p_T lepton identification, b- or τ-tagging of jets. However the integration with the ATLAS HLT will allow other, more sophisticated algorithms [3].

4. Conclusion

The FTK system design was defined and the performance presented. The design of individual boards is in progress. In particular some of the dual output HOLA cards are already installed. Other parts, like the AM board, the AUX card or the FTK_IM are already at prototype level. Prototypes for the rest of the boards are expected soon. The final TDR of the system, where the first test of the prototypes will be included, is expected for the spring 2013. The installation is expected to start in 2014.

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