



A Novel Design of Reversible Multiplier Circuit

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ABSTRACT

Adders and multipliers are two main parts of arithmetic units of computer hardware and play an important role in reversible computations. This paper introduces a novel reversible 4×4 multiplier circuit that is based on an advanced “Partial Product Generation Circuits” (PPGC) with Peres gates only without duplicating gates. Again, an optimized Peres full adder reversible gate is used in “Reversible Parallel Adder” (RPA) part with accompaniment with the carry save adder technique. The comparison of the proposed design with previous ones shows that the proposed reversible multiplier improves the quantum parameters. The proposed design shows lower quantum cost, depth with the help of a novel design in PPGC. The circuit cost of the proposed design is a little higher than the best compared design, but the proposed design shows the lowest total cost which is defined as sum of quantum cost and circuit cost. Moreover, the number of gates, garbage input and output has no change regarding to the best compared design. The proposed multiplier can be generalized as an n×n bit multiplication.

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NOMENCLATURE

ALU	Arithmetic Logic Unit	MKG	Majid Keivan Gate
CC	Circuit Cost	NG	New Gate
CPA	Carry Propagating Adder	NoG	Number of Gates
CSA	Carry Save Adder	O _v	Output Vector
D	Depth	PA	Parallel Adder
DSP	Digital Signal Processor	PFAG	Peres Full Adder Gate
FA	Full Adder	PG	Peres Gate
FG	Feynman Gate	PPGC	Partial Product Generation Circuits
FRG	Fredkin Gate	QC	Quantum Cost
Gin	Garbage Input	RPA	Reversible Parallel Adder
Gout	Garbage Outputs	TC	Total Cost
HA	Half Adder	TG	Toffoli Gate
HNG	Haghparsast Navi Gate	TSG	Thapliyal Srinivas Gate
I _v	Input Vector	VLSI	Very Large Scale Integrated

1. INTRODUCTION

Power dissipation is one of the important parameters in the digital circuit design. A part of this energy loss is due to non-ideality of switches and other technological

factors. Another part according to Landauer's principle in 1961 [1] is due to irreversible logic computations that result in the energy dissipation as data loss. Irreversible circuits dissipate $KT \ln 2$ joules of energy for every bit of information that is lost regardless of their implementation technologies, where $K=1.38 \times 10^{-23}$

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$m^2kg^2k^{-1}$ (Joules Kelvin⁻¹) is the Boltzmann's constant, and T is the absolute temperature at which the computation is performed.

Due to irreversible gates, the power loss is negligible for current logic technologies using adiabatic design. However, it is well known that Moore's law, which states that processing power will double every 18 months, will stop functioning in the years 2010-2020. This particular problem of VLSI designing was realized by Feynman and Bennet in 1970s [2].

In 1973 Bennet [3] showed that energy dissipation problem of VLSI circuits can be circumvented by using reversible logics that will not loose energy during internal calculations (However, energy may be lost for input and output operations). Furthermore, the reversible logics will finally need hardware for the implementation. Quantum gates are inherently reversible [4], so that quantum computation can be considered as a basis for reversible logic implementations.

An introduction on reversible logics and corresponding parameters are presented in the Appendix. Reversible circuits for different purposes e.g. HA (Half Adder), FA (Full Adder) [5-7], multiplier [8-12] have been proposed recently. Among these reversible circuits, multiplier circuits are of special importance because they are widely used in every modern ALU (Arithmetic Logic Unit) of computer system and DSP (Digital Signal Processor). Consequently, optimized multipliers are on demand while designing an arithmetic unit [13].

Several reversible logic gates have been proposed in the literature, including 2×2 Feynman gate (FG) [14], 3×3 Toffoli gate (TG) [15], 3×3 Fredkin gate (FRG) [16], 3x3 Peres gate (PG) [17], 3×3 New gate (NG) [18], 4×4 TSG gate [5], 4×4 MKG gate[6], 4×4 HNG gate[7] and 4×4 PFAG gate [11]. Significant aspect of these universal 4×4 reversible gates is that they can work singly as a reversible FA. Table 1 presents these reversible gates including their quantum implementation, cost and depth.


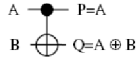

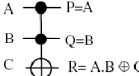

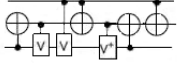

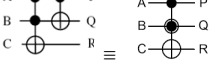

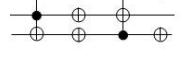

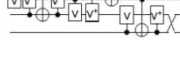

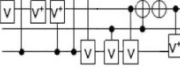

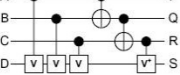

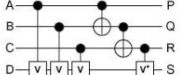
Among these reversible logic gates, several 4×4 reversible gates (e.g. TSG [5], MKG [6], HNG [7] and PFAG [11]) have been used in reversible multiplier designing to construct the FA.

In this paper, a novel reversible 4×4 multiplier is designed which improves the quantum parameters and can be generalized to construct fast reversible n×n bit multipliers. The proposed reversible PPGC (Partial Product Generation Circuits) has minimum quantum cost among all the reversible PPGC designs in reversible multiplier circuits literature.

The related works in reversible multiplier circuit's designs is presented in Section 2. Our proposed reversible multiplier circuit design is described in Section 3. The comparisons and discussion about the

results of the proposed design and the previous ones are described in Sections 4 and 5, and finally Section 6 concludes the paper.

TABLE 1. Reversible gates, their quantum implementation, quantum cost (QC) and depth (D).

Reversible gates	Quantum implementation	QC	D
 $P = A$ $Q = A \oplus B$	 $P=A$ $Q=A \oplus B$	1	1
 $P = A$ $Q = B$ $R = AB \oplus C$	 $P=A$ $Q=B$ $R=A.B \oplus C$	5	2
 $P = A$ $Q = A'B \oplus AC$ $R = A'C \oplus AB$		5	3
 $P = A$ $Q = A \oplus B$ $R = AB \oplus C$		4	2
 $P = A$ $Q = AB \oplus C$ $R = A'C' \oplus B'$		7	3
 $P = A$ $Q = A'C' \oplus B'$ $R = (A'C' \oplus B') \oplus D$ $S = (A'C' \oplus B').D \oplus (AB \oplus C)$		14	5
 $P = A$ $Q = C$ $R = (A'D' \oplus B') \oplus C$ $S = (A'D' \oplus B').C \oplus (AB \oplus D)$		13	5
 $P = A$ $Q = B$ $R = A \oplus B \oplus C$ $S = (A \oplus B).C \oplus AB \oplus D$		6	4
 $P = A$ $Q = A \oplus B$ $R = A \oplus B \oplus C$ $S = (A \oplus B).C \oplus AB \oplus D$		6	4

2. RELATED WORKS

The operation of a 4×4 parallel multiplier is depicted in Figure 1. It can be applied to any other n×n reversible multiplier. The existing parallel multiplier circuits have two important components: The PPGC and multi-operand parallel adder (PA). Reversible multiplier can be designed after planning of these two circuits as a reversible.

The operation of the reversible PPGC consists of 16 partial product bits of form $x_i.y_j$, where $i,j=0, 1, 2, 3$. The parallel adder as shown in Figure 2 uses the FAs and HAs to products final results. Some reversible gates

including TSG, MKG, HNG and PFAG can be used as a reversible FA.

Different designs of parallel reversible multipliers circuits are described in the literature. In the first design that was introduced in 2005, FRGs are used for designing of PPGC part of this circuit and TGs, NGs are used for RPA (Reversible Parallel Adder) designing [8]. Another reversible multiplier circuit that was introduced in 2006 used parallel FRGs as PPGC and TSGs as FAs and HAs in RPA section [9].

Another reversible multiplier circuit was introduced in 2008. The only difference between PPGC of this design with the previous circuits is the use of PGs instead of FRGs (see Figure 3). This circuit uses PGs because they have less logical calculation and less quantum cost than the FRGs [10]. The operation of RPA of this circuit can be planned with MKGs as FAs and HAs [10].

Another reversible multiplier circuit was introduced in 2008. Its only difference with former models is using PG as HA and HNG gate as FA in RPA section of the circuit which results in better circuits than previous ones [7]. Another circuit was suggested in 2009 applied PFAG instead of HNG. This yields in similar results with HNG gate due to its similar quantum implementation [11].

It is to be noted that in reversible logics, fan-out of any gate output is not allowed and every output can be used only once. The 2×2 FG with one "0" input can be used as copying circuits to duplicate the fan-out.

		x_3	x_2	x_1	x_0	
		$\times y_3$	y_2	y_1	y_0	
		x_3y_0	x_2y_0	x_1y_0	x_0y_0	
		x_3y_1	x_2y_1	x_1y_1	x_0y_1	
		x_3y_2	x_2y_2	x_1y_2	x_0y_2	
		x_3y_3	x_2y_3	x_1y_3	x_0y_3	
P_7	P_6	P_5	P_4	P_3	P_2	P_1
						P_0

Figure 1. Operation of a 4×4 multiplication

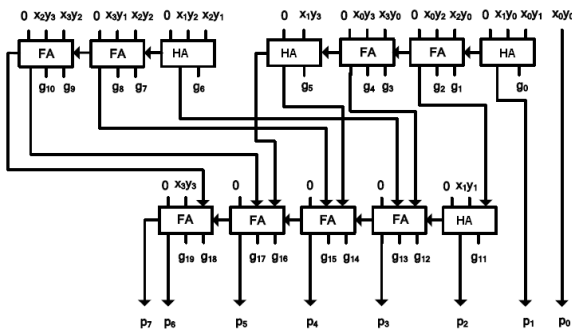


Figure 2. 4×4 reversible multiplier circuit in which output of PPGC are input of parallel adder

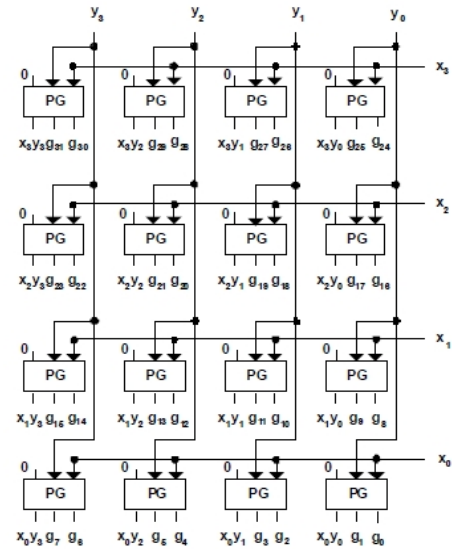


Figure 3. Reversible PPGC using 16 Peres gates

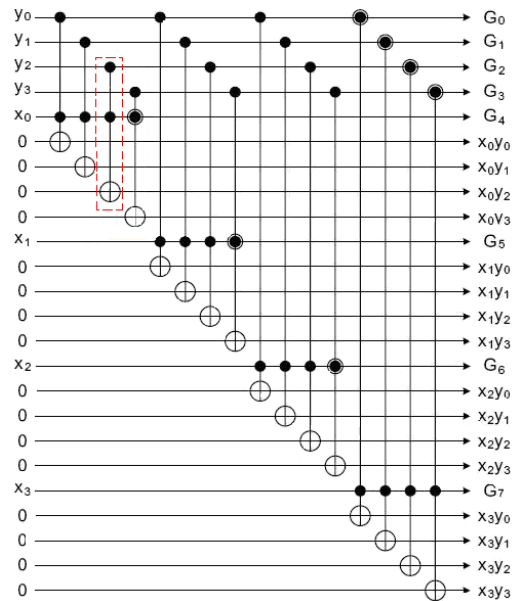


Figure 4. Reversible PPGC with TGs and PGs

The duplicating gates in the previous designs [7-11] are one the most disadvantages which degrades the quantum parameters. In order to remove these duplicating gates, the other suggested circuits in 2009 have different design in PPGC part, as shown in Figure 4. Using of TGs and PGs for generating of partial products, have better results in numbers of garbage outputs, constant inputs and reversible gates than the previous designs [12]. There are two designs in RPA part of this circuit. The first design uses an optimized HNG FA as reversible FA and the second approach uses PFAG (Peres Full Adder Gate). In addition, they need four reversible HAs that they use PG as reversible HA.

3. THE PROPOSED MULTIPLIER CIRCUIT

As mentioned before, a reversible 4×4 multiplier circuit has two important parts: PPGC and then RPA. The purpose of this paper is the design of reversible multiplier circuits with the aim of improving the quantum parameters without losing its efficiency.

3.1. PPGC Implementation of the PPGC of the proposed reversible multiplier circuit is based on the PPGC described in [12]. Since the Peres gate (PG) quantum cost is less than Toffoli gate (TG), therefore we replace TGs with PGs. One sample of replacing TG with PG is shown by the dashed rectangle in Figure 4. Applying PGs instead of TGs (see Figure 5) results in the proposed PPGC uses only PGs as shown in Figure 6.

There is an intrinsic advantage of this circuit over others. As it is made up of same gates, it is easy to implement. Again, PGs have less QC than the TGs (see Table 1). Thus, we have found that proposed PPGC block with lowest QC can be achieved through PGs.

3.2. RPA Circuit The basic cell in a reversible multiplier is a reversible FA which accepting three bits and one constant input. We use Peres FA gate (PFAG) [11] as a reversible FA that is shown in Figure 7. The PFAG can be implemented by two complex 4×4 reversible Peres gate as shown in Figure 8. Because of its complex functionality, it seems the PFAG has a large QC of 8. But, the suggested quantum implementation of the PFAG in 2009 [19] proved that it has QC of 6 and circuit depth of 4. As a result, its quantum cost is lower than other reversible FAs are available in the literature and has the minimum QC reported for FA (see Figure 9). In order to decrease the circuit depth, the CSA (Carry Save Adder) technique can be used in implementing of the RPAs [20] of the proposed multiplier. As shown in Figure 1, in the reversible 4×4 multiplier, four operands must be added to produce the final product. We use the CSA tree to reduce the four operands to two. Thereafter, the CPA (Carry Propagating Adder) adds these two operands and produces the final 8-bit product (see Figure 10). However, this implementation leads the designer to take less depth than prior designs. Finally, we apply the reversible PFAG as a FA and PG as a HA to implement this part as shown in Figure 11. In this figure, the shaded blocks indicate the critical path of this circuit.

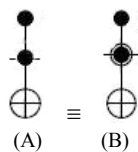


Figure 5. Using the Peres gate instead of the Toffoli gate. (A) TG, (B) PG

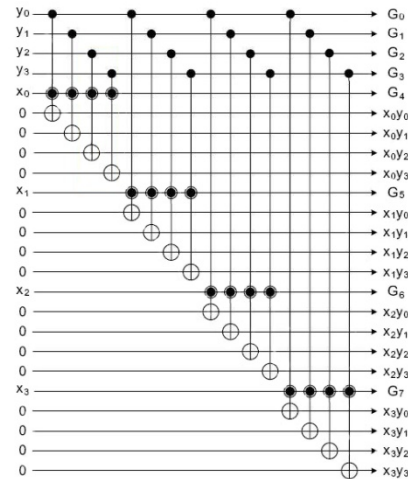


Figure 6. The proposed reversible PPGC with only PGs

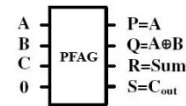


Figure 7. Reversible PFAG as a reversible FA

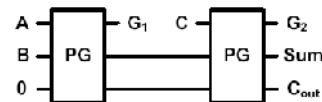


Figure 8. Implementation of PFAG using Peres gates

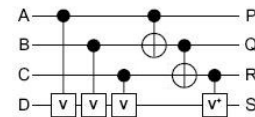


Figure 9. Quantum implementation of PFAG

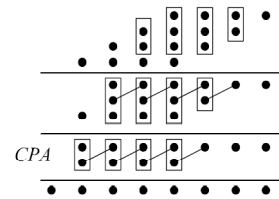


Figure 10. Four-operand Addition (Dot notation) [20]

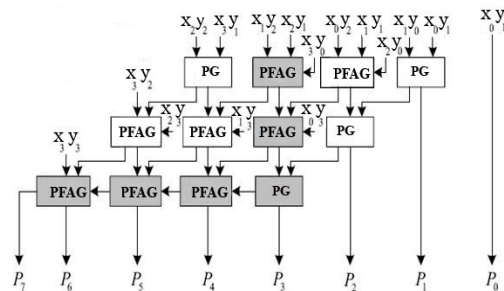


Figure 11. The proposed RPA circuit using PFAG

4. QUANTUM PARAMETERS OF DIFFERENT DESIGNS

Some quantum parameters of the proposed multiplier as well as some other ones [8-12] are calculated in this section. As mentioned before, in reversible logics, fan-out of any gate output is not allowed and every output can be used only once. Therefore, FGs should be used for duplicating each bit of the operands in reversible PPGC in [7-11]. It is to be noted that PPGC proposed in [12] used 12 FGs for duplicating gates but that design approach did not pay enough consideration to numbers of FGs. Actually, all conclusions of that paper was wrong because of those errors. Another design was suggested in 2010 [21] rebuild PPGC with 16FGs instead of 12 FGs (see Figure 12).

Here we use correct approach [21] and believe that for duplicating fan-out, 16 FGs is necessary which increases the quantum parameters. Since the quantum cost and depth of 2x2 FG is one, the number of gates, circuit cost and number of constant inputs, quantum cost and depth in [7-12] should be added with 16 FG, because of its PPGC part.

4.1. Number of Gates One of the major constraints in designing a reversible logic circuit is the number of reversible gates. For an arbitrary circuit C with K gates g_1, g_2, \dots, g_k , the number of gates metric is defined as $NoG=k$ [22]. The NoG of the compared designs are shown in Table 2.

4.2. Garbage Output Garbage output (Gout) refers to the output of the reversible gate that is not used as a primary output or as input to other gates. The garbage outputs of the compared designs are shown in Table 3.

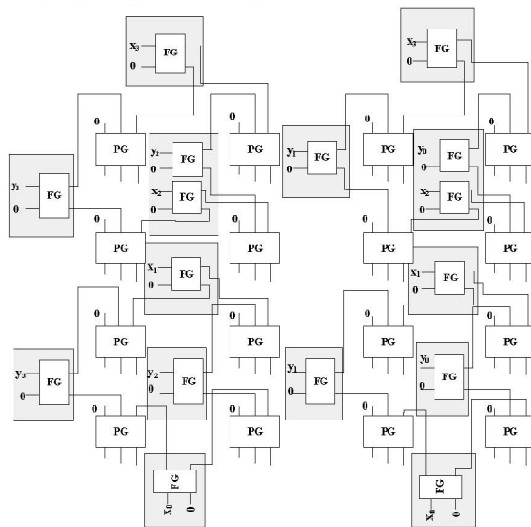


Figure 12. The proposed reversible PPGC using PGs and FGs [21]

4.3. Quantum Cost and Total Cost Quantum cost (QC) is one of the other main factors in designing a reversible logic circuit. Again, in order to consider the effects of garbage output and number of gate as the accompaniment to quantum cost, the total cost (TC) of a circuit is defined as sum of number of gate, garbage outputs and quantum cost [19]. The quantum costs and total costs of the compared designs are shown in Table 4.

TABLE 2. Comparison of number of gates (NoG) of the proposed circuit with the compared circuits

Reversible multiplier	Calculations	NoG
The proposed design	$16(PG)+8(PFAG)+4(PG)$	28
Reference [12] (second design)	$(9TG+7PG)+8PFAG+4PG$	28
Reference [12] (first design)	$(9TG+7PG)+8HNG+4PG$	28
Reference [11]	$(16PG+16FG)+8PFAG+4PG$	44
Reference [7]	$(16PG+16FG)+8HNG+4PG$	44
Reference [10]	$(16PG+16FG)+12MKG$	44
Reference [9]	$(16FRG+16FG)+13TSG$	45
Reference [8]	$(16FRG+16FG)+12NG+12TG$	56

TABLE 3. Comparison of garbage outputs (Gout) of the proposed circuit with the compared circuits

Reversible multiplier	Gout
The proposed design	28
Reference [12] (second design)	28
Reference [12] (first design)	28
Reference [11]	52
Reference [7]	52
Reference [10]	56
Reference [9]	58
Reference [8]	56

TABLE 4. Comparison of quantum costs (QC) and total costs (TC) of the proposed circuit with the compared circuits

Reversible multiplier	Calculations	QC	TC
The proposed design	$(16 \times 4)(\text{for PG})+(8 \times 6)(\text{for PFAG})+(4 \times 4)$	128	184
Reference [12] (second design)	$(9 \times 5)(\text{for TG})+(16 \times 1)+(11 \times 4)(\text{for PG})+(8 \times 8)(\text{for PFAG})$	153	209
Reference [12] (first design)	$(9 \times 5)(\text{for TG})+(16 \times 1)+(11 \times 4)(\text{for PG})+(8 \times 6)(\text{for HNG})$	137	193
Reference [11]	$(16 \times 5)+(16 \times 1)+(4 \times 4)+(8 \times 8)$	160	256
Reference [7]	$(16 \times 5)+(16 \times 1)+(4 \times 4)+(8 \times 8)$	160	256
Reference [10]	$(16 \times 4)+(16 \times 1)+(12 \times 13)$	236	336
Reference [9]	$(16 \times 5)+(16 \times 1)+(13 \times 14)$	278	381
Reference [8]	$(16 \times 5)+(16 \times 1)+(12 \times 7)+(12 \times 5)$	220	332

4. 4. Circuit Depth Depth of circuits (D) is one of the other main factors in designing a reversible logic circuit. The circuit depths of the compared designs are shown in Table 5.

4. 5. Constant Garbage Input Number of constant garbage inputs (Gin) is one of the other main factors in designing a reversible logic circuit. For the compared designs, Garbage inputs are shown in Table 6.

4. 6. Circuit Cost One of the factors of hardware complexity of reversible circuits is the numbers of XOR, AND, NOT logic in the output expressions which are defined as:

- a = calculation of a two input XOR gate.
- b = calculation of a two input AND gate.
- d = calculation of a NOT gate.

The circuit costs (CC) (sometimes called total logic calculations or complexity) of the compared designs are shown in Table 7.

TABLE 5. Comparison of depths (D) of the proposed circuit with the compared circuits

Reversible multiplier	Calculations	D
The proposed design	2(for PG)+(4+4)(for PFAGs) +2(for PG)+(4+4+4)(for PFAGs)	24
Reference [12] (second design)	2(for TG and PG) + 2(for PG) + (4×4) + (2×4)	28
Reference [12] (first design)	2(for TG and PG) + 2(for PG) + (4×4) + (2×4)	28
Reference [11]	2(for FG)+2(for PG)+ 2(for PG)+(2×4)+(4×4)(for PFAG)	30
Reference [7]	2(for FG)+2(for PG)+ 2(for PG) +(2×4)+(4×4)(for HNG)	30
Reference [10]	2(for FG)+2(for PG)+(7×5) (for MKG)	39
Reference [9]	2(for FG)+5(for FRG) +(7×5)(for TSG)	42
Reference [8]	2(for FG)+5(for FRG) +7(3+2)(for TG and NG)	42

TABLE 6. Comparison of garbage inputs (Gin) of the proposed circuit with the compared circuits

Reversible multiplier	Gin
The proposed design	28
Reference [12] (second design)	28
Reference [12] (first design)	28
Reference [11]	28+16=44
Reference [7]	28+16=44
Reference [10]	32+16=48
Reference [9]	34+16=50
Reference [8]	31+16=47

TABLE 7. Comparison of circuit cost (CC) of the proposed circuit with the compared circuits

Reversible multiplier	Logic Calculations	CC
The proposed design	16×(2a+1b)(for PG)+ 8×(5a+2b)(for PFAG) + 4×(2a+1b)(for PG)	80a+36b
Reference [12] (second design)	9×(1a+1b)(for TG)+ 7×(2a+1b)(for PG)+ 8×(5a+2b)(for PFAG)+ 4×(2a+1b)(for PG)	71a+36b
Reference [12] (first design)	9×(1a+1b)(for TG)+ 7×(2a+1b)(for PG)+ 8×(5a+2b)(for HNG)+ 4×(2a+1b)(for PG)	71a+36b
Reference [11]	(80+16)a+36b	96a+36b
Reference [7]	(80+16)a+36b	96a+36b
Reference [10]	(92+16)a+52b+36d	108a+52b+36d
Reference [9]	(110+16)a+103b+71d	126a+103b+71d
Reference [8]	(80+16)a+100b+68d	96a+100b+68d

5. DISCUSSION

The quantum parameters of the different multiplier circuits are shown in Table 8. Regarding to the previous multiplier circuits in [7-12], all quantum parameters of the proposed design is improved. However, in term of the number of reversible logic gates, garbage output and input, the proposed multiplier shows the same value as the multiplier circuit in [12].

In term of quantum cost and depth, our proposed circuit is the best, because using the CSA in RPA part, and replacing the Toffoli gates with Peres gates in PPGC part of the original circuit [12]. On the other hand, the circuit cost of the proposed circuit is slightly worse than the reference [12], but in the same time, the total cost of the proposed circuit is the best.

6. CONCLUSION

Reversible logic circuits are of particular interest in low power CMOS design, optical computing, DNA computing, bioinformatics, quantum computing and nanotechnology. Multiplier is a basic arithmetic cell in computer arithmetic units. Furthermore, reversible implementation of this unit is necessary for quantum computers. Targeting this purpose, various designs can be found in the literature.

This paper introduces a novel 4×4 reversible multiplier circuit. The advanced design based on the same gates (PGs only) that it is easy to implement. In addition, with using PGs in PPGC part improves the quantum cost of the proposed design without needing to any duplicating gates. Furthermore, using CSA technique in RPA part reduces the circuit depth of the proposed design.

TABLE 8. Comparison of the different reversible multiplier circuits (a,b and c: number of XOR, AND, and NOT gates respectively, CC:Circuit Cost, NoG:Number of Gate, Gout:Garbage output, Gin:Garbage input, QC:Quantum Cost, TC:Total Cost, D:Depth)

Reversible multiplier	CC	NoG	Gout	Gin	QC	TC	D
The proposed design	80a+36b	28	28	28	128	184	24
Reference [12] (second design)	71a+36b	28	28	28	153	209	28
Reference [12] (first design)	71a+36b	28	28	28	137	193	28
Reference [11]	96a+36b	44	52	44	160	256	30
Reference [7]	96a+36b	44	52	44	160	256	30
Reference [10]	108a+52b+36d	44	56	48	236	336	39
Reference [9]	126a+103b+71d	45	58	50	278	381	42
Reference [8]	96a+100b+68d	56	56	47	220	332	42

Regarding to the best previous design, the proposed reversible multiplier decreases the quantum cost, total cost and depth, without increasing in the number of gate, number of garbage input and outputs. However, the circuit cost is increased slightly regarding to the best previous design.

As future works, some other reversible implementation of more complex arithmetic circuits such as function evaluations and multiplicative division circuits can be investigated using the proposed multiplier.

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APPENDIX

An introduction to reversible logics and corresponding quantum parameters are presented in this appendix.

1. Introduction to Reversible Logics

A reversible logic circuit comprises reversible gates. A gate that implements one to one mapping between n inputs and n outputs is called an $n \times n$ reversible logic gate that can be represented as:

$$\begin{aligned} I_V &= (x_1, x_2, \dots, x_n) \\ O_V &= (y_1, y_2, \dots, y_n) \end{aligned} \quad (1)$$

where I_V and O_V are the input and output vector.

The reversible logic gate must have the same number of inputs and outputs, and for each input pattern there must be a unique output pattern [3]. Reversible logic circuits avoid energy loss by "uncomputing" the computed information using recycling the energy in the system [3].

Synthesis of the quantum or reversible logic circuits in compared to synthesis of the traditional irreversible

logic circuits has two restrictions that should be mentioned [23]:

- In the reversible logic, fan-out of any gate output is not allowed.
- Several authors assume that there should be no loops of gates and we followed this assumption in this paper.

Due to these restrictions, synthesis of the reversible circuits can be carried out from the inputs towards the outputs and vice versa [22]; so, there is a one-to-one mapping between input and output vector. In an n -output reversible gate, the output vectors are permutations of the numbers 0 to $2^n - 1$.

2. Parameters of Reversible Circuits

There are some important parameters in designing an efficient reversible logic circuits including: the number of gates (NoG), quantum cost (QC), number of garbage outputs (Gout), number of constant garbage inputs (Gin), circuit cost (CC) (which is sometimes called the total logic calculations or hardware complexity) and depth of reversible circuits (D).

The number of gates has been used to evaluate nearly in all synthesis approaches so far. The quantum cost of a reversible circuit is the number of (1×1) or (2×2) reversible gates used to implement the circuit. These elementary quantum gates with quantum cost equal to one is defined as follows [4]:

- Inverter (NOT): A single qubit (basic unit of information in quantum computer) is inverted.
- Controlled - NOT (CNOT): The target qubit is inverted if the control qubit is 1.
- Controlled - V: Performs the V operation known as the square root of NOT, since two consecutive V operations are equivalent to an inversion.
- Controlled - V^+ : Performs the inverse of V.

The circuit depth is defined as the number of steps required to execute all available gates in a circuit [24]. The garbage outputs must be added as necessary so that the output patterns are distinct, and it is not used for further computations. Of course, the constant garbage inputs must be added, as necessary, to balance the number of inputs and outputs [25]. Reduction of these quantum parameters is the bulk of the work in reversible circuits design.

A Novel Design of Reversible Multiplier Circuit

TEACHNICAL
NOTE

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جمع کننده‌ها و ضرب کننده‌ها، دو بخش اصلی واحدهای محاسباتی سخت‌افزار کامپیوتر محسوب شده و نقش عمده ای در محاسبات برگشت پذیر ایفا می کنند. این مقاله، مدار ضرب کننده برگشت پذیر 4×4 نوبنی را معرفی می‌کند که در طراحی مدار مولد حاصلضرب های جزئی، تنها از دریچه های پرس استفاده کرده است و نیازی به دریچه های کپی ندارد. در ضرب کننده پیشنهادی، از دروازه برگشت پذیر تمام جمع کننده پرس بهینه شده، به همراه روش جمع با ذخیره نقلی، در قسمت جمع کننده موازی استفاده شده است. مقایسه ضرب کننده برگشت پذیر پیشنهادی با دیگر طرح‌ها نشان می‌دهد که پارامترهای کوانتومی بهبود یافته است. طرح پیشنهادی، کمترین مقدار هزینه کوانتومی و عمق را به کمک طراحی نوبنی در قسمت مدار مولد حاصلضرب‌های جزئی نشان می‌دهد. هزینه مداری طرح پیشنهادی به نسبت بهترین طرح مورد مقایسه اندکی افزایش یافته، اما از نقطه نظر هزینه کل که به صورت مجموع هزینه کوانتومی و هزینه مداری تعریف می‌شود، کمترین مقدار را نشان می‌دهد. علاوه بر این، در طرح پیشنهادی، تعداد دریچه، خروجی اضافه و ورودی اضافه، نسبت به بهترین طرح مورد مقایسه، افزایش نیافته است. ضرب کننده پیشنهادی، برای یک ضرب کننده $n \times n$ قابل توسعه است.

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