UNIVERSITÀ
DEGLI STUDI
DI MILANO

Dottorato di Ricerca in Informatica

PhD dissertation in Computer Science

Integrated Circuits for High Energy Physics Experiments

Author:
Seyed Ruhollah SHOJAII
Supervisor:
Prof. Valentino LIBERALI
Co-supervisor:
Dr. Alberto STABILE

A.A. 2015/2016

Thank you professor Valentino and dear Alberto.

CONTENTS

1. Introduction 9

2. Radiation Effects 13
2.1 Interaction between Radiation and Silicon 13
2.1.1 Ionization 13
2.1.2 Displacement 16
2.2 Radiation Effects on ICs 18
2.2.1 TID Effects and Hardening 19
2.2.2 Single Event Effects 22
2.2.3 Single Event Effect and Hardening: 23
2.2.4 Latch-up 25

3. Radiation Environment 29
3.1 Space 29
3.1.1 Energetic Plasma 30
3.1.2 Trapped Electrons 30
3.1.3 Trapped Protons 31
3.1.4 Solar Energetic Particles 32
3.2 High Energy Physics Experiments 33
3.2.1 Hadron Collider Radiation Environment Radiation Issues 35
3.2.2 HL-LHC Upgrade and RD53 36

4. Radiation Hardened SRAM 39
4.1 Radiation Hardened SRAM Architecture 39
4.1.1 DICE SRAM 41
4.1.2 Memory Array 42
4.1.3 Decoders 42
4.1.4 Equalizer 44
4.1.5 Sense amplifier 45
4.1.6 How SRAM Block Works 46

4.2 Radiation Hardened SRAM Layout 47
4.2.1 Euler Graph 49
4.2.2 Single Memory Cell Layout: First Version 50
4.2.3 Single Memory Cell Layout: second version 50
4.2.4 Single Memory Cell Layout: third version 52
4.2.5 Word-line decoder 52
4.2.6 Bit-line Decoder 53
4.2.7 Wire and Read Circuits 56
4.3 Chip Prototype 57

5. Modeling and Simulations 63
5.1 Parasitic Extraction and Simulation 63
5.2 Total Dose Effect Simulation 64
5.3 Single Event Effect simulation 69
5.3.1 FISAR approach 69
5.3.2 Calculation of charge collected within each box 73
5.3.3 FISAR Simulation Procedure 75
5.3.4 FISAR simulation results 76

6. Characterization 79
6.1 Test Set-up 79
6.2 VHDL architecture 81

7. Fast Tracker Trigger System 85
7.1 ATLAS and Triggering system 85
7.2 Fast TracKer Trigger System 85
7.3 New Content Addressable Memory 87
7.3.1 Conventional CAM cells 88
7.3.2 The new XORAM cell 89
7.3.3 The 18-bit Word CAM 90
7.3.4 Simulation Results 91

8. Conclusion and Results 95
8.1 Radiation Hard SRAM 95
8.2 Dual-rail Logic 97
8.3 Fast Tracker Trigger 98
8.4 Published Papers And Presentations 98

Bibliography 100

1. INTRODUCTION

Integrated Circuits are used in most people's lives in the modern societies. An important branch of research and technology is focused on Integrated Circuit (IC) design, fabrication, and their efficient applications; moreover most of these activities are about commercial productions with applications in ambient environment. However the ICs play very important role in very advance research fields, as Astronomy or High Energy Physics experiments, with absolutely extreme environments which require very interdisciplinary research orientations and innovative solutions.

For example, the Fast TracKer (FTK) electronic system, which is an important part of triggering system in ATLAS experiment at European Organization for Nuclear Research (CERN), in every second of experiment selects 200 interesting events among 40 millions of total events due to collision of accelerated protons. The FTK function is based on ICs which work as Content Addressable Memory (CAM). A CAM compares the income data with stored data and gives the addresses of matching data as an output. The amount of calculation in FTK system is out of capacity of commercial ICs even in very advanced technologies, therefore the development of innovative ICs is required. The high power consumption due to huge amount of calculation was an important limitation which is overcome by an innovative architecture of CAM in this dissertation.

The environment of ICs application in astrophysics and High Energy Physics experiments is different from commercial ICs environment because of high amount of radiation. This fact started to get seriously attention after the first "Telstar I" satellite failure because of electronic damages due to radiation effects in space, and opened a new field of research mostly about radiation hard electronics.

The multidisciplinary research in radiation hard electronic field is about radiation effects on semiconductors and ICs, deep understanding about the radiation in the extreme environments, finding alternative solutions to increase the radiation tolerance of electronic components, and development of new

simulation method and test techniques.

Chapter 2 of this dissertation is about the radiation effects on Silicon and ICs. Moreover, In this chapter, the terminologies of radiation effects on ICs are explained. In chapter 3, the space and high energy physics experiments environments, which are two main branches of radiation hard electronics research, are studied.

The radiation tolerance in on-chip circuits is achieving by two kinds of methodology: Radiation Hardening By Process (RHBP) and Radiation Hardening By Design (RHBD).

RHBP is achieved by changing the conventional fabrication process of commercial ICs [1], [2], [3]. RHBP is very expensive so it is out of budget for academic research, and in most cases it is exclusive for military application, with very restricted rules which make the access of non-military organizations impossible.

RHBD with conventional process is the approach of radiation hard IC design in this dissertation. RHBD at hardware level can be achieved in different ways:

- **System level RHBD:** radiation hardening at system level is achieved by algorithms which are able to extract correct data using redundant information.

- **Architecture level RHBD:** some hardware architectures are able to prevent of lost data or mitigate the radiation effects on stored data without interfacing of software. Error Correction Code (ECC) circuits and Dual Interlocked storage CEll (DICE) architecture are two examples of RHBD at architecture level.

- **Circuit level RHBD:** at circuit level, some structures are avoided or significantly reduced. For example, feedback loops with high gain are very sensitive to radiation effects.

- **Layout level RHBD:** there are also different solutions in layout design level to increase the radiation tolerance of circuits. Specific shapes of transistor design, optimization of the physical distance between redundant data and efficient polarization of substrate are some techniques commonly used to increase significantly the radiation tolerance of ICs.

An innovative radiation hard Static Random Access Memory (SRAM), designed in three versions, is presented in chapter 4. The radiation hardening

is achieved by RHBD approach simultaneously at architecture, circuit and layout levels. Complementary Metal-Oxide-Semiconductor (CMOS) 65 nm is the technology of design and the prototype chip is fabricated at Taiwan Semiconductor Manufacturing Company (TSMC).

Chapter 5 is about the development of simulation models that can help to predict the radiation effect in the behavior of SRAM block.

The setup system developed to characterize the radiation hard SRAM prototype chip is presented in Chapter 5. The setup system gives the possibility of testing the prototype exposed under radiation in a vacuum chamber and regular laboratory environment.

Chapter 6 is about the contribution of this dissertation on FTK project and the conclusion of all research activities is shown in the final part of this dissertation.

The research activities of this dissertation in supported by Italian National Institute for Nuclear Physics (INFN) as part of CHIPIX65 project and RD53 collaboration at CERN.

2. RADIATION EFFECTS

In this chapter after a brief introduction about the phenomena of radiation effects on the silicon material, the effects of radiation on integrated circuits which has the silicon as primitive material are discussed. Furthermore the standard categories of radiation effects on electronics components are explored and explained. These informations are needed for better understanding of next chapters of the dissertation.

2.1 Interaction between Radiation and Silicon

The interaction between particles with semiconductors is divided into two main categories of phenomena: *ionization* and *displacement.*

When particles pass through semiconductors the *Coulomb interaction*, they can ionize the semiconductor material. The **ionization** phenomena generates free carriers which can drift and diffuse. Somehow it may happen that carriers remain trapped in lattice defects of semiconductor and create a permanent charge which affects the density of carriers.

Mechanical interaction may also happen when particles pass through semiconductor material, causing the **displacement** of atoms from their original position.

2.1.1 Ionization

Ionization of a target of material is caused by the interaction of high-energy photons or charged particles with atoms of the material in different way:

- **Photons** interact with semiconductor material through three different processes: photoelectric effect, Compton effect, pair production (Figure 2.1) [4].
- **Neutrons** are neutral particles which interact with semiconductor materials in two ways:

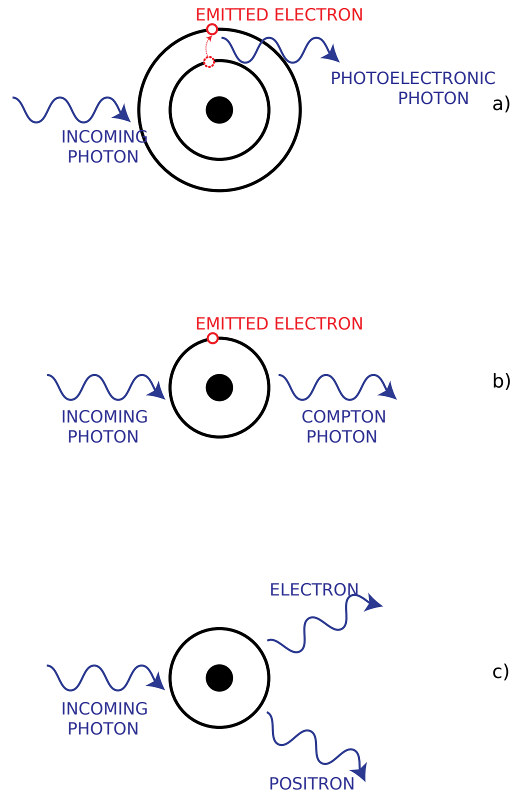

Fig. 2.1: (a) Photoelectric effect; (b) Compton effect; (c) Pair Production.

  - nuclear reaction by absorbing with nucleus and emitting secondary particles;
  - anelastic collisions cause the emitting of γ rays by excitation of nucleus.

- **Protons and Electrons** are charged particles and ionization can be induced by means of Coulomb interaction.

- **Heavy Ions** are charged particles with a high atomic number and ionization can be induced by means of Coulomb Interaction.

However, protons and heavy ions produce higher quantity of ionization due to nuclear interaction. Results of all these processes is the creation of energetic secondary electrons that pass through the material and generate electron-hole

pairs. The density of these electron-hole pairs is proportional to the energy transferred from incident particle to the target material. The transferred energy is measured with Linear Energy Transfer (LET), which is defined as the particle energy loss per unit length. LET is function of particle mass and energy as well as the target material density:

$$LET = \frac{dE}{\rho \cdot dx} \qquad \left[\mathrm{MeV} \cdot \frac{\mathrm{cm}^2}{\mathrm{mg}}\right] \tag{2.1}$$

where ρ is the density of the target material, and $\frac{dE}{dx}$ indicates the average energy transferred into the target material per length unit along the particle trajectory. To estimate the number C_{num} of electron and hole pares generated, it is necessary to integrate the LET coefficient on the path of semiconductor:

$$E_{totlost} = \int \frac{dE}{\rho \cdot dx}\, dx \qquad \left[\mathrm{MeV} \cdot \frac{\mathrm{cm}^3}{\mathrm{mg}}\right] \tag{2.2}$$

and to divide $E_{totlost}$ by E_m, which is the experimental average energy necessary to create one HEP, and is equal to:

- in silicon: $E_m = 3.6\,\mathrm{eV}$
- in oxide (SiO_2): $E_m = 17\,\mathrm{eV}$

$$C_{num} = \frac{E_{totlost}}{E_m} \tag{2.3}$$

From the number of Hole-Electron Pairs (HEP) generated, it is possible to calculate the total charge deposited. For instance, in silicon, a LET of $97\,\mathrm{MeV\,cm^2/mg}$ corresponds to a charge deposited of $1\,\mathrm{pC/\mu m}$. All these assumptions are valid for short paths and space applications [5], [6].

Figure 2.2 shows a plot of LET for electrons and protons. The LET for protons is higher than electrons at lower energy and decreases rapidly by increasing of proton energy. Electrons have a non-monotonic response, LET decreases with increasing of electrons energy before 1 MeV but after start to increase [4].

The total energy deposited by a particle is called **Total Ionizing Dose** (TID). The TID unit in SI is the **gray** (Gy): 1 Gy = 1 J/kg. However the **rad** (Radiation Aabsorbed Dose) is the conventional unit in space industry and it is equivalent to 100 erg/g (1 rad = 0.01 Gy).

The initial deposition of energy with ionizing radiation leads to ionizing defects on metal-oxide-semiconductor structure with two physical processes:

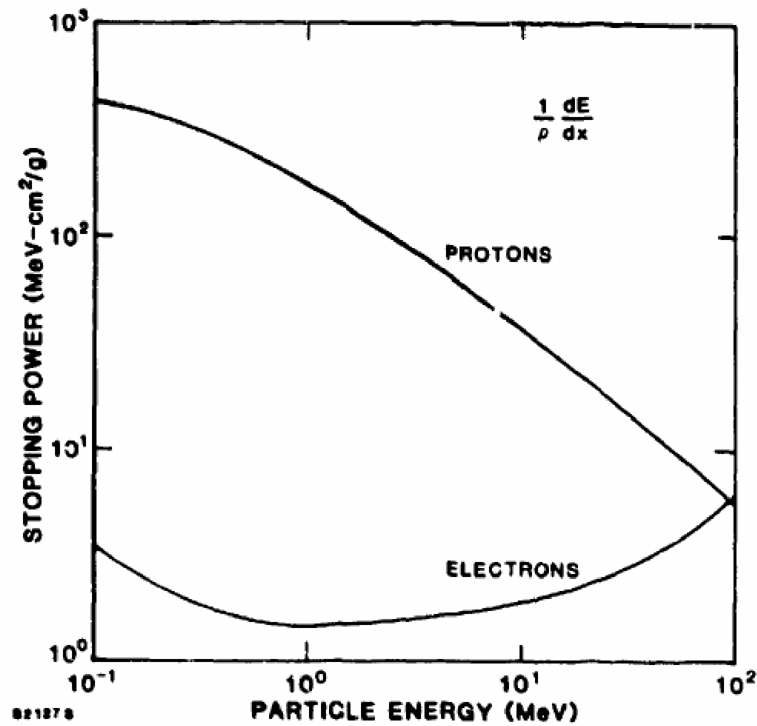

Fig. 2.2: Stopping power versus particle energy for electrons and protons incident of silicon (from [4]).

1. formation of trapped charge via hole trapping in defect precursor sites;
2. formation of interface traps via reactions mostly involving hydrogen.

These processes are summarized in Figure 2.3 [7].

2.1.2 Displacement

Highly energized particles can damage semiconductor materials by displacing atoms. If the energy transferred from the particle to the silicon is greater than 20 eV, the particle can displace an atom. Displaced atom can also displace other atoms of semiconductor crystal. For example a neutron at 1 MeV transfers 70 keV to a silicon lattice atom, which displaces approximately 100 other atoms over a length of 100 nm (Figure 2.4).

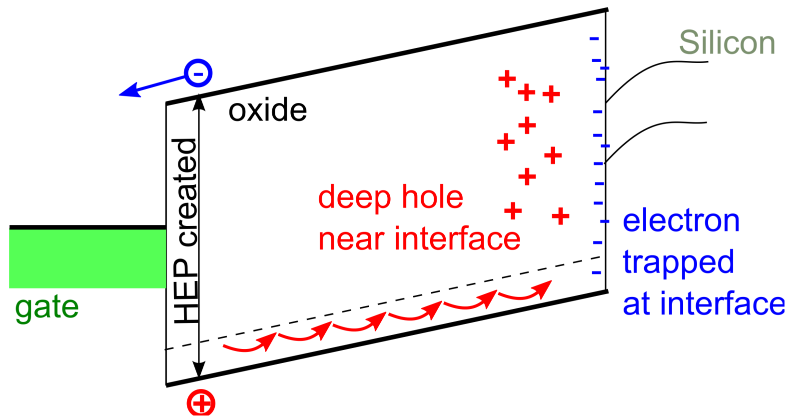

Fig. 2.3: Trapped particles in silicon oxide and at Si-SiO_2 interface.

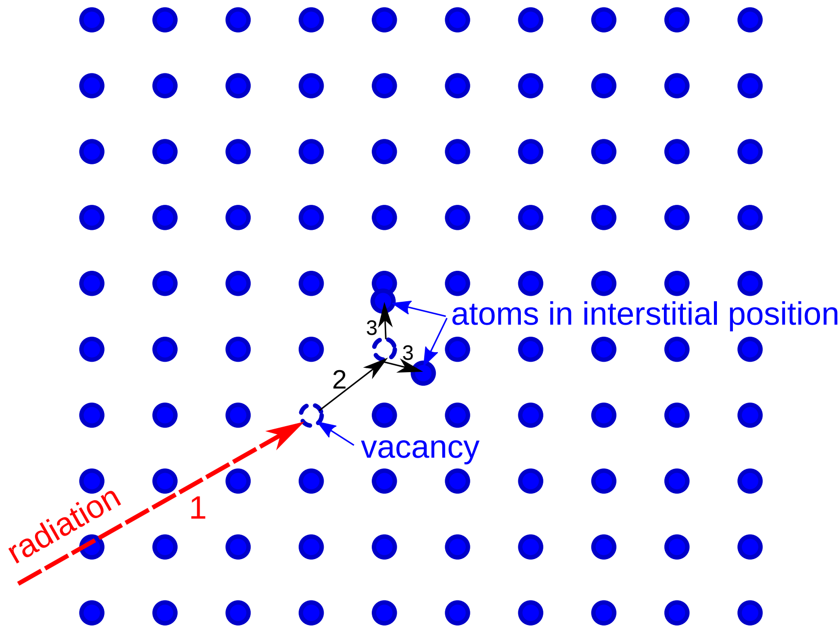

Fig. 2.4: Displacement damaging effect.

Displaced atoms cause lattice defect which acts as additional energy levels in band-gap and change the probability of carrier transition which is dependent exponentially on band-gap level.

Moreover, in the presence of electric field, displacement phenomenon introduces two different damaging effects:

1. generation of HEPs in depleted regions of p-n junctions and then inverse current as a consequence;

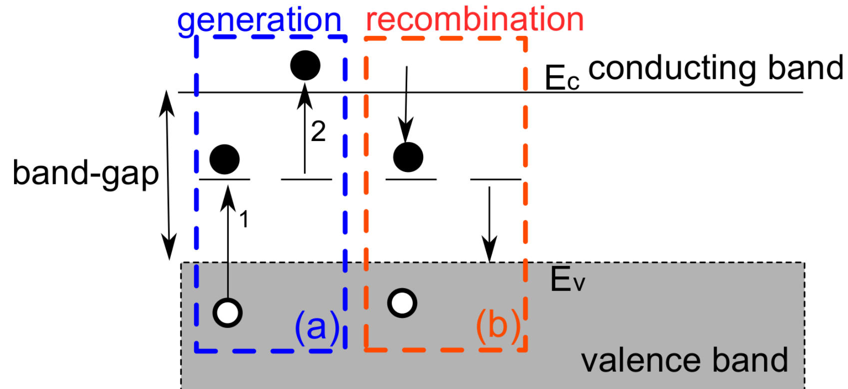

Fig. 2.5: Displacement damaging effects: (a) generation effect; (b) recombination effect.

2. recombination of HEPs in p-n junction forward-biased and reduction of charge flux (Figure 2.5).

2.2 Radiation Effects on ICs

The previous Section described the main radiation effects in a generic semiconductor. This section presents damaging effects of radiation in ICs.

Radiation effects in ICs are divided into two major categories:

1. **Cumulative Effects**, due to a long-time exposure to radiation;
2. **Single Event Effects (SEE)**, due to interaction with a single particle.

Cumulative effects are divided into **Total Ionizing Dose (TID)** effects, and **Displacement Damage Dose (DDD)** effects.

TID effects are due to electron-hole pairs generated in the oxide layer by the radiation crossing the integrated circuit. Electrons quickly flow towards electrodes while holes remain trapped within the oxide for a long time [6], [8]. Furthermore, channel carriers can be trapped at the Si-SiO_2 interface [9]. These effects cause variations in transistor parameters, such as increase or decrease of threshold voltage, increase of parasitic currents, decrease of carrier mobility and transconductance.

DDD effects are due to collisions between particles and nuclei of silicon belonging to the lattice structure [10]. These collisions may create defects into

the silicon lattice and introduce energy states in the band-gap. These trap states facilitate electron transitions between valence band and conduction band and causes mobility degradation [11].

2.2.1 TID Effects and Hardening

In CMOS integrated circuits, the most sensitive region to cumulative effects is the gate oxide. The collision of single particles with the oxide generate HEPs and if the ionized region is crossed by an electric field the electrons and holes separate. Electrons are quickly collected by neighboring electrodes because their mobility is approximately $220\,\mathrm{cm^2/(V{\cdot}s)}$, while holes move slowly toward the SiO_2-Si interface, because their mobility ranges from $10^{-4}\,\mathrm{cm^2/(V{\cdot}s)}$ to $10^{-11}\,\mathrm{cm^2/(V{\cdot}s)}$. These holes remain trapped into the oxide for a long time (approximately from $10^3\,\mathrm{s}$ to $10^6\,\mathrm{s}$) [9].

The trapped holes can be seen as fixed positive charges, which introduce a negative shift in threshold voltage, given by:

$$\Delta V_{ot} = -\frac{q}{C_{ox}}\Delta N_{ot} = -\frac{q}{\epsilon_{ox}} t_{ox} \Delta N_{ot} \tag{2.4}$$

where q is the elementary charge, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the oxide capacitance per unit area, N_{ot} is the density of trapped holes into the oxide, ϵ_{ox} is the dielectric constant of the oxide, t_{ox} is the oxide thickness.

Experimental results in the Figure 2.6 show at first degree of approximation, ΔV is proportional to t_{ox}^2 [12]. For very thin gate oxide (e.g, for thickness lower than approximately 3 nm), threshold shift becomes negligible. However, field oxides are thick (approximately in the range from 100 nm to 1000 nm) and trap positive charged particles.

The trapped positive charges generate three kinds of leakage current:

- leakage between drain and source of an n-channel MOS transistor;
- leakage between the drain-source of different n-channel devices;
- leakage between an n-well of a p-channel device and drain/source region of a nearby n-channel device.

Charge trap effects occur especially in the Shallow Trench Isolation (STI) regions at the transition between field thick oxide and gate thin oxide. The region on the side of an STI can be modeled as a parasitic transistor in

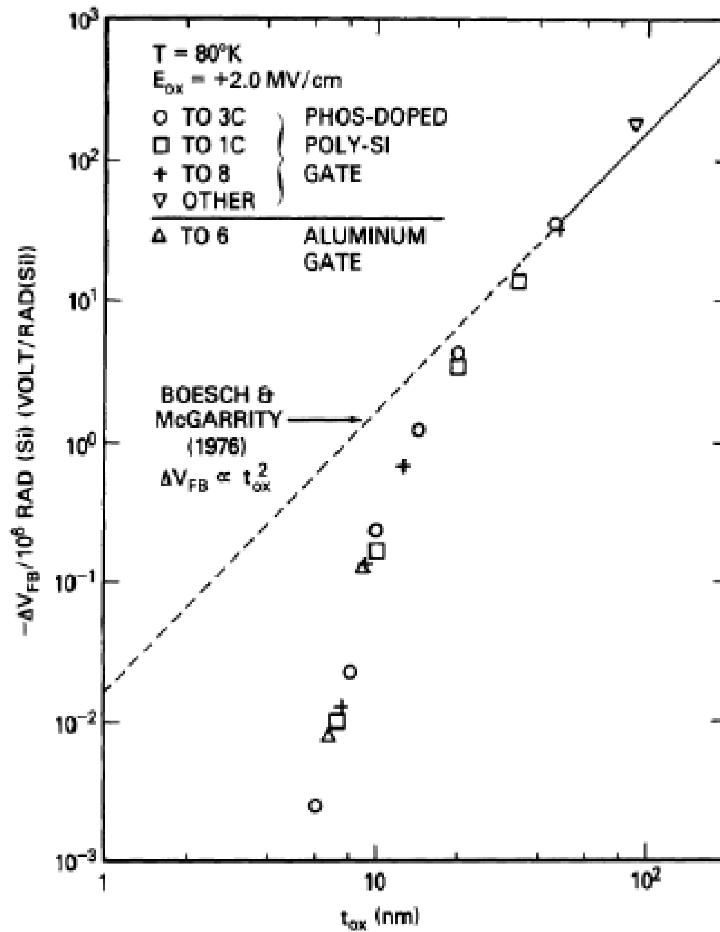

Fig. 2.6: Threshold voltage shift as function of the oxide thickness: experimental data are obtained at 80 K with an electric field of 2 MV/cm [12].

parallel to the MOS transistor channel. Parasitic transistors have the same length as designed transistors, however their voltage threshold is larger due to thick oxide, therefore the parasitic transistors are normally turned off.

The trapped positive charged particles in the thick oxide region attract negative carriers which can be considered as fixed charge on the gate of parasitic transistors and able to turn them on (Figure 2.7). The turn on parasitic transistor acts as parasitic path between drain and source, in parallel with the MOS transistor channel. Therefore, in NMOS transistors, TID may induce a parasitic channel between the source and the drain, leading to a leakage current when the NMOS device is in the “off” state.

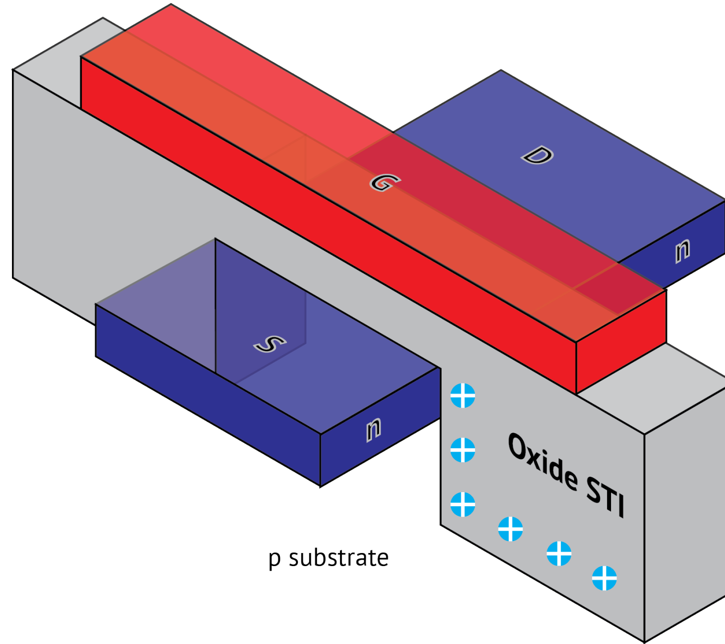

Fig. 2.7: Holes trapped in the shallow trench isolation (STI).

Furthermore, channel carriers can be trapped at the Si-SiO_2 interface [13] and decrease carrier mobility and transconductance. In a PMOS transistor, TID causes an increase of the threshold voltage and a reduction of the effective channel width. The latter effect is negligible for usual transistor sizes; however, for very narrow PMOS devices, this effect must be taken into account [14].

DDD effects are due to collisions between neutral particles and nuclei of silicon belonging to the lattice structure [15]. Lattice defects at Si-SiO_2 interface introduce energy states in the bandgap, which may trap channel carriers. The voltage threshold shift is:

$$\Delta V_{it} = -\frac{Q_{it}}{C_{ox}} \tag{2.5}$$

where Q_{it} is the trapped charge at the interface, which depends on device biasing and $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is oxide capacitance per unit area. Moreover, trap states due to lattice defects facilitate electron transitions between valence band and conduction band, and the carrier mobility decreases [16]:

$$\mu = \frac{\mu_0}{1 + \alpha \cdot \Delta N_{it}} \tag{2.6}$$

where μ_0 is the pre-irradiated mobility, α is a parameter dependent on the chosen technology, N_{it} is the number of charges trapped at interface.

It is important to point out that nowadays, TID affects mainly at the circuit in the IC periphery (pad ring) require a special care compare to IC core, due to the higher voltage and the thicker oxide of the periphery transistors [1].

2.2.2 Single Event Effects

Single Event Effects (SEE) indicates any measurable change in state or performance of a microelectronic device due to strike of a single energetic particle. SEEs can be either **soft errors** and **hard errors**.

- **Soft Error** is an error caused with radiation or electromagnetic pulses on device. Soft Error is not destructive and device remains functional;
- **Hard Error** is losing data with a permanent physical defect on device and it is not reversible, even after power reset and re-initialization.

Single Event Effects are divided in the following categories:

- **Single Event Upset (SEU)**: a soft Error caused by transient signal, generated by energetic particle strike. SEU can be expressed with:
  - SEU cross-section per device;
  - SEU cross-section per bit;
  - SEU rate (the rate of SEU occurrence).
- **Single Event Transient(SET):** a transient voltage change at a node of integrated circuit because of a single energetic particle strike.
- **Single Event Latchup (SEL):** losing the device functionality because of a parasitic current when a single energetic particle passage through sensitive region. SEL could cause also a hard error by permanent damage on device.
- **Single Event Gate Rupture (SEGR):** total or partial damage of the dielectric gate material due to an avalanche breakdown.
- **Multiple Cell Upset(MCU):** a single event that induces several cell upsets in an integrated circuit.
- **Multiple Bit Upset(MBU):** loosing of two or more bits due to SEU in a same word data.

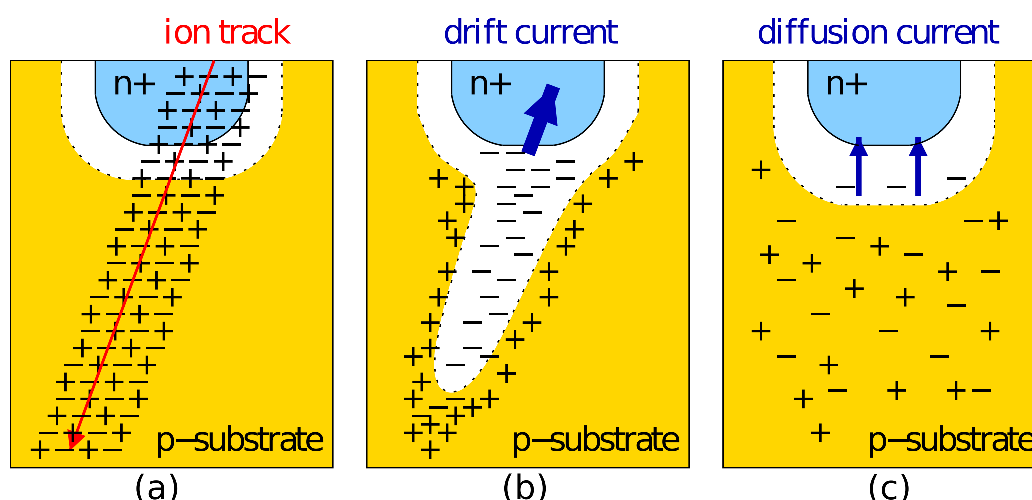

Fig. 2.8: a) Hole-electron pair generation due to a high-energy particle strikes in a p-n junction; b) Depletion region deformation and hole-electron separation (spike current due to drift); c) Diffusion current.

Reduction of transistors scales in advanced fabrication technologies increases a lot the sensitivity to the single events of radiation. In particular, ultra-scaled memory integrated circuits are more sensitive to Single Event Upset (SEU) and digital devices are more affected by Single Event Transient(SET). This sensitivity is consequence of reduction of device dimension and low voltage supplying. These reasons cause the reduction of both critic charge (the minimum of charge required to induce the flipping of logic state) and the sensitive area.

2.2.3 Single Event Effect and Hardening:

Single Event Effects (SEE) are due to charge generation in a reverse-biased p-n junction in the CMOS IC. The junction may be part of a MOS transistor (drain-body or source-body), or may be a well substrate junction.

The electric field in the reverse-biased p-n junction separates electrons and holes. The generated carriers are collected by neighbouring electrodes, thus giving a parasitic current with a peak due to carrier drift, followed by a tail due to carrier diffusion (Figure 2.8).

Sensitivity versus SEE in any particular device is evaluated by measuring the corresponding cross section vs LET:

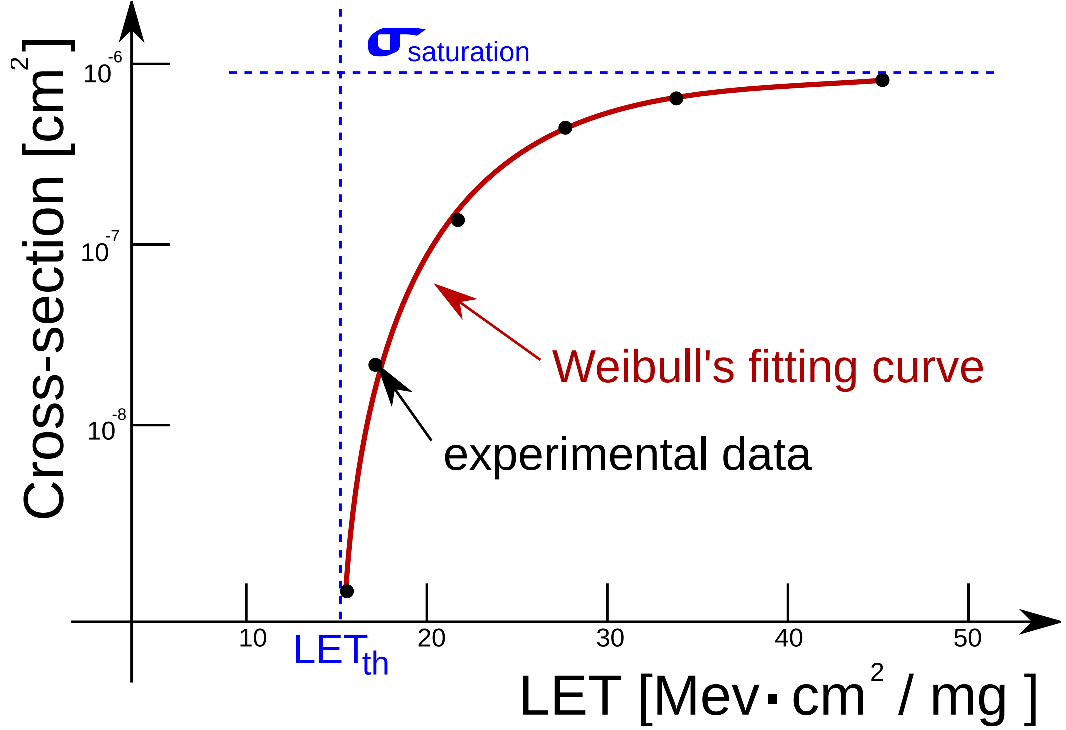

Fig. 2.9: Cross section qualitative example. LET_{th} indicates the minimum level of LET which triggers a SEE.

$$\sigma = \frac{N_{SEE}}{\Phi} \tag{2.7}$$

where σ is the cross section, N_{SEE} is the number of single events and Φ is the uniform flux over some fiduciary area. Usually, for a memory device, the cross section is normalized with the number of bits: σ is expressed in square centimeters per bit ($\mathrm{cm}^2/\mathrm{bit}$).

The error prediction rate can be derived by the cross section and some others parameters like the event duration and the nature of particle. Figure 2.9 shows a qualitative example of cross section vs. LET. The threshold LET (LET_{th}) is defined as the maximum LET value at which no effect is observed at a flux of 1×10^7 particles/cm^2 [17].

The asymptotic saturation cross section $\sigma_{\text{saturation}}$ is the value of σ approached at high LET values. The curve of σ as function of the LET is obtained by measuring the cross section at a few LET values and fitting the

data with a Weibull curve :

$$\sigma(LET) = \sigma_{saturation} \cdot (1 - e^{-(LET - LET_{th})/W^S}) \tag{2.8}$$

where W and S are fitting parameters.

2.2.4 Latch-up

Latch-up phenomena occurs in semiconductor structures with four distinct regions: p-n-p-n. These regions are physically interconnected, the middle junction is reverse biased and the other two junctions are forward biased. Latch-up is regenerative mechanism which can increase the internal current to high values after a certain threshold condition.

The latch-up mechanism is shown in Figure 2.10. The dashed line in the figure shows the negative resistance region and it occurs when applied voltage is higher than breakover voltage.

Key parameters in the latch-up characteristics are the holding voltage and holding current (I_H), which are the minimum conditions required to sustain latch-up.

These currents generated in latch-up are in order of 0.3 A to 3 A for typical devices. The high current causes localized heating in the latch-up path and because of excessive heat some failures in devices can happen as failure of metallization or bond wire, which are the most important destructive effects of latch-up in device application.

- **Two-Transistor Model:** The most usual model of latch-up phenomena is two transistors model shown in Figure 2.11, with n-well and p-substrate CMOS circuit [18]. In this model, two transistors share the same collector region and they are interconnected. The vertical p-n-p transistor is formed by the p-source (or drain) of PMOS devices within the well, the n-well, and the p-substrate. The gain of the vertical transistor is very high (30 to 100) and has a base width which is comparable to the well diffusion depth. The lateral n-p-n transistor is formed by the n-well, p-substrate, and n-source (or drain). The lateral structure typically has a much lower gain (2 to 20) and has base width which is determined by lateral dimensions imposed.

  Typical equilibrium currents in latch-up cycle is in the order of 100 mA to several ampere. This value is quite high due to the following reasons:

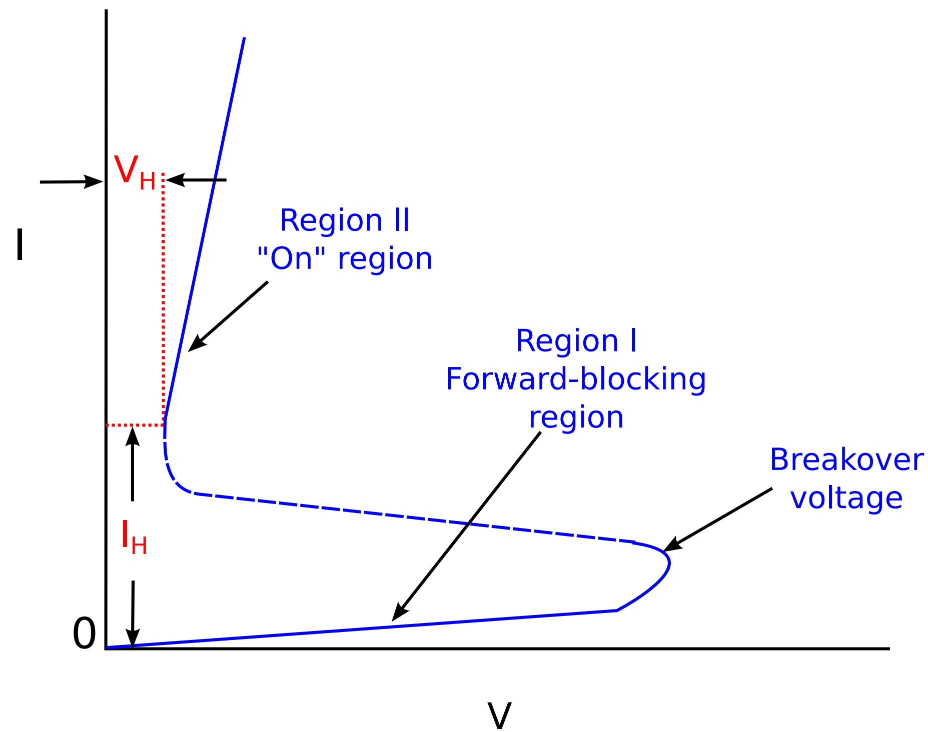

Fig. 2.10: V-I characteristics of Latch-up.

1. There are many different substrate contacts in a large area circuit, which reduces the substrate resistance. 2. The equilibrium current is limited only by external circuit resistance (typically bond and metallization resistance).

Latch-up occurs by these conditions:

- The gain of the compound structure must provide positive feedback. It means $\beta_V.\beta_L > 1$ where β_V and β_L are the gain of vertical and lateral transistors;
- The applied voltage to the structure, holds initial voltage value which is vital for existence of latch-up condition.

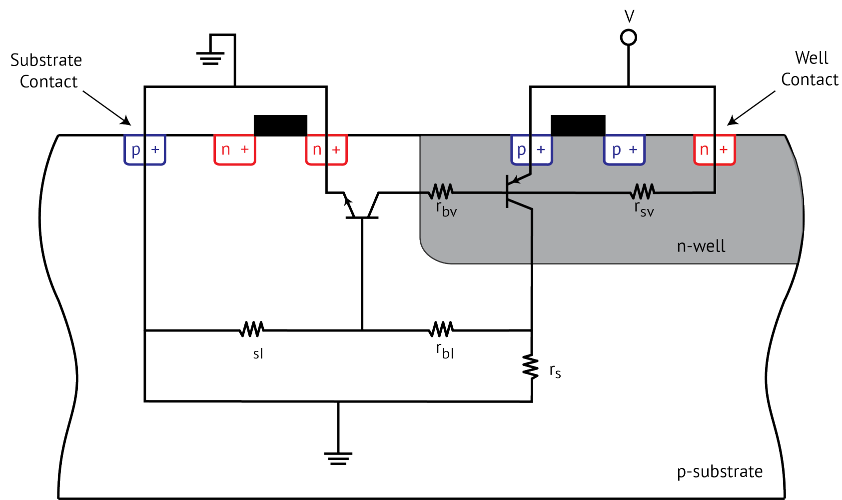

Fig. 2.11: Latch-up schematic in CMOS transistors.

3. RADIATION ENVIRONMENT

3.1 Space

The radiation environment around the Earth is historically divided into: inner belt dominated by energetic protons, a slot region of relatively lower dose behind shielding and an outer belt dominated by energetic electrons (Figure 3.1). Throughout these regions, there are cold plasma and during geometric storm and sub-storms hot plasma. At high latitudes and altitudes, these population intermix with interplanetary environment dominated with cold plasma and energetic particles of solar and galactic origin. In semiconductor instruments the low energetic particles affect surface, causing total dose degradation through both ionizing and not-ionizing charge. Table 3.1 summarizes the Satellite hazards of particles and their dynamic timescales [19].

Satellite operations are affected by the variations of the particle population identified in Table 3.1. Hereafter the different kind of particle identifications are discussed in more details.

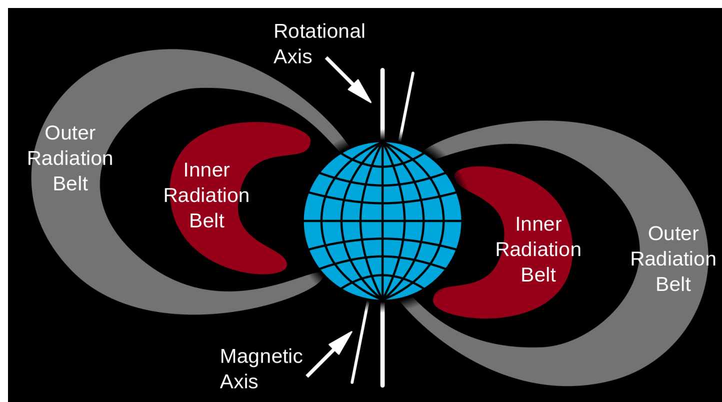

Fig. 3.1: The cross sections of Van Allen radiation belts.

Tab. 3.1: Satellite hazards due to space radiation and plasma, the responsible particles and their dynamic timescale.

Satellite Hazard	**Particle Population**	**Natural Variation**
Surface Charging	0.01 - 100 keV e^-	Minutes
Surface Dose	0.5 - 100 keV e^-, H^+, O^+	Minutes
Internal Charging	100 keV - 10 MeV e^-	Hours
Ionizing Dose	>100 keV H^+, e^-	Hours
Single Event Effects	>10 MeV/amu H^+, heavy ions	Days
Displacement Damage Dose	>10 MeV H^+ , Secondary n, MeV e^-	Days and hours for e^-
Nuclear Activity	>50 MeV H^+ , Secondary neutrons	Weeks

3.1.1 Energetic Plasma

Hot plasma is composed of ionized particles with energy in the range of kiloelectronvolt (keV). Hot plasmas are trapped by the Earth's magnetic field and some of energetic plasmas carry significant current which modifies in large scale the Earth's electromagnetic field specially during strong magnetic activity in the space. Figure 3.2 shows a large scale view of the magnetosphere and it's domains, where the energetic plasma is found in the plasma sheet and the ring current. Magnetic storm flows a ring of current in the equatorial plain and burst current flows from the magnetotail into the inner magnetosphere. The figure 3.3 shows the schematic plasma injection from the magnetotail into the inner magnetosphere.

3.1.2 Trapped Electrons

Electrons with energy above of 100 keV should be treated separately from plasma electrons for two main reasons: at first they are dominated by magnetic force and other dynamic forces can be neglected, second they can penetrate just the thinnest shielding. Thus 100 keV becomes the dividing point between plasma electrons and radiation belt electrons. Trapped electrons are found often in inner magnetosphere in two or more belts and the inner belt has lower energy electrons compare to outer one. The region between belts is called

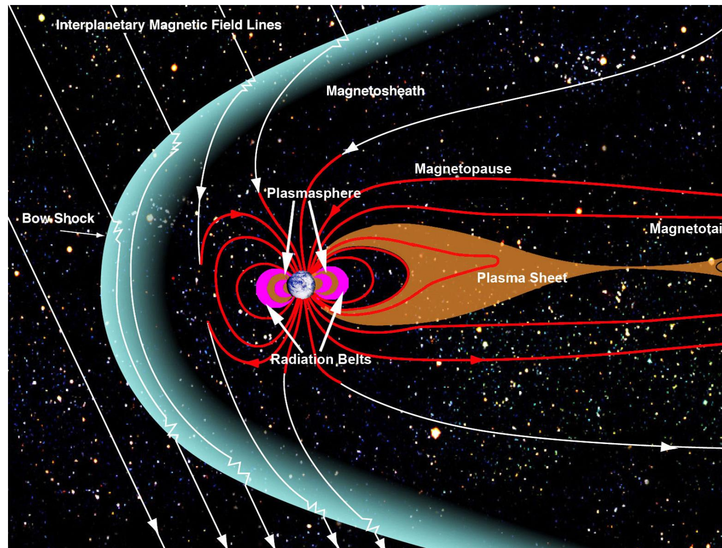

Fig. 3.2: Diagram of Earth's magnetosphere (from `www.nasa.gov`).

.

Slot and it's location and size depend on energies and magnetic activity. The figure 3.4 shows a cutaway view of the two-belt structure electron radiation belts. The outer radiation belt intensity can vary by orders of magnitudes on timescales, from minutes to days, and typically it begins with a sudden loss of trapped electrons with the depth of penetration of loss which depends on the intensity of the storm. After the storm, the slot starts to re-establish itself in few days.

3.1.3 Trapped Protons

Trapped protons have energies up to a few gigaelectronvolt and are found in the Earth's inner radiation belt. Their intensity is peaking near magnetic equator at altitudes about 3000 km. For altitudes up to 2000 km the radiation is systematically more intense over the South Atlantic and South-Eastern Pacific ocean, and less intense or absent over the Indian Ocean. Above 8000 km the intensity episodically changes in response to the solar particle and *geomagnetic activity*. The intensity of trapped protons has evolving time in order of decadal (period of 10 years) with the change in the Earth's internal magnetic field.

The radiation protons are generated from two sources: *Cosmic Ray Albedo Neutron Decay (CRAND)* and *Solar Energetic Protons*. CRAND is a slow

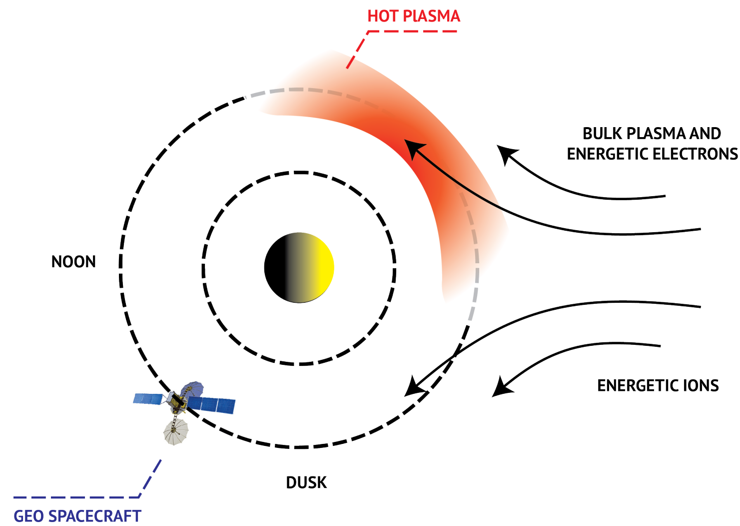

Fig. 3.3: Schematic hot electron plasma injection from the magnetotail into the inner magnetospher.

process and varies in time of solar cycle. Solar Energetic Protons are trapped in the inner belt when a geomagnetic storm coincides with a solar particle event [20] and their transient increase during intense geomagnetic activity [21]. However during quiet and moderate geomagnetic activity the trapped proton population is typically very stable.

3.1.4 Solar Energetic Particles

Solar Energetic Particles flood interplanetary space with protons and heavy ions with energy upto 100 MeV [22]. These event begin with a *Solar Flare* or/and *Coronal Mass Ejection (CME)* at the Sun (Figure 3.5). When a Solar Flare happens, a first wave of energetic particles arrives at Earth, essentially at the speed of light, and then a second more intense wave of energy particles arrives along with the CME. Sometimes, events can also be detected by observing an increase in neutron radiation at ground level.

Particles in interplanetary space can absorbed and trapped in some regions of earth magnetosphere, and the dividing lines between these regions is known as the *geomagnetic cutoff*. At polar latitudes, essentially all solar energetic particles have access all the way down to the atmosphere. In fact, intrinsically, the magnetic field is actually stronger by a factor of two at the pole than the equator. However, it is the topology of the magnetic field that ultimately

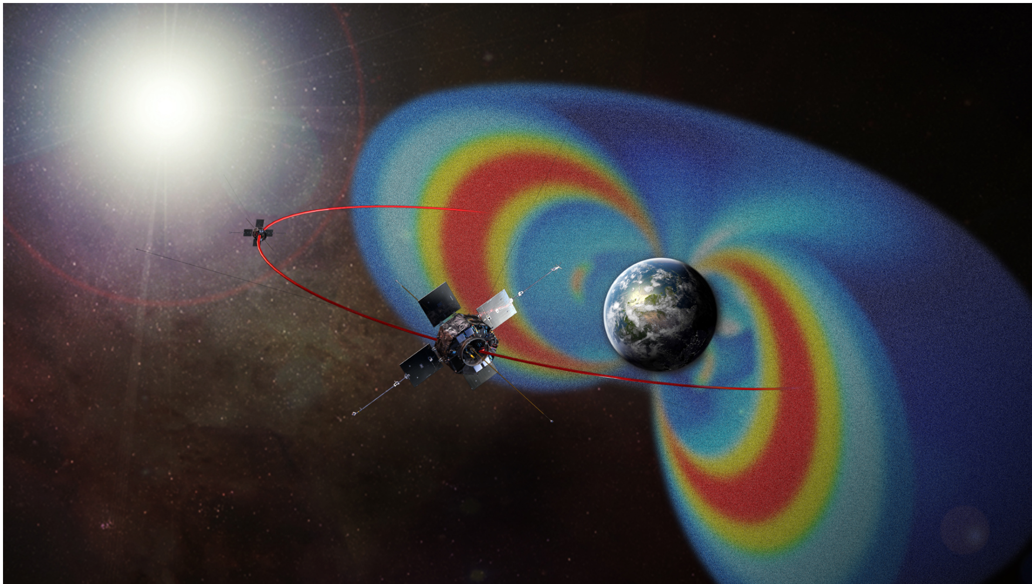

Fig. 3.4: Cutaway view of the two-belt structure electron radiation belts (from `www.nasa.gov`).

filters out the interplanetary particles (Figure 3.6). The Solar Energetic Particles contribute to Ionizing, Displacement and Single Event Effects. The proton and ion flux together can be used to estimate the permanent SEE failures like latch-up during a satellite space mission.

The scientific and technical challenges introduced in this chapter need a continuous improvements in physical modeling of environment effects on electronic components and, moreover, better radiation hard design and test method are needed to reach a higher performance of electronic components in harsh environments.

3.2 High Energy Physics Experiments

The environment of collision area in high energy physics experiments has very particular conditions because of high flux of particles and high temperature. In specific, at the European Organization for Nuclear Research (CERN) the radiation environment of ATLAS and CMS experiments is determined by the proton-proton collision at their center.

The collision environment of CMS and ATLAS at CERN contains the charged Hadrons with energy distribution which covers the range between

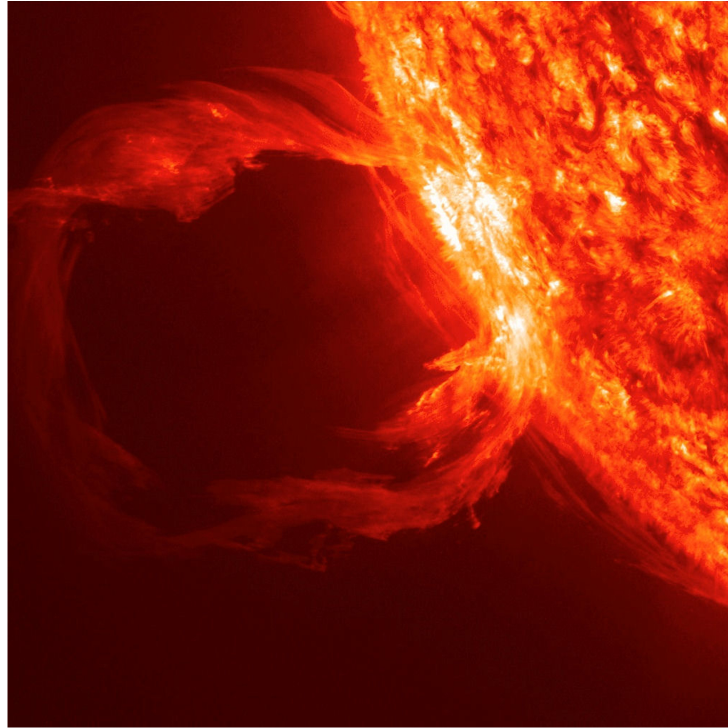

Fig. 3.5: An eruption on April 16, 2012 was captured here by NASA's Solar Dynamics Observatory in the 304 Å wavelength, which is typically colored in red. (from `www.nasa.gov`)

about 1 MeV and 10 GeV. The spectrum is peaked at around 200-300 MeV and remains almost invariant in shape from the tracker to the outer periphery of the experimental cavern with absolute fluxes which change by order of magnitude. The neutron distribution has instead a substantial flat low-energy component, typically only one order of magnitude lower than the peak at 1 MeV and this range of neutrons contributes significantly to Displacement Damage Effects. The neutron spectrum has also another peak at 60 MeV to 100 MeV and extends at high energy up to about 1 GeV to 10 GeV, which depends mainly on the location point.

Table 3.2 summarizes the radiation levels in different regions of ATLAS as cumulative doses over the 10 years expected lifetime of the Large Hadron Collider (LHC) at CERN. In each region of Table 3.2 the field is characterized by three parameters: TID level, fluence of neutrons above 100 keV and fluence of all Hadrons above 20 MeV which are reference levels for Ionization, Displacement Damage and Single Event Effects.

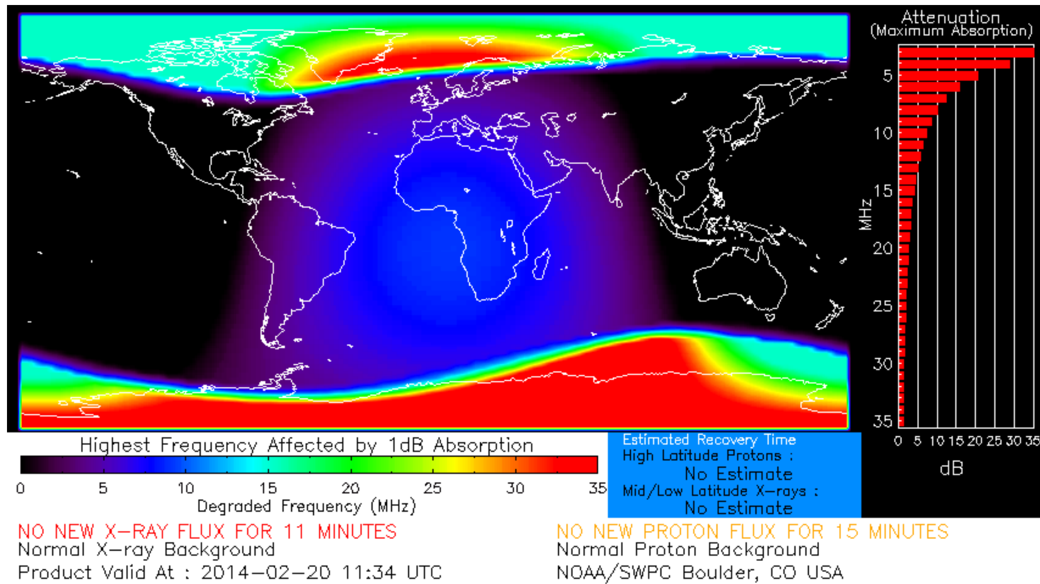

Fig. 3.6: The sun erupted peaked in X-ray at 7:56 UTC on Feb. 20, 2014 (3:56 EST) (from `http://www.thesuntoday.org/`).

3.2.1 Hadron Collider Radiation Environment Radiation Issues

The radiation environment issues at CERN are somehow different from space applications, mainly because of absence of heavy ions. For instance, the proton radiation test demonstrates a very low frequency of Single Event Latch-up (SEL) or Single Event Gate Rupture (SEGR) in similar radiation environments. Moreover the abundance of neutrons with energy higher than 100 keV increases significantly displacement damage (DD) compared to the space application environment.

The radiation environment at CERN experiments can be divided into two main regions: **inner region** (Figure 3.7) and **outer region** (Figure 3.8).

In the inner region, the TID levels are very high and it is unthinkable to use commercial electronics, therefore all electronics are implemented by custom ASICs. These developed custom electronics need to be manufactured in technologies able to withstand to the expected total dose and have a high tolerance of IC design to SEEs in order of minimize the rate of soft errors such as Single Event Upset (SEU), Transient and Functional Interrupt (SEU, SET or SEFI). In the outer region of CERN experiments, the TID level varies between less than 1 krad to more than 25 krad, therefore most of electronic functions are implemented with commercial devices.

Tab. 3.2: Cumulative dose of radiation over 10 years in different region of Large Hadron Collider (LHC).

Detector region	**TID[rad]**	**Neutrons 1 MeV [cm^{-2}]**	**Hadrons > 21 MeV [cm^{-2}]**
Innermost tracker (barrel)	$2.7 \cdot 10^7$	$4.7 \cdot 10^{14}$	$5.4 \cdot 10^{14}$
Outer tracker (barrel)	$5.1 \cdot 10^6$	$1.910^{14}\cdot$	$9.3 \cdot 10^{13}$
ECAL (barrel)	$1.1 \cdot 10^4$	$3.110^{12}\cdot$	$6.0 \cdot 10^{11}$
HCAL (barrel)	$1.0 \cdot 10^3$	$4.3 \cdot 10^{11}$	$1.0 \cdot 10^{11}$
Muon detector (forward)	$3.4 \cdot 10^4$	$1.2 \cdot 10^{13}$	$1.9 \cdot 10^{12}$
Experimental cavern	$1.7 \cdot 10^3$	$6.5 \cdot 10^{10}$	$1.5 \cdot 10^{10}$

3.2.2 HL-LHC Upgrade and RD53

The High Luminosity LHC (HL-LHC) at CERN is the proposed upgrade to the LHC to be made in a long machine shutdown which should take place in the years 2023 to 2025.

The upgrade aims at increasing the luminosity of the machine, i.e, the ratio of the number of events detected in a unit of time to the interaction cross-section, up to $5 \times 10^{34}\,\mathrm{cm}^{-2}\cdot\mathrm{s}^{-1}$, which means an increase by a factor of 10 with respect to the current luminosity. The upgrade will improve statistically marginal measurements and will allow a better chance to see rare processes.

The ATLAS and CMS experiments at CERN are planning major detector upgrades to cope with the increase in beam luminosity. Pixel detectors are placed in the innermost part of the experiments and are therefore exposed to the highest flux and highest ionizing radiation dose. Simulations show that the innermost parts of the new pixel detector will integrate a flux of about $10^{16}\,\mathrm{n/cm}^2$ (MeV neutron equivalent) and a Total Ionizing Dose (TID) of 1 Grad [23]. HL-LHC requires a new generation of hybrid pixel detectors which present major challenges on several fronts. The IC design issues include: smaller pixels to resolve tracks in boosted jets, much higher hit rates (1 GHz/cm^2 to 2 GHz/cm^2), unprecedented radiation tolerance (10 MGy), much higher output bandwidth, and large IC format with low

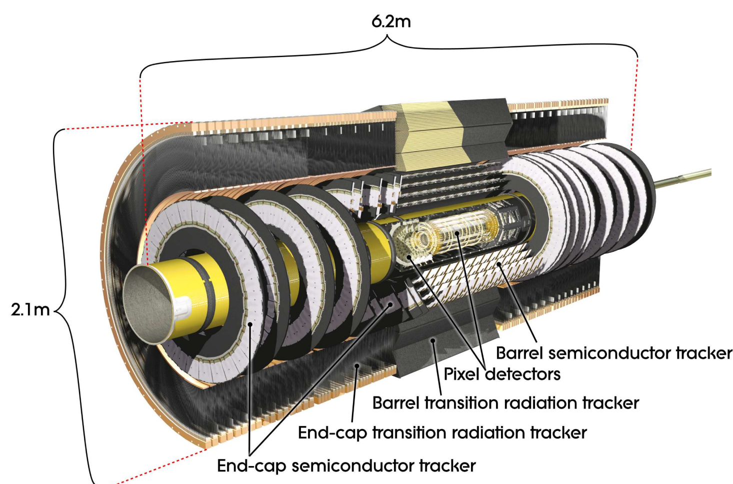

Fig. 3.7: Inner region of ATLAS experiment at CERN (from `http://home.web.cern.ch/`).

power consumption in order to instrument large areas while keeping low the material budget.

RD53 is a new collaboration at CERN with 18 participating institutes in the aim of design the next generation of hybrid pixel readout chips for both ATLAS and CMS Phase 2 pixel upgrades.

The RD53 collaboration is focused on: qualification of a technology able to survive in the harsh radiation environment, definition of a top level architecture, development of a simulation framework, development of radiation hard cells, evaluation and design of the analog front-end, design of specific IP blocks.

CHIPIX65 is the Italian part of RD53 collaboration with 35 members funded by National Institute for Nuclear Physics (INFN). CHIPIX65 supports the development and test the radiation hard SRAM prototype which is the main subject of this dissertation.

The technology chosen by the RD53 collaboration is 65 nm CMOS technology. This particular choice is done for different factors: first of all, it allows for considerably higher density and lower power consumption designs compared to technologies used in current projects (mainly 250 nm and 130 nm). Then, it is a mature technology, being first introduced in the market in 2007 and it will be available for the foreseeable future, as it's widely used in the semiconductor industry [24].

The 65 nm CMOS process can be an optimal option for the future pixel

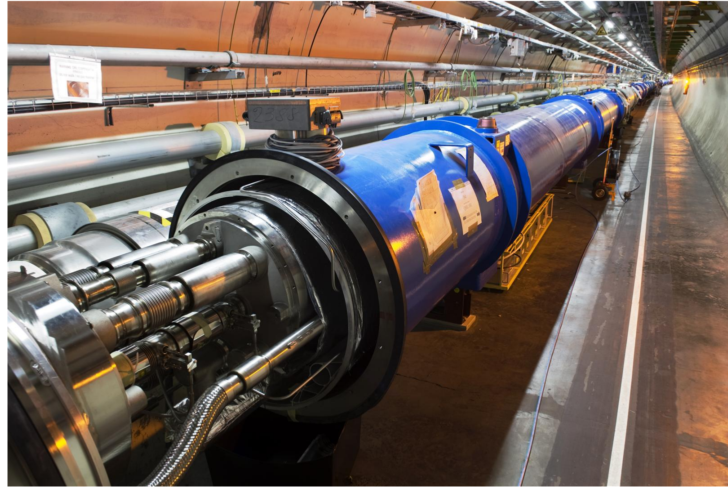

Fig. 3.8: Outer region, view of the tunnel LHC machine (from `http://home.web.cern.ch/`).

readout chips in term of high integration density, but it still have to be extensively tested and qualified for the irradiation, which in HL-LHC will reach unprecedented levels. The radiation damage on the proposed 65 nm technology, due to both total dose and single event effects, has been studied by the RD53 Radiation Working Group [23] and demonstrates a good compatibility with experiment requirements.

4. RADIATION HARDENED SRAM

Detector readout circuits in high energy physics experiments are very sensitive circuits and they are exposed to very high amount of radiation. In this dissertation an innovative radiation hardened Static RAM (SRAM) is proposed, designed and characterized for application in pixels readout operation in high energy physics experiments, specially at CERN. Moreover, the proposed radiation hardened SRAM is also suitable for space environment application. Radiation Hardening of circuit is achieved by Radiation Hardened by Design methodology. The proposed radiation hardened SRAM is designed in 65 nm CMOS technology. The particular choice of 65 nm was done due to a number of factors. First of all it allows for considerably higher density and lower power consumption designs compared to technologies used in current projects of high energy physics experiments (mainly 250 nm and 130 nm). It is a mature technology, being first introduced in the market in 2007 and it will be available for the foreseeable future, as it is widely used in the semiconductor industry [24]. Even though TSMC 65 nm CMOS technology has a high intrinsic radiation tolerance even though innovative architecture and implementations are still needed to reach higher level of radiation tolerance in extreme environments [23].

4.1 Radiation Hardened SRAM Architecture

The most important environment limitation in using memory cells in radiation is Single Event Upset (SEU). SEU occurs when a single particle (e.g., a cosmic ray, a recoiling nuclear reaction product or an alpha particle from radioactive decay) strikes a sensitive volume of a memory cell, generating sufficient charge to cause a change in the logic state of the cell (Figure 4.1) [25], [26]. The affected node will remain in the upset state until new data is written into the memory element. Furthermore if a single particle strikes several cells a Multiple Bit Upset (MBU) might occur.

RHBD solutions to mitigate SEU in SRAM can achieved by:

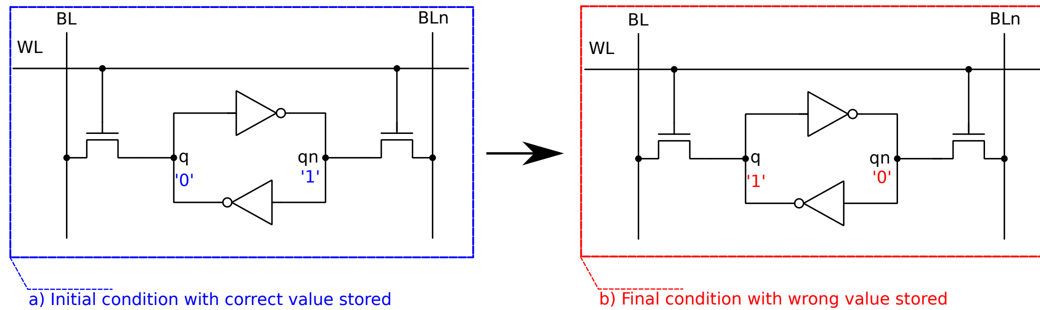

Fig. 4.1: The charge delivered to the node q is larger than the critical charge: (a) before the interaction, the cell stores a '1', (b) after the collision the latch changes its state to '0'.

- designing larger transistors to increase the critical charge;
- designing a conventional 6-T SRAM cell and adding extra capacitors or resistors to increase the node critical charge [27];
- designing a cell composed of several feedback loops (Dual Interlocked storage CEll: DICE) [28–30];
- using Triple Modular Redundancy (TMR) or encoding and decoding data.

In high density CMOS ICs, Single Event Upset is the most difficult radiation effect to avoid and experimental results shows that the critical charge able to produce an upset decreases as the inverse square of the feature size [31]. Therefore, technology scaling makes front-end electronics for high energy experiments much more sensitive to SEU effects, and old SEU hardening design techniques (e.g., resistive or capacitive hardening) are not efficient anymore.

Based on RHBD approach, system level design solution can also be used to increase the tolerance of ICs to SEU. For instance, coding techniques for error detection and correction can be used for memory array [32] or Triple Modular Redundancy (TMR) techniques, consisting in storage cell replication and majority decision, can be applied to flip-flop and registers in sequential logic. However, these SEU hardening methods need additional circuits at system level which cause higher power dissipation. Moreover in some cases upset tolerance can be lost as the result error latency. Indeed, a first upset is tolerated, but the state of the affected element may not be restored before the

subsequent occurrence of a second upset, and thus the system is vulnerable to correlated double errors.

In this dissertation an innovative architecture based on Dual Interlocked storage Cell (DICE) is employed to design a radiation hardened SRAM. The literature shows that the DICE architecture has already used and investigated as a single cell, however design and test of an array of DICE SRAM in 65 nm CMOS technology is innovative. To identify the radiation tolerance of radiation hardened SRAM, a big array of memory is required to reach a high statistic of bit upsets in radiation test. The design based on DICE architecture has a lower area overhead compared to other logic design hardening techniques for both CMOS static RAM cells and sequential logic elements (latches, flip-flops, registers etc.) [30].

4.1.1 DICE SRAM

Dual Interlocked Cell (DICE) is an alternative architecture which can be used to mitigate the Single Event Upset in several digital circuits. DICE SRAM cell architecture employs 4 PMOS and 8 NMOS transistors and has two interlocked SRAM cells with 4 pass transistors. In this architecture both the bit and the inverted bit are stored into two separate nodes (Figure 4.2), therefore data is redundant.

In Figure 4.2, the nodes with the same letter and different numbers are equivalent, and the whole circuit is in a stable state just when these equivalent nodes have the same logic value.

Writing operation occurs when all 4 NMOS pass transistors are active and all identical nodes change the logic value simultaneously.

When a particle passes through a DICE SRAM single memory cell, changing the logic state requires the simultaneous changes of at least one pair of equivalent nodes. Physical separation of equivalent nodes at layout design decrease significantly the probability of single upset events. Further different studies at layout level are performed in this dissertation to increase the tolerance of circuit to SEU.

Pass transistors of the DICE cell can be either PMOS or NMOS transistors; in this implementation NMOS transistors are chosen because they have higher tolerance in total dose effects.

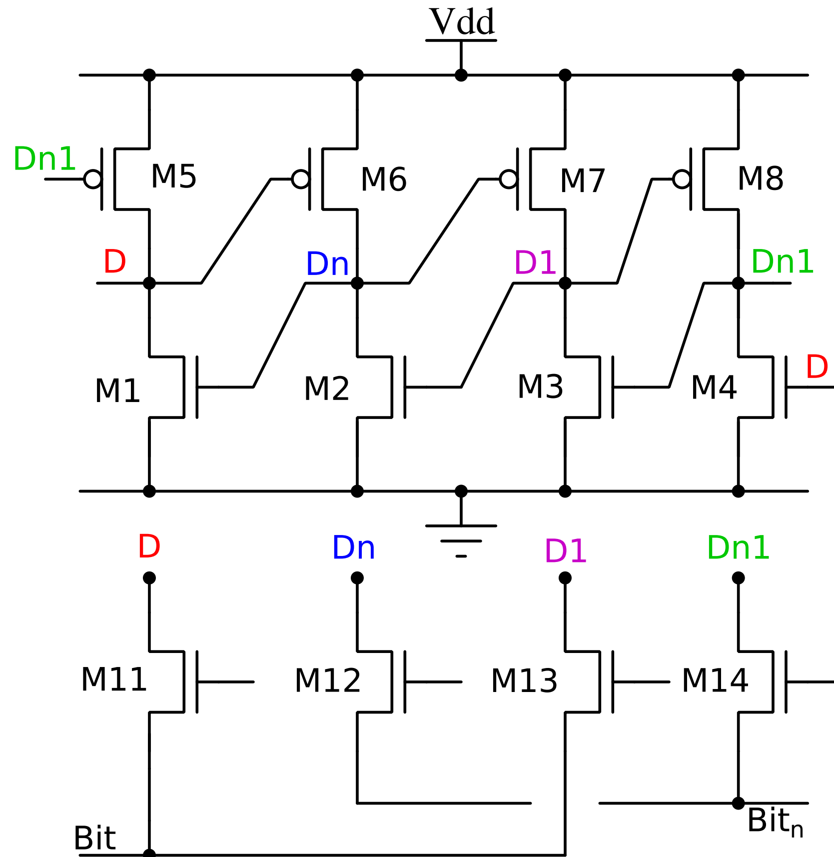

Fig. 4.2: Schematic view of DICE Single Memory Cell architecture.

4.1.2 Memory Array

The memory array is arranged in 256 × 256 single memory cells. The block of memory has 256 word-lines and 256 bit-lines. The crossing point of selected word-line and bit-line is the selected single memory cell for read or write operation (Figure 4.3).

4.1.3 Decoders

The architecture of memory block decoder has three main parts:

- 256-output word-line decoder: selects a word-line among 256;
- 256-output bit-line decoder: selects a bit-line among 256;
- demultiplexer: converts the 16 addresses bit: A<0:15>, into 64 output signals:

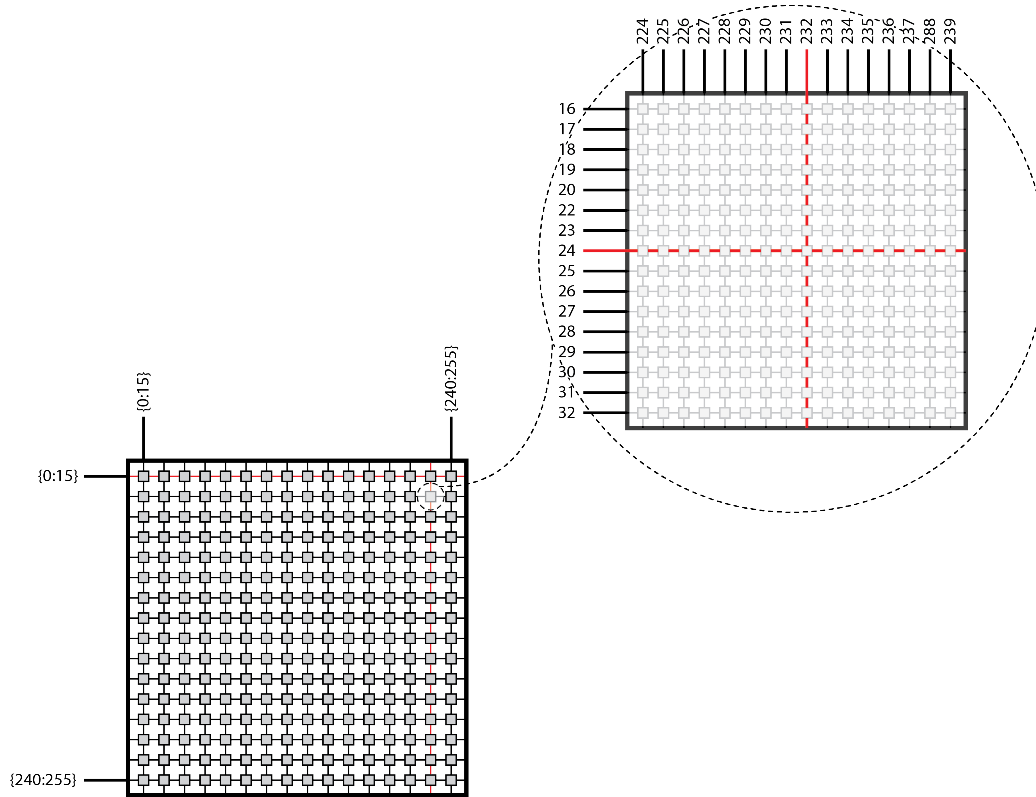

Fig. 4.3: Schematic of memory array architecture: the crossing point of horizontal red-line (word-line 24) and vertical red-line (bit-line 232) is pointed on selected single memory cell.

- p<0:15> and d<0:15> are the address signals used inside the word-line decoder. In particular, p<0:15> signals are used in the first level, whereas d<0:15> are used in the second level of the word-line decoders.
- Y_n<0:15> and Y_m<0:15> are the address signals used inside the bit-line decoders. In particular, Y_m<0:15> signals are used in the first level, whereas Y_n<0:15> are used in the second level of the bit-line decoders.

As shown in the figure 4.4 in a schematic way, the decoder operation has two levels:

1. A line in the group of sixteen lines is selected;
2. A line in a group of sixteen lines, previously selected, is selected.

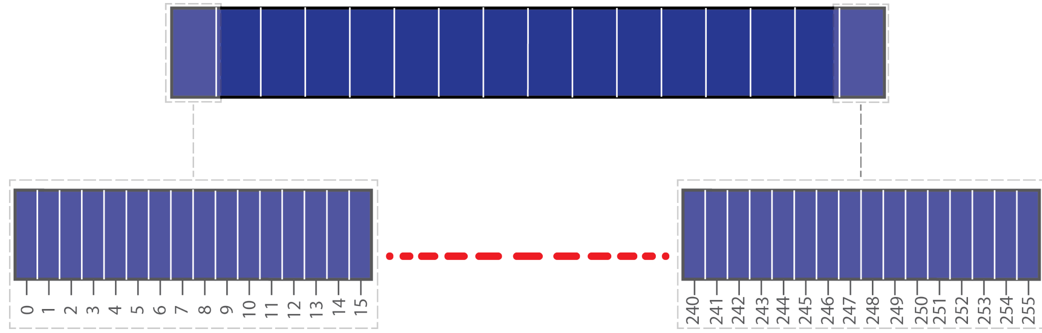

Fig. 4.4: Decoder architecture.

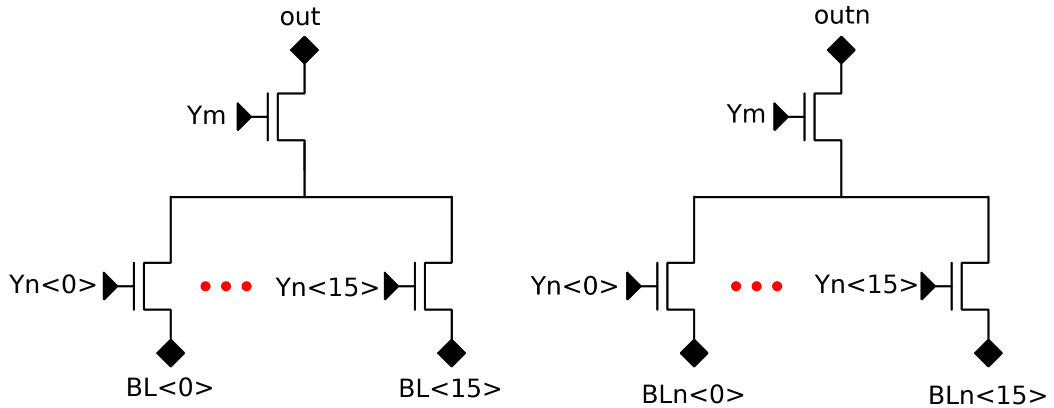

Fig. 4.5: Bit-line decoder: schematic view of final stage.

The bit-line decoder consists of two pass transistors connected in series (Figure 4.5). The first series of transistors belongs to the first level of the decoder and the second series of transistors belongs to the second level of decoder. Each decoder has 16 transistors in first level controlled by Y_m<0:15> signals and 256 transistors which are 16 blocks with 16 transistors for each block at second level controlled by Y_n<0:15> signals.

The word-line decoder consists of a pass transistor biased by the first level of decoder signals p<0:15> and controlled by the second level of decoder signals d<0:15>. The pass transistor is followed by an inverter in final stage (Figure 4.6).

4.1.4 Equalizer

The bit-line wires in the array of memory are as long as the vertical length of memory array. The high capacitance value (some picofarad) of bit-line wires

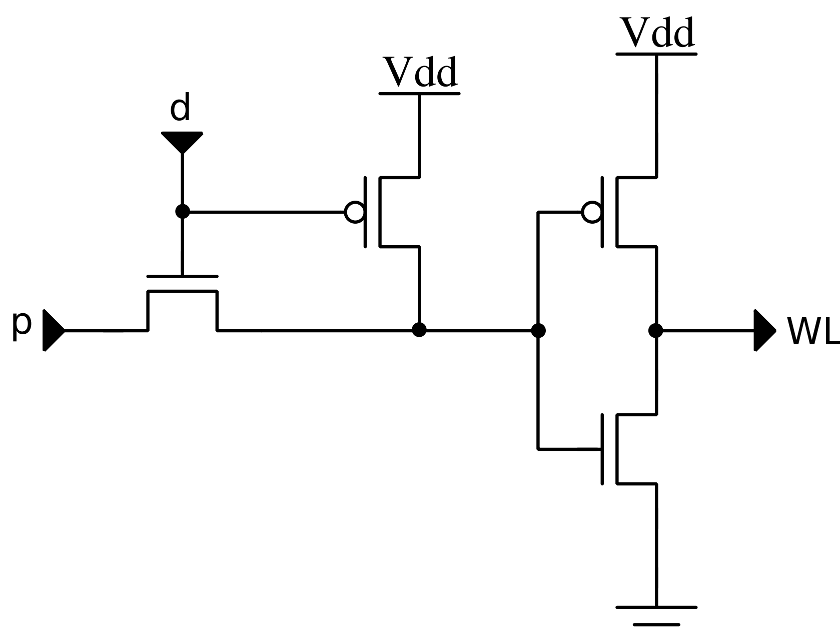

Fig. 4.6: Word-line decoder schematic in final stage.

leads to delay in achieving high or low logic value voltages during *write* and *read* operation. To solve this problem, a dedicated circuit is used to equalize the voltage of bit-lines after every read and write operation. The architecture contains two pass-transistors as which equalize the voltage of bit-line and negative bit-line when Eq signal has high voltage value (Figure 4.7). The voltage of bit-line wires reaches to half of high voltage value, therefore the bit-line wires require the same time to reach both the low logic voltage and high voltage value.

4.1.5 Sense amplifier

Transistor conductance might be different for transistors designed with the same characterization. To pass over this problem in read operation, the sense amplifier circuit is employed to have readout operation with differential approach. Sense amplifier circuit reads analog voltages difference between bit-line and negative bit-line. The read operation is activated by the EN signal (Figure 4.8).

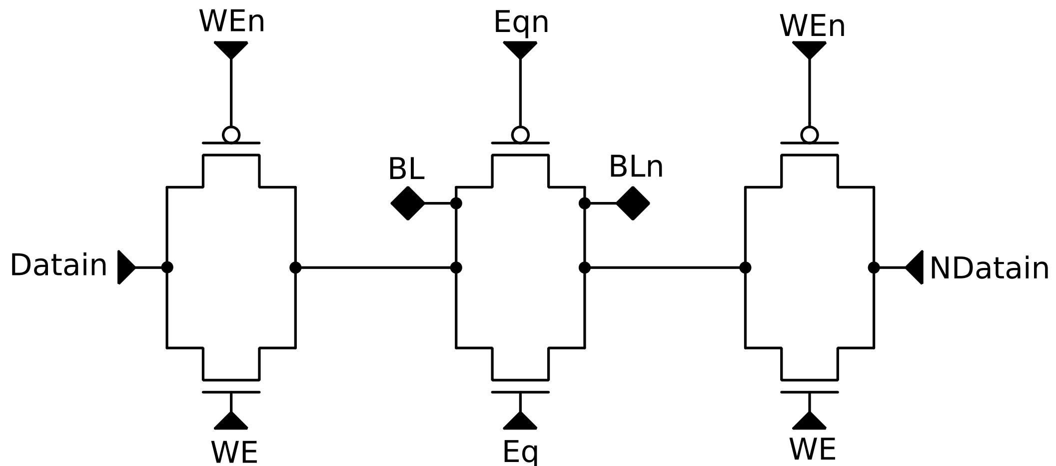

Fig. 4.7: Schematic view of the equalization circuit.

4.1.6 How SRAM Block Works

The SRAM block has three modes of operation (Figure 4.9):

- **Stand-by:** the memory stays in the static mode with stored data. The memory block has the lowest power consumption in this state and transistors do not commute.

- **Write:** the single memory cell, which is selected by decoder, stores the input-data (Figure 4.10). Write operation occurs when:

  - WE pin has high voltage value and the pass transistors are turned-on, therefore Bit and Negative Bit signals pilot the Bit-line and Negative Bit-line;
  - sense circuit is disactived by low voltage on SenseEn pin;
  - specific single memory cell is selected by 16 addressing bits on decoders.

- **Read:** data storage in selected single memory cell reads from the output pin of memory block (Figure 4.11). Read operation occurs when:

  - sense circuit is active with low voltage on SenseEN pin, therefore the sense amplifier circuit performs the differential read-out operation;

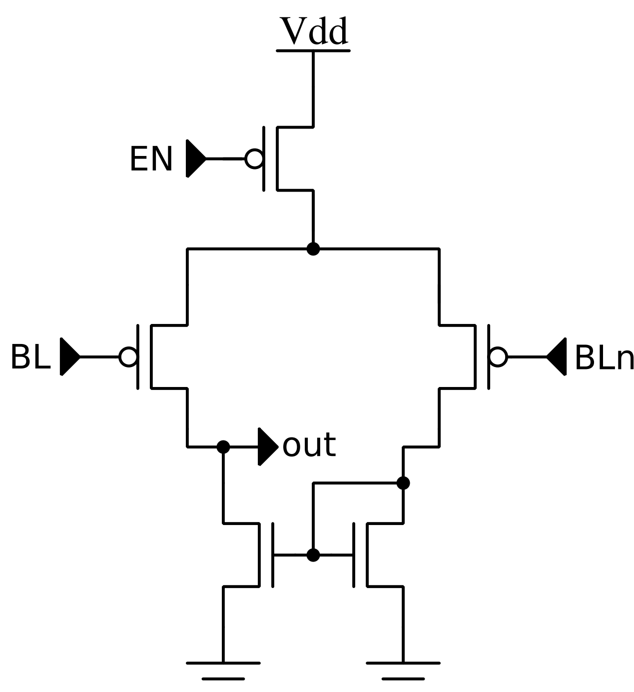

Fig. 4.8: Schematic view of Sense amplifier.

Fig. 4.9: Diagram of SRAM operation.

- pass transistors of equalizer circuit are disactived with low voltage signal on WE pin;
- addressing the decoders with 16 address bits for specified single memory cell.

4.2 Radiation Hardened SRAM Layout

The layout design of different parts of the SRAM block is explained in this section. Studying the radiation effects on SRAM memory and finding a specific layout design technique to increase the tolerance to different effects of radiation is one the most important part of this dissertation.

The layout of whole memory block, including single memory cells, Decoders, Write and Read circuits are designed with full-custom methodology in

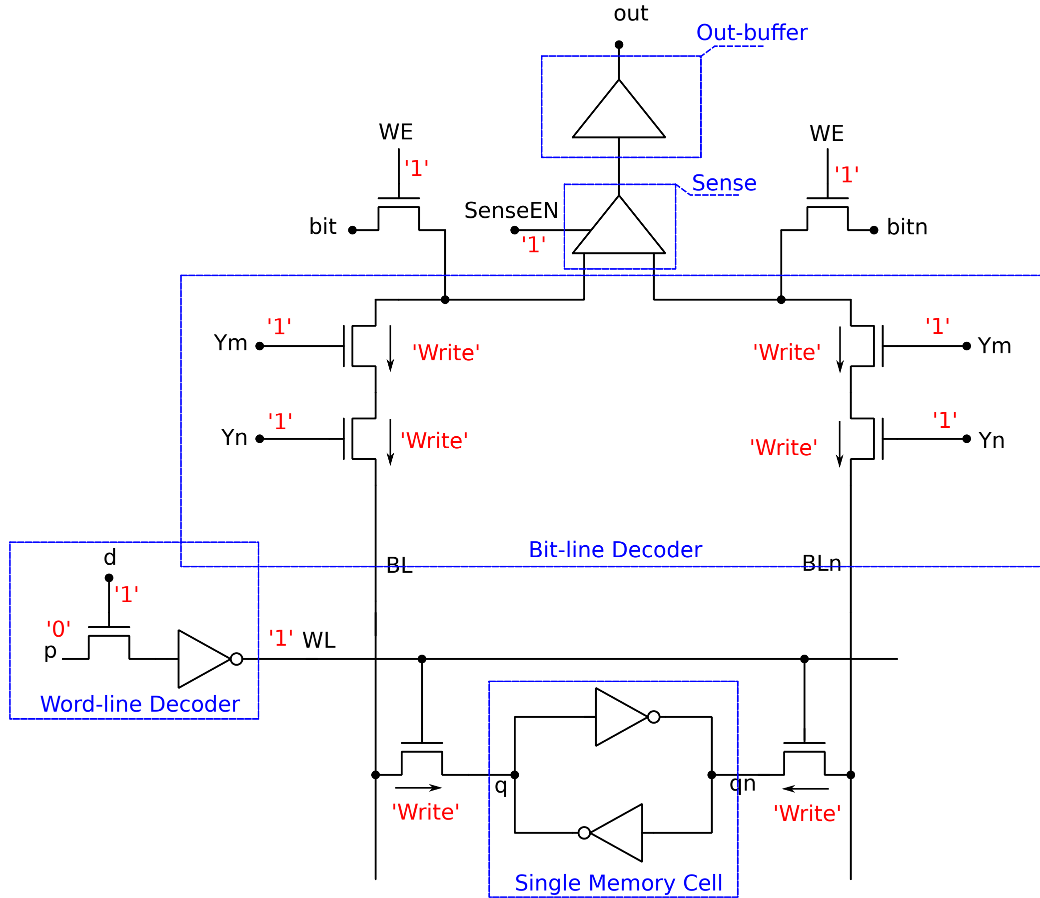

Fig. 4.10: Schematic of Write operation.

65 nm CMOS Technology and manufactured in **Taiwan Semiconductor Manufacturing Company (TSMC)**.

The important points to consider for full-custom layout designing in this dissertation are:

1. keeping in mind the design rules of CMOS TSMC 65 nm technology;
2. less occupied area means lower cost;
3. short interconnections wires in memory array by optimizing the interconnection wires at single memory cell design level to decrease the parasitic resistance and capacities in array of SRAM block;
4. try to reach a symmetric design, in order to have a higher final robustness.

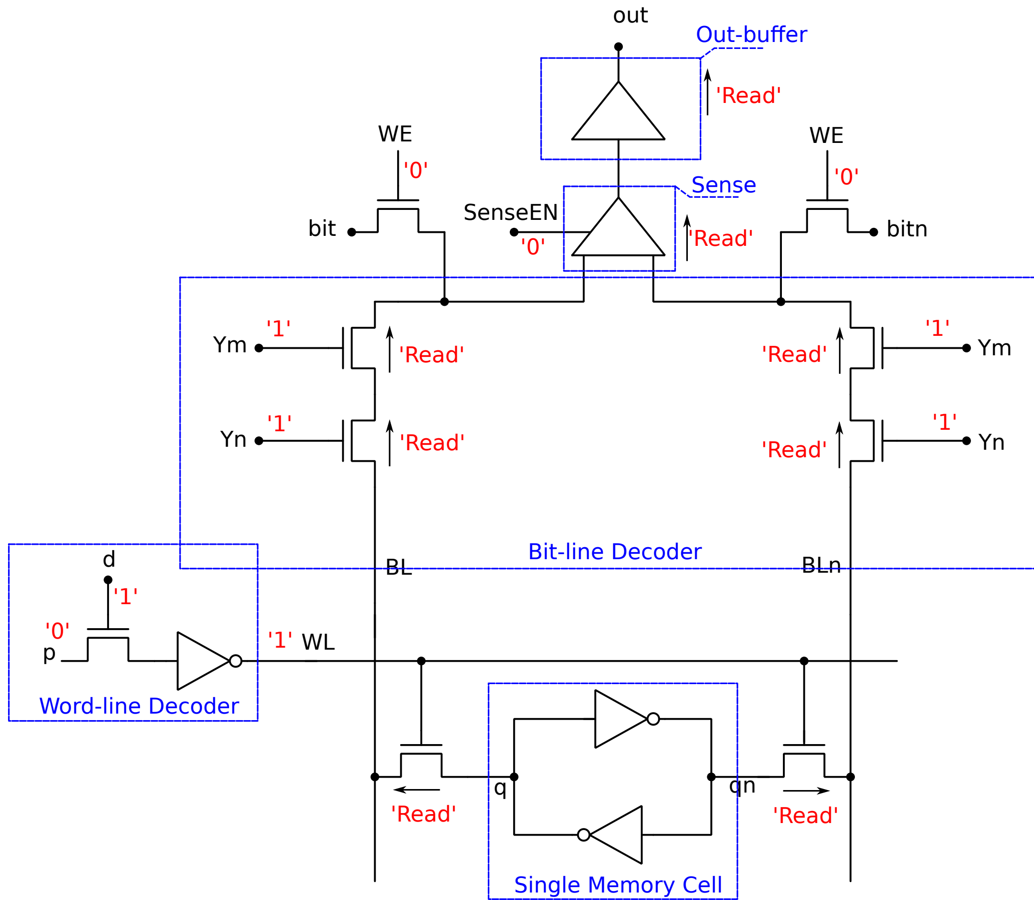

Fig. 4.11: Schematic of Read operation.

For achieving the items 2 and 3, the **Euler Graph** method is used to design stacked transistors. Stacked transistors occupy less area and help to simplify the placement and routing of the final design to have shorter interconnections wires.

4.2.1 Euler Graph

The Euler graph contains vertex and arcs, and each vertex connects a couple of arcs. The Euler graph of DICE SRAM single cell is made with a pull-up part for n-type transistors and a pull-down part for p-type transistors. Each node of circuit corresponds to a vertex and every transistor corresponds to an arc. The arcs connect the vertexes corresponded on drain and source terminal of represented transistor. Each arc has the same name as the transistor gate.

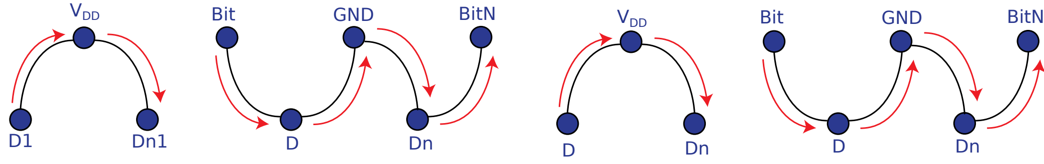

Fig. 4.12: Euler Graph of DICE single memory cell layout design: the letters correspond the nodes with the same name in schematic view of Figure 4.2.

After finding the Euler graph of specified circuit, the next step is finding one or more routes which cross all arcs just once and vertexes at least once. The cross direction is not important because the MOS transistors are symmetric.

Figure 4.12 shows the Euler graph of DICE single memory cell which is used to have the final layout design. The labels represent the same schematic nodes of DICE single memory cell in Figure 4.2.

4.2.2 Single Memory Cell Layout: First Version

Figure 4.13 shows the layout of four juxtaposed single memory cells in a memory array of the first design version. Blue layer is gate, red layer is active area of P and N doped substrate and green is the contact with interconnection metals. Single memory cell layout can be vertically divided into two symmetric blocks, and every block is related to one of identical part of DICE SRAM architecture. The polarization contact of the substrate and of the n-walls are very important for radiation hardened design, therefore the design is optimized to achieve a trade-off between the minimum of whole layout area with bigger polarized active area and more interconnection between different layers of metals and active area. The different transistor gates which have the same signal are connected by poly-silicon layers instead of metal layers. In Figure 4.13, cell 2 is mirrored of cell 1 horizontally while cell 1 and cell 3 are vertically mirrored. Every single memory cell layout contains due identical parts and two identical bits are stored in each parts. Single memory cell design is made in a way to achieve a compact layout of memory array.

4.2.3 Single Memory Cell Layout: second version

Low supply voltage (1.2 V) in 65 nm CMOS technology avoids latch-up in memory cells at room temperature, therefore this problem is not considered

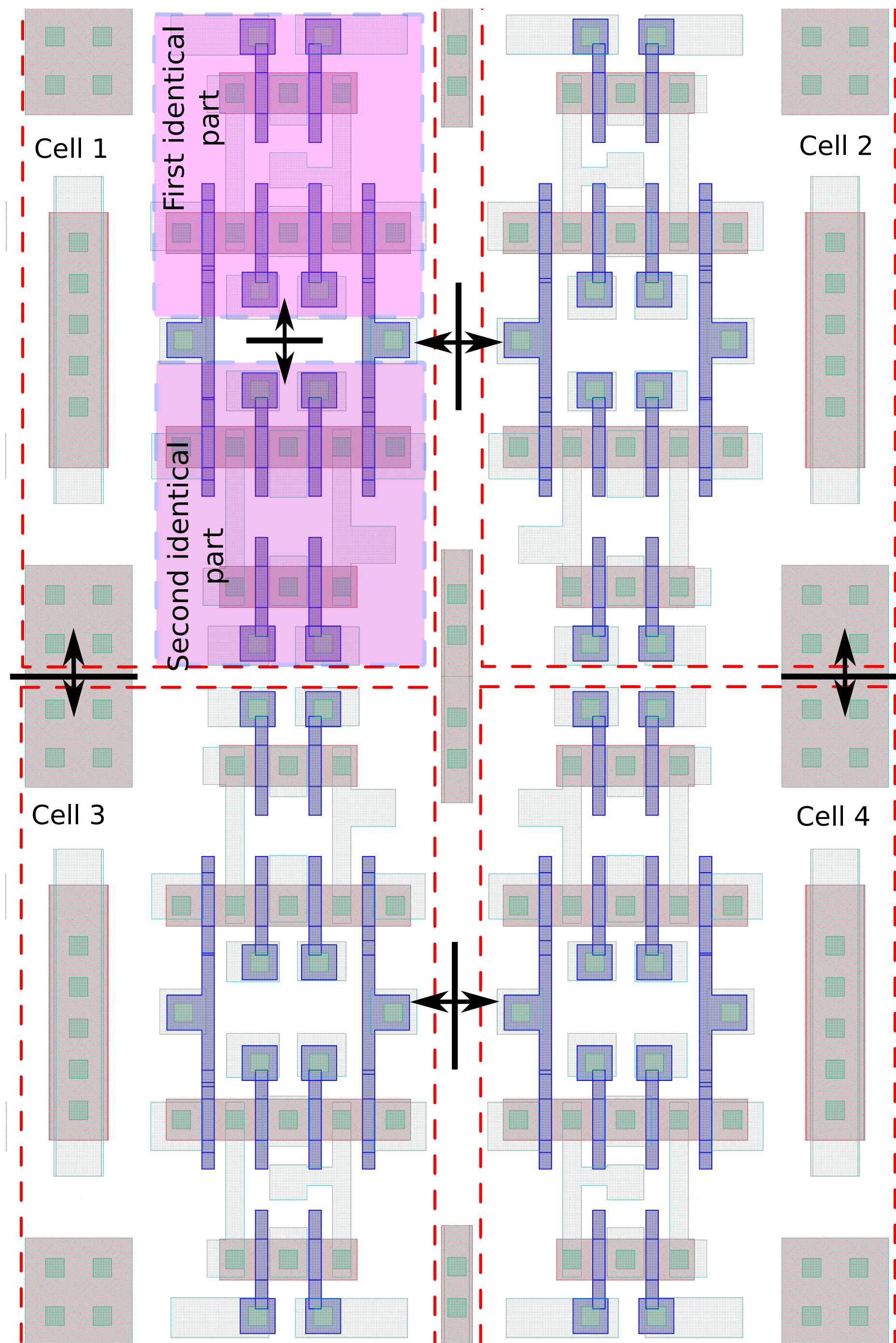

Fig. 4.13: Four single memory cell layout in array of memory.

in the first version of single memory cell layout design. However, some

studies demonstrate that at higher temperature (more than 80 °C) latch-up Event Upset is still a problem, even for CMOS technologies with low supply voltage [33].

In order to mitigate the risk of latch-up at high temperature, the second version of DICE SRAM is designed and studied in this dissertation. To come over this problem guard-rings are included in design, while single transistors has the same dimension and shape as the first design version (Figure 4.14). The guard-rings are the biasing regions for the substrate and for the n-wells, and they surrounds the stacked transistors. The currents generated by particles in the reversed biased p-n junctions find a low-impedance path towards a constant voltage source in guard rings. This mechanism prevents the latch-up phenomena.

The comparing of radiation effects in two different versions of the same architecture, with and without guard rings, gives the possibility of a general understanding of the latch-up effect impact on memory cells in CMOS 65nm technology with 1.2 V supply voltage.

4.2.4 Single Memory Cell Layout: third version

DICE architecture increases the tolerance of memory cell to SEU, but also Multiple Event Upset (MBU) is also an important issue to deal in CMOS memories application. In version 3 of DICE single memory cell design, the idea of increasing the distance between two identical parts of the same single memory cell is realized by combining two interleaved half-cells in array of memory (Figure 4.15).

With this design approach the distance between two identical parts of each cell is increased to 5 µm which is double compared to the first design version. The third design version occupies the same area as the second version and the approach is achieved just with more complex wire routing. Therefore this design is hardened to MBU in addition to SEL and SEU.

4.2.5 Word-line decoder

Figure 4.16 shows the layout of two steps word-line decoder which is integrated in the first version of single memory cell, while a second design with guard ring was also developed (Figure 4.17) to be integrated in the second and third versions of memory cells. The designs are polarized in efficient way with big area of polarization compared to the whole design area. The inverter which

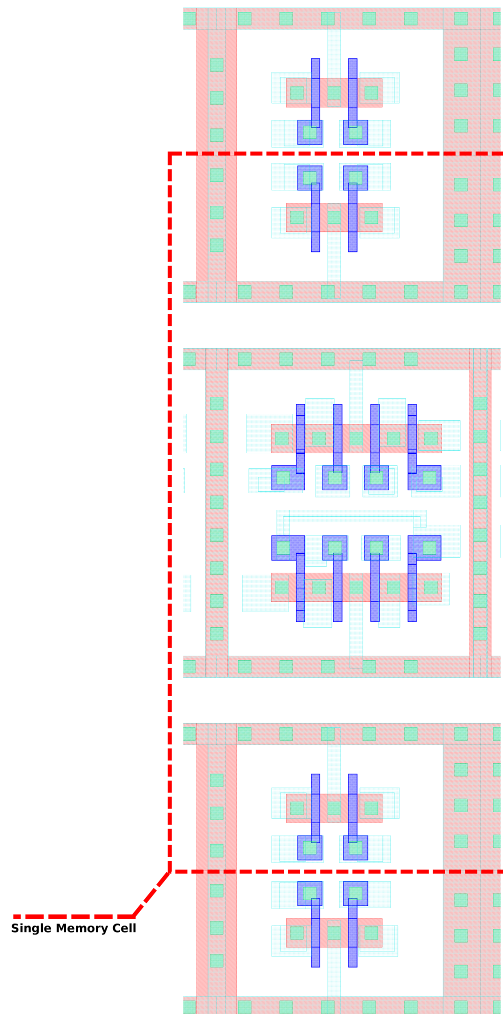

Fig. 4.14: Second version of memory cell layout.

drives the word-line wires in the last step is made with transistors with wider channel because the world-line wires are as long as horizontal length of final memory block.

4.2.6 Bit-line Decoder

Figure 4.18 shows the bit-line decoder layout which is integrated in the first version of the single memory cell. Figure 4.19 shows the second design of bit-line circuit with guard ring included which is integrated to second and third versions of memory designs. Transistors with wider channel are used

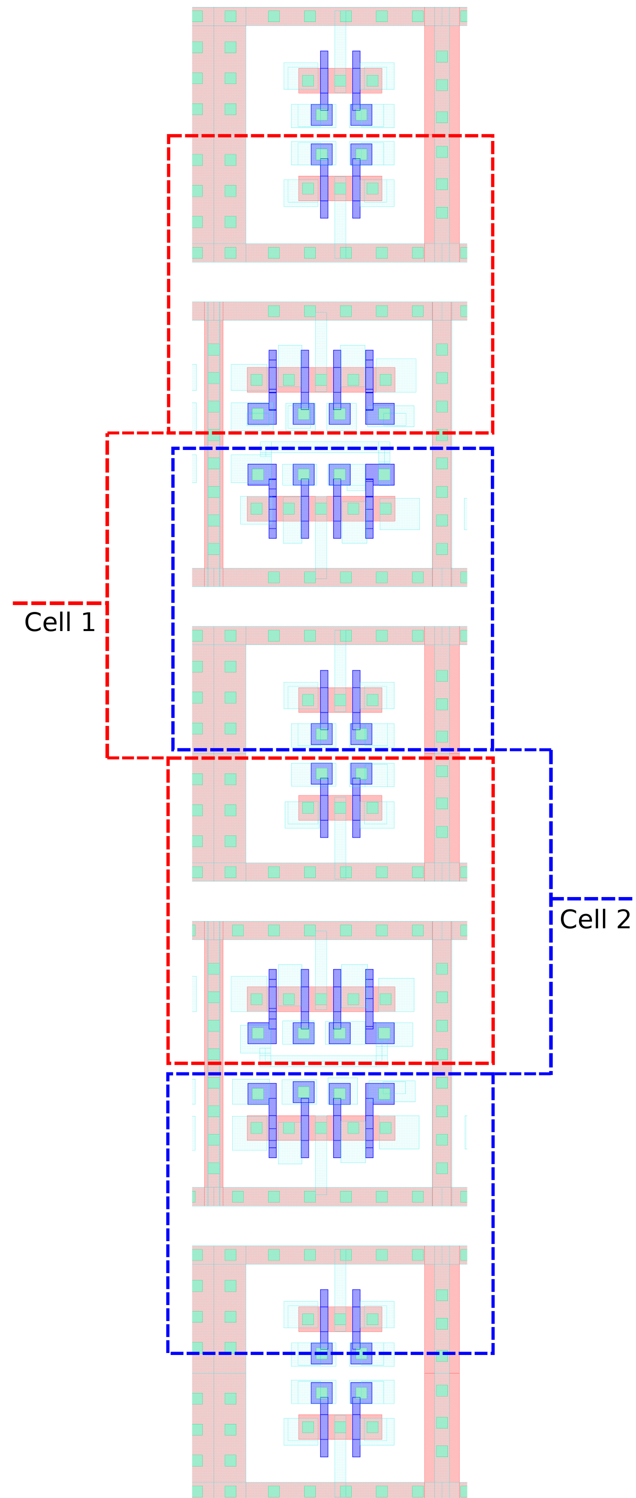

Fig. 4.15: Third version of single memory cell layout: two interleaved memory cells.

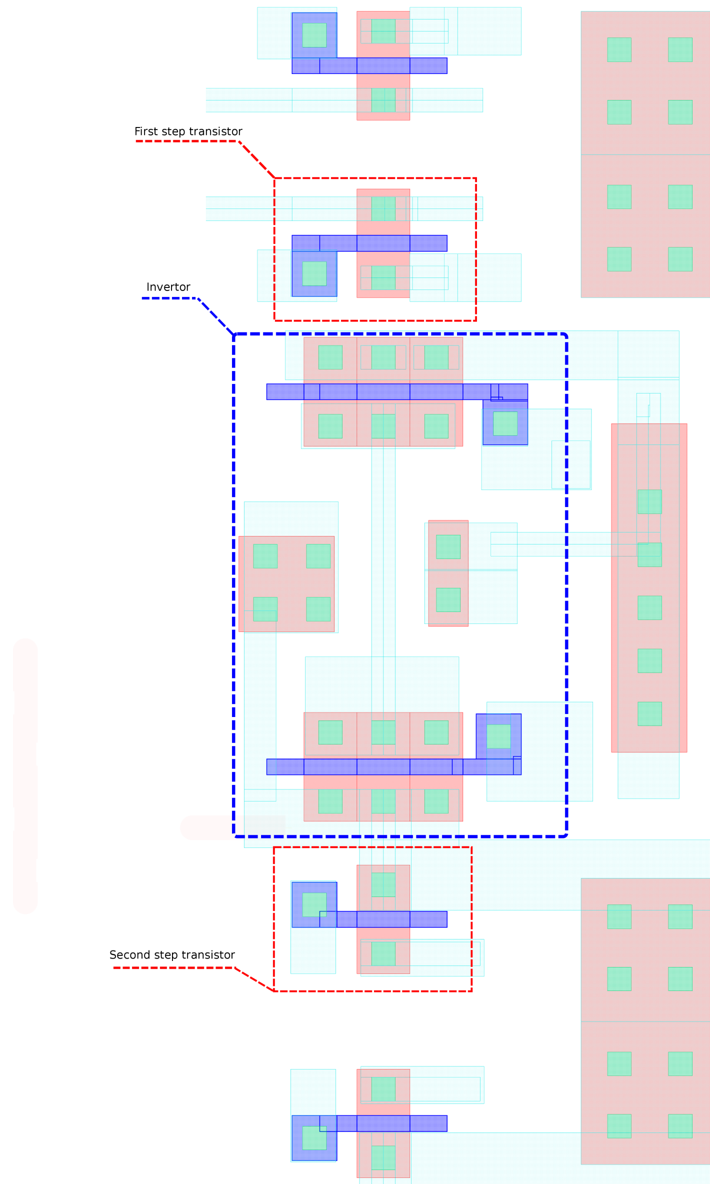

Fig. 4.16: Word-line decoder: first design without guard ring.

to drive the bit-line wires which are as long as vertical length of memory block. Long wire have high parasitic resistance and capacitance, therefore they cause a voltage drop and slow down the logic transistors.

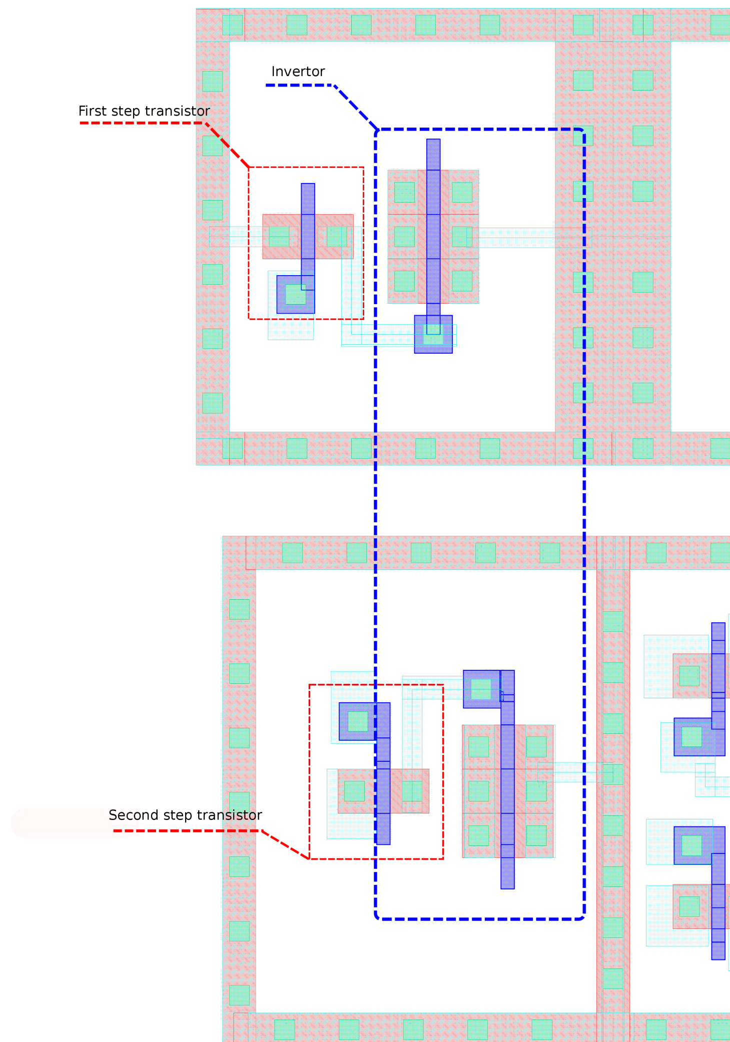

Fig. 4.17: Word-line decoder: second design with guard-ring.

4.2.7 Wire and Read Circuits

Figures 4.20 and 4.21 show the layout of the Sense and Equalizer circuits, discussed in section 3.1.4 and 3.1.5. These circuits are analog parts of memory block. The transistors of the equalizer circuit have a larger channel compare to other array transistors. These transistors should be able to pilot the voltage of all the bit and inverted bit-lines of memory array to half supply voltage value, after each Read and Write operation. Guard rings are included in both

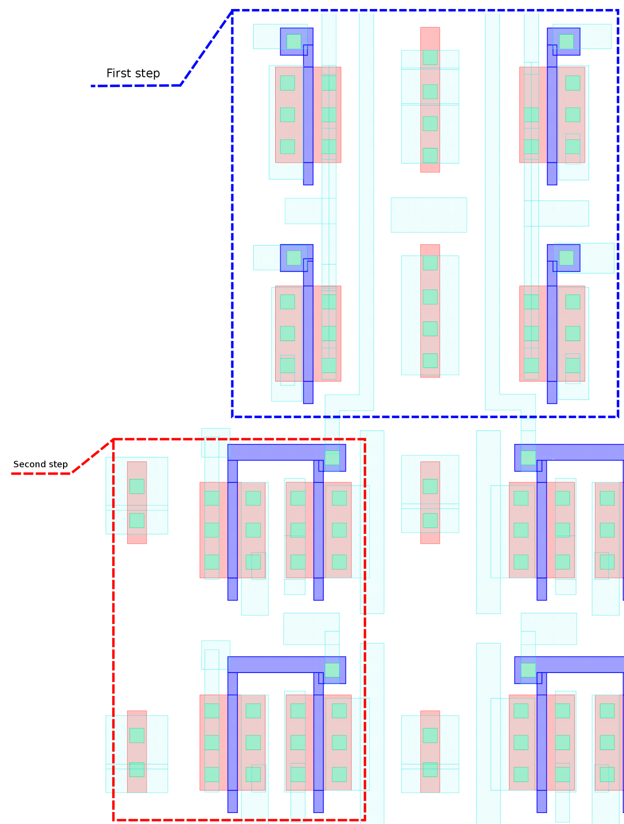

Fig. 4.18: Bit-line decoder: first design without guard-ring.

circuit layout designs.

4.3 Chip Prototype

The three versions of SRAM arrays, each of them with separate decoders and write/read circuitry, have been integrated and independently supplied and testable:

1. simple DICE (first version of design) to mitigate SEU;

2. DICE including guard ring (second version of design) to mitigate SEU and SEL;

3. interleaved DICE (third version of design), including guard ring to mitigate SEU, SEL and MBU.

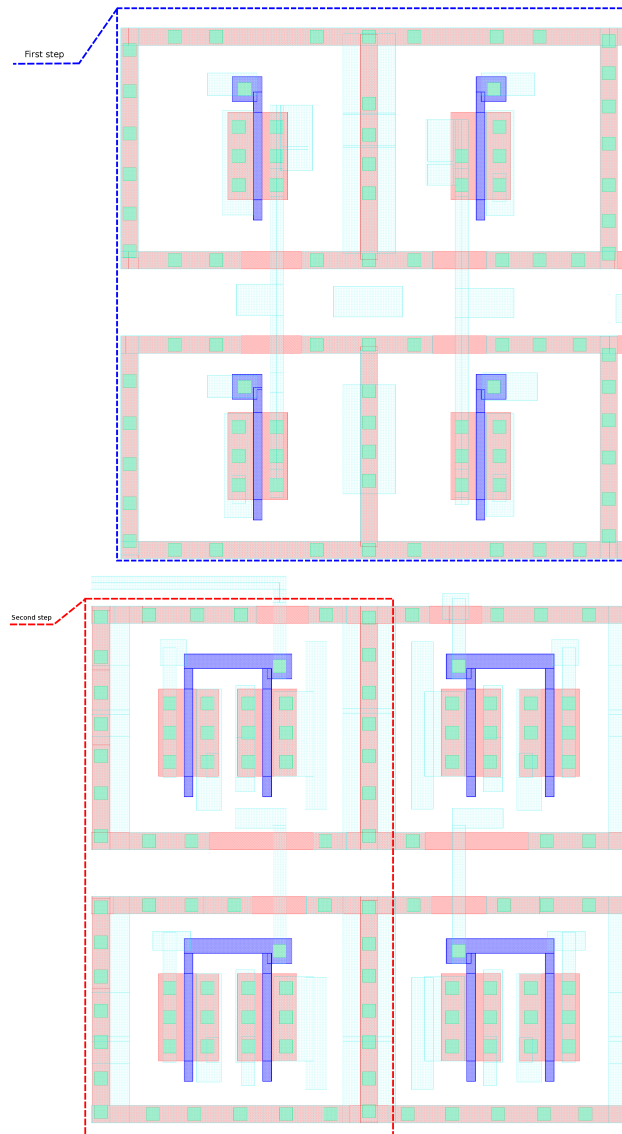

Fig. 4.19: Bit-line decoder: first design with guard-ring.

The three versions are integrated in a single prototype chip and submitted in TSMC foundry in CMOS 65 nm technology. The submission is supported by Italian National Institute for Nuclear Physics (INFN) in CHIPIX65 project, inside the RD53 collaboration.

The chip package is a QFN-80 with dimensions of 12 mm × 12 mm. The prototype includes also a SERDES block and single transistors for other activities of the CHIPIX65 projects. The SRAM blocks employed 46 pins of

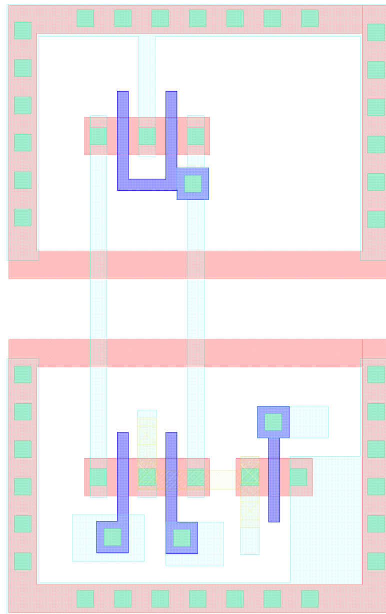

Fig. 4.20: Sense circuit layout.

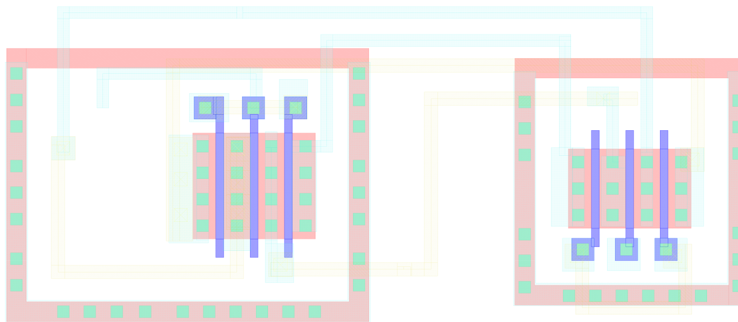

Fig. 4.21: Equalizer circuit layout.

the package:

- 16 address pins;
- 3 control pins of Write and Read circuits;
- 3 pins of Input data for three blocks;
- 3 pins of output data for three blocks;
- control signal of PAD's buffer;

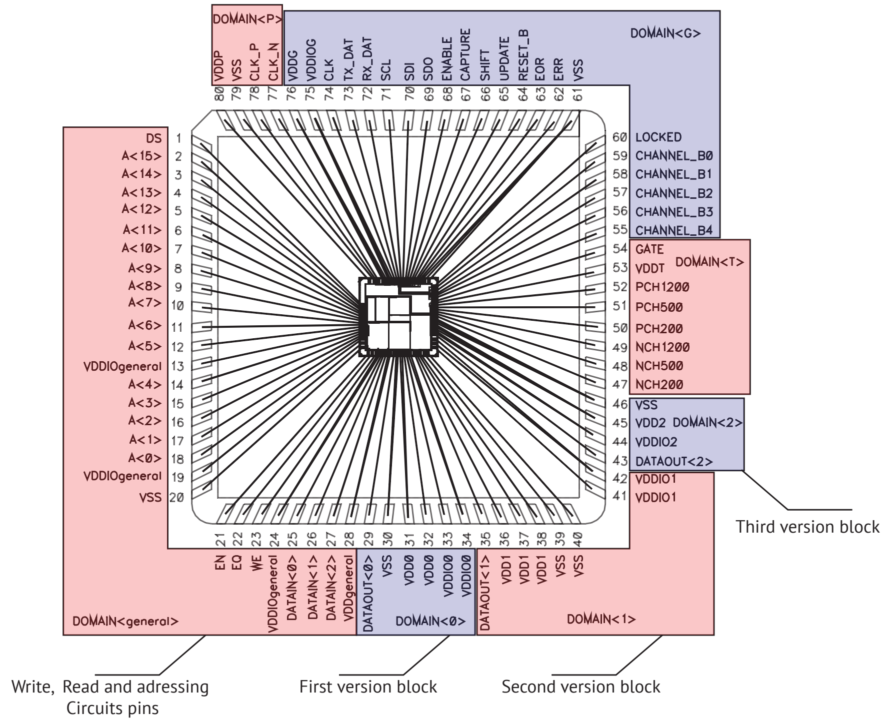

Fig. 4.22: Chip prototype bonding diagram.

- 7 pins for PADs supplying, connected together;
- 7 pins for core supplying which give the possibility of turning on and off the three blocks of memory separately;
- 5 ground pins, connected together (Figure 4.22 and 4.23).

The fabricated chip has an open package with a removable plastic cover on the top, to allow the die to be exposed to radiation in order to characterize the radiation tolerance of the design.

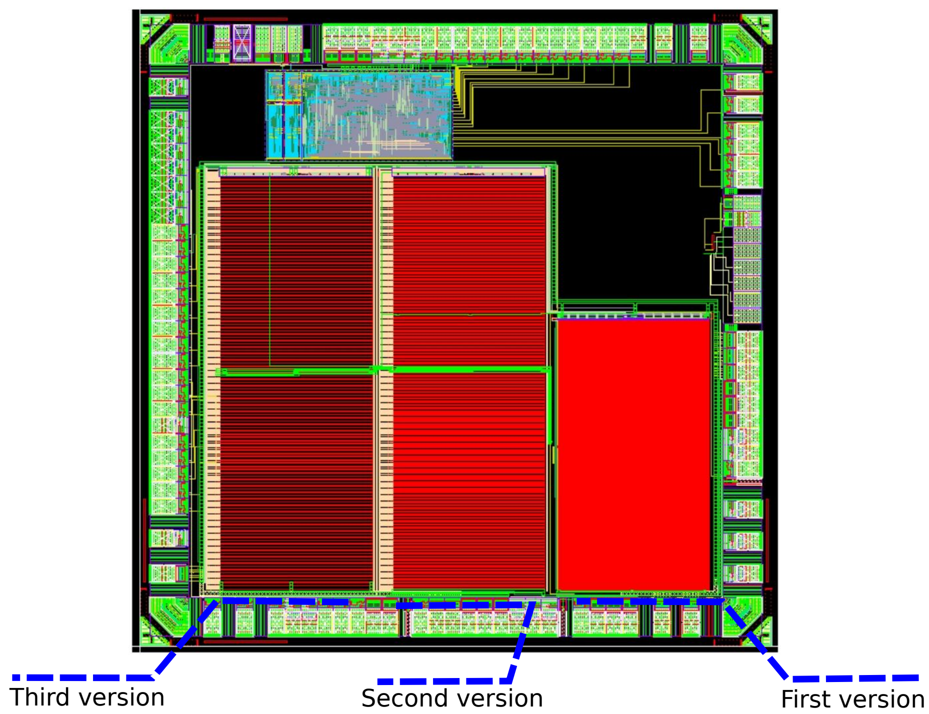

Fig. 4.23: Chip prototype layout: first version is hardened to SEU; Second version is hardened to SEU and SEL; Third version is hardened to SEU, SEL and MBU.

5. MODELING AND SIMULATIONS

The performance of an IC requires to be proven by simulation in realistic conditions before submission and fabrication. In fact, every IC layout contains parasitic components which affect the performance of IC, therefore the simulation of radiation hard SRAM block with parasitic components is presented in this dissertation.

Parasitic component extraction of radiation hardened SRAM block layout requires huge computation time and a prohibitive amount of computer memory. To over-come this problem, a new approach of simulation is developed in this dissertation.

Also the radiation effects on integrated circuits have been studied and simulated to confirm the radiation tolerance of layout design in this section. Fault charge injection method is used to simulate single event effect and a novel simulation method is developed to simulate total dose effects on radiation hard SRAM memory block.

5.1 Parasitic Extraction and Simulation

Simulation of integrated circuit layout design in worst-case condition is important and in the evaluation of performance of IC design in real condition and parasitic components need to be considered.

Calibre from Mentor Graphics gives the possibility of extracting the parasitic components from the layout design and, in the next stage, the extracted parasitic components can be integrated in the main circuit for worst-case condition simulation.

The extraction of parasitic components is a new challenge, because the layout of the memory array contains 64 k single memory cells and periphery circuits. The extraction of parasitic components of the whole memory block layout requires a heavy calculation process and an amount of RAM far exceeding the 128 GB installed on the computer used for the design. To

overcome this obstacle the amount of calculation was reduced by simulating only the most critical parts of the memory array.

In fact the bit-lines and word-lines are the longest wires of memory block and each of them is connected to several nods, therefore the signal at the end of these wires is strongly influenced by parasitic components of interconnection wires. Therefore single memory cells in the 4 corners of the array are the most sensitive parts of array to parasitic components disturbances.

A new layout of radiation hard SRAM is designed to apply this methodology of simulation (Figure 5.1).

This layout design included:

- 4 corner single memory cells;
- all single memory cells which have interconnection with bit-line and word-line of selected single memory cells in the angles of array;
- word-line and bit-line decoders;
- write and read circuits.

This design, compared to the original one, has a significant reduction of the number of circuit and parasitic components.

The simulation of related circuit of the schematic in Figure 5.1 which included the parasitic component of layout design is performed. The bits '1' and '0' are written alternatively in the corner single memory cells. After a short period of time the stored bits of the same cells are readout. The correct readout bits confirms the performance of SRAM block up to 100 MHz.

.

5.2 Total Dose Effect Simulation

Various research groups already made accurate investigation about Total Dose Effects on single transistor in different technologies of fabrication [34]. The majority of published studies are focused on:

1. changes in threshold voltage because of trapped charge in Si-SiO_2 surface and displacement damage on isolate oxide of transistors gate;

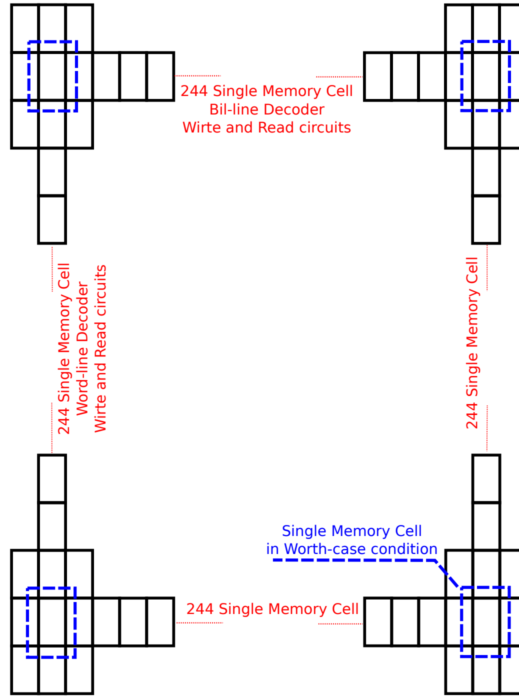

Fig. 5.1: Schematic of layout design for simulation with parasitic components. The simulation of 4 angles single memory cells is performed included all parasitic components of layout block.

2. leakage current: in ultra small CMOS technologies high flux of radiation cause radiation-induced degradation in Shallow Trench Isolation (STI) (Figure 5.2). This phenomenon significantly increases the leakage current of standby NMOS transistors. The impact of STI radiation damage on drain current can be seen in the plot of Figure 5.3 which shows the TID effect. measurements of 180 nm N-channel MOSFETs fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) [34].

Based on experimental results the leakage current in radiation test of single transistors in 65 nm CMOS TSMC technology is not remarkable compared to older technologies. The threshold voltage shift is still evident as predicted by the formula:

$$\Delta V_{ot} = -\frac{q}{C_{ox}}\Delta N_{ot} = -\frac{q}{\epsilon_{ox}}t_{ox}\Delta N_{ot} \tag{5.1}$$

where q is the elementary charge, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the oxide capacitance per unit area, N_{ot} is the density of trapped holes into the oxide, ϵ_{ox} is the dielectric constant of the oxide, t_{ox} is the oxide thickness. The threshold voltage

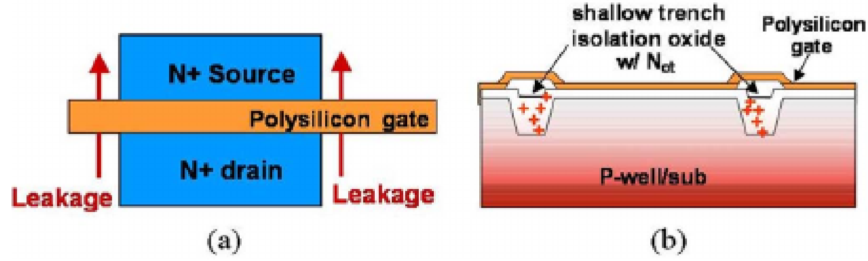

Fig. 5.2: (a) Illustration of drain-source leakage path in n-channel FETs and (b) its cause: oxide trapped charge buildup in the isolation oxide (from [35]).

shift has a linear correlation with thinness of oxide gate therefore in 65 nm technology, it is not negligible because of the very thin gate oxide.

Moreover, the relevant change in drain current in active-region is a new phenomena which is evident in experimental results.

After understanding how the characterization of single transistors changes in time when they are exposed to radiation, it is very important to use these results at the level of circuit layout design to increase the radiation tolerance of integrated circuits. In this chapter, a simple physical model developed to explain how the performance of single transistors changes under radiation. This model was developed is described to predict the whole integrated circuit performance after different amount, of total dose of radiation.

The change of drain channel current and threshold voltage of single transistors in radiation tests depends on: transistor fabrication technologies, transistor channel dimension, temperature, and total dose of radiation. However these variables are different for PMOS and NMOS transistors. Figure 5.4 shows some of radiation test results on single MOS transistors in 65 nm TSMC technologies [23].

The main transistor parameter which has an evident change in the graph of drain current vs gate source voltage is the transconductance. After 1 Grad of total dose radiation, NMOS transistors lost 70% and PMOS transistors lost almost 95% of drain current.

The drain current vs gate-source voltage in saturation region ($V_{ds} > V_{gs} - V_{th}$) with ideal functionality can described with 5.2:

$$I_D = K \cdot (V_{gs} - V_t)^2$$

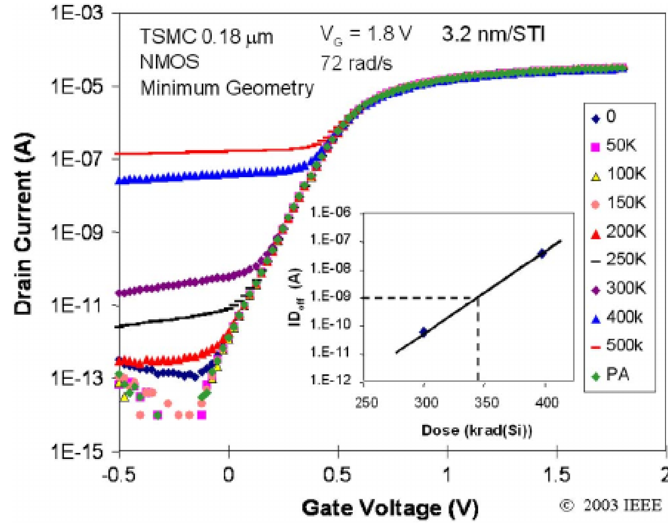

Fig. 5.3: Impact of STI radiation damage on the current-voltage characteristics of NMOS transistors fabricated in TSMC 0.18 nm CMOS (from [35]).

Based on hypothesis of change the transconductance factor in linear way vs Total dose of radiation, Formula 5.2 can be re-formalized to include the total dose effect 5.2:

$$I_D = K \cdot (1 - g_{n,p}) \cdot (V_{gs} - V_t)^2$$

In the red part of formula 5.2, g_n for NMOS transistor and g_p for PMOS transistor describes the loss in transconductance factor after the exposure to the radiation. The g_n and g_p can get extracted from numerical analysis of experimental measurement of drain current vs gate-source voltage.

The additional part of Formula 5.2 can be simulated by adding a current-controlled current source in parallel to the single transistor in the schematic of Cadence simulator (Figure 5.5). The g_n and g_p factors of current generator are set as variables in simulator and they varies between 0 to 1 based on total dose radiation.

This method can be extended to circuit level of Total Dose Effect simulation. The steps are:

- generating a symbol of circuit in the figure 5.5 for PMOS and NMOS transistors. The channel length of transistor and the gain factor of current generator are given as variables in the netlist of simulator;

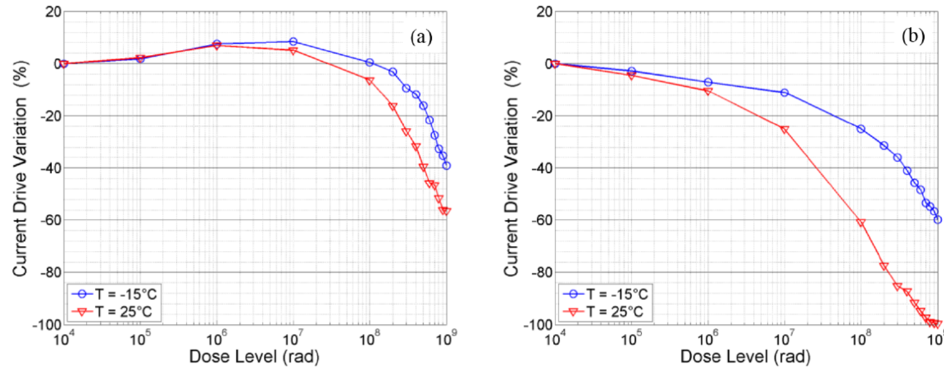

Fig. 5.4: Current variation versus the TID level for minimum size transistor with 1.2 V supply voltage (a) 120 nm/60 nm NMOS device (b) 120 nm/60 nm PMOS device (from [23]).

- changing the schematic of the original circuit in simulator by replacing the single transistor symbol of Cadence standard library with the symbol generated above;
- setting-up the channel length factor of single transistors based on circuit architecture and g_n, g_p factors based on total dose radiation;
- processing the simulation in the same conditions of original circuit.

The radiation hard SRAM block was simulated using this methodology. With different values for g_n and g_p independently. The bit '1' is written in a selected single memory cell of array and read-out after 70 ns of time. The graph of Figure 5.6 shows the readout signal of memory block for different simulation processes, each with different values of g_n and g_p.

It is evident that for some values of g_n and g_p the readout voltage has a low voltage value which does not correspond to the stored bit '1'. It means for those values of g_n and g_p and the related total dose of radiation, the single memory cell loses the stored data and therefore the memory block is not functional any more.

The plot of Figure 5.7 shows a summary of the simulation results of SRAM block performance in a schematic way for different total dose of radiations. The vertical and horizontal axes represent the g_n and g_p factor values and the red area represent where the simulations show the efficient functionality of radiation hard SRAM block.

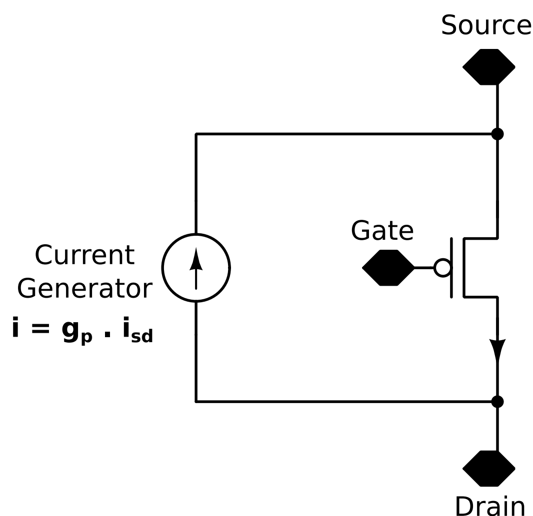

Fig. 5.5: Schematic of total dose effect simulator circuit.

The single transistors are submitted to the fabrication in the same prototype of SRAM blocks in 65 nm TSMC technology in order to measure the experimental values of g_n and g_p for different total dose of radiations. Once these transistors will be characterized under different total dose of radiations, the g_n and g_p factors can be determined from the test results of source-drain current vs gate-source voltage for different total dose of radiations.

5.3 Single Event Effect simulation

SEE's are directly related to the amount of charge collected in the sensitive nodes of ICs. The interaction between particles and CMOS devices has been investigated in the past years [2, 36, 37].

The two-dimensional (2-D) and three-dimensional (3-D) numerical simulations are already developed to describe the physics of charge collection phenomena in CMOS devices [38]. For this purpose, commercial software based on 3-D models are available, however it requires detailed information about fabrication parameters which are not commonly accessible.

5.3.1 FISAR approach

The technique used in this dissertation to simulate the interaction between particles and p-n junction is based on drift-diffusion model. This model

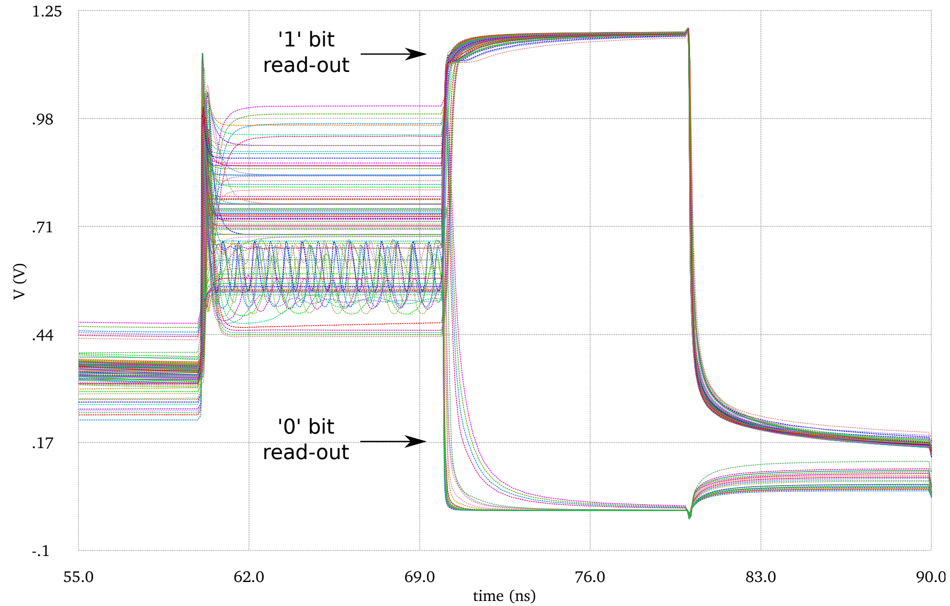

Fig. 5.6: Simulation of readout signal of storage bit '1' in memory array. Each plot shows the simulation result for a different value of g_n and g_p.

is based on Boltzmann transport equation which describes the statistical distribution of particles in a fluid.

The commercial software used to design ICs are based on 2-D (planar) environments (e.g., Cadence Virtuoso). Designers draw 2-D polygons in different layers which are used to fabricate lithograph to build real 3-D layers.

The interaction between a particle and ICs strongly depend on the vertical structure of ICs and therefore a high level accurate three dimensions model is needed to describe non-orthogonal (with different incidence angles) particle strikes. Figure 5.8 shows a non-orthogonal particle collision with an IC. This particle ionizes several p-n junctions [39].

A particle may ionize different regions with different charge density values. The silicon foundries do not always release information about fabrication process (e.g., layer thickness, doping profiles, etc.) and performing a 3-D simulation by only a set of 2-D parameters provided by the silicon foundry is not easy.

For a simulation at the electrical level, formula 5.2 is the most used description of the current generated by the strike of particles in CMOS circuits.

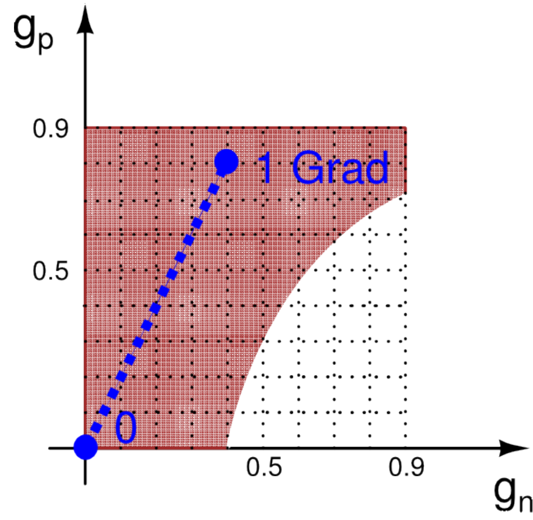

Fig. 5.7: The radiation hard SRAM block simulation results with different value of g_n and g_p: the red area shows functional results. The blue line indicates the variation of the conductance parameters from 0 to 1 Grad of total dose.

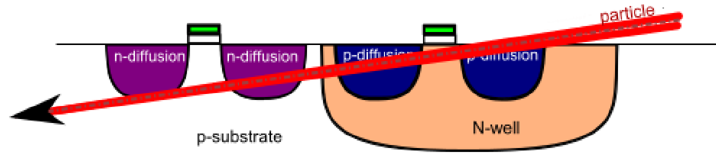

Fig. 5.8: Non-orthogonal particle collision with an IC

$$i(t) = \frac{Q}{t_1 - t_2} \cdot (e^{-t/t_1} - e^{-t/t_2}) \tag{5.2}$$

where Q is the total injected charge, t_1 is the collection time constant of the junction, t_2 is the time constant for initially establishing the ion track.

Moreover the striking of a particle in CMOS technologies with high scaled dimension of transistors can influence more that one node, simultaneously. For this reason an alternative model with charge injection at circuit level is used in this dissertation [40].

The model is based on the multiple injections of parasitic currents by means of voltage-controlled current sources. The figure 5.9 shows the schematic of the proposed model assuming that there are four nodes ionized by radiation.

In the Figure 5.9 the holes are injected in four different p-n junctions and the number of junctions can change depending on the particle hit position.

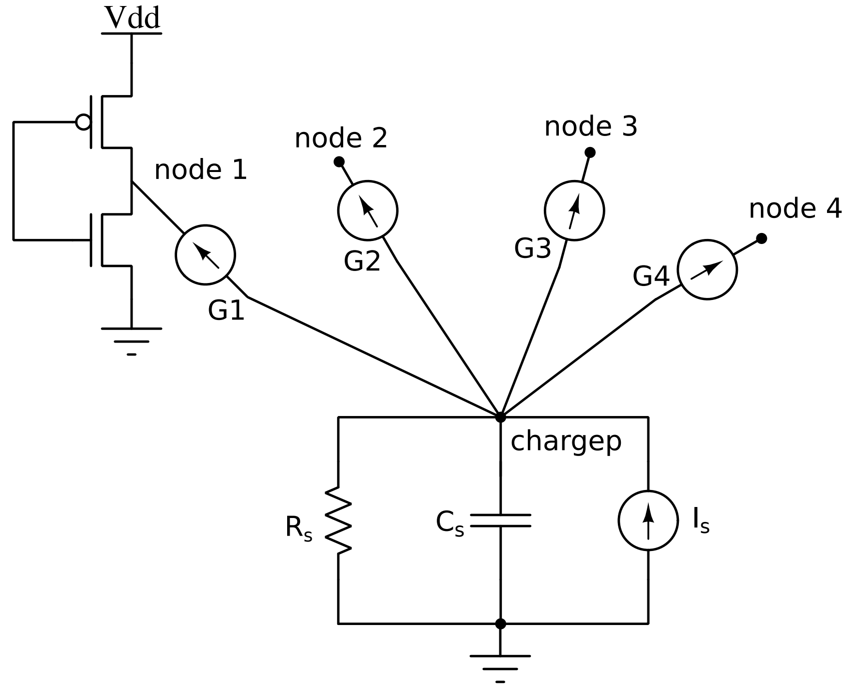

Fig. 5.9: Injection model for 4 differnet p-diff/n-well junctions.

Total charge is injected by means of the independent current generator I_s in the node `chargep`. The I_s generator a current similar to a Dirac's delta with an area equal to the value of total injected charge. Therefore Dirac's delta time correspond to the single event time. The *Voltage-Controlled Current Sources: VCCS (G1, G2, G3 and G4)* in the schematic of Figure 5.9 have the same rise time of generator I_s.

The current generated by the VCCS's is described with this formula:

$$i_n(t) = k_n \cdot V_s \cdot V_n \tag{5.3}$$

where V_n is taken between target node n and the voltage power supply of bulk, k is used to split the total charge in different junctions, depending on the hit position and on the geometrical shape of the junction. To inject electrons in p-n junctions we have to use a negative Dirac's delta and take V_n between ground and the target node. The recombination time is given by $\tau = C_s \cdot R_s$.

FISAR: Fault Injection Simulation and Analysis for Radiation hardening is an approach which employs the technique of injection of parasitic currents at the circuit level to simulate the interaction between a single ionizing particle and the p-n junctions within any region of the IC. The FISAR approach is

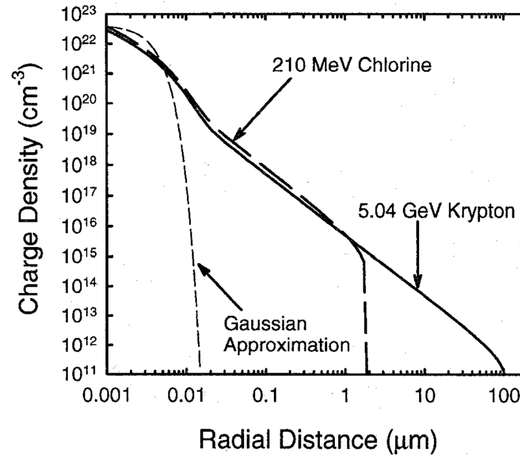

Fig. 5.10: Injection model for 4 different p-n junctions.

employed to validate SEU tolerance of radiation hardened memory block in this dissertation.
Moreover the nature and energy of the particle is important because the extension of the ionization column may range from some nano-meters to some micro-meters, as shown in figure 5.10 [41].

5.3.2 Calculation of charge collected within each box

The assumptions are that the p-n junction is the only part of layout that collect the generated parasitic charge by particle strike and the HEP density distribution is simple 2-D gaussian. Therefore the colliding angle of the particle is assumed orthogonal to the IC surface and ionization outside the $5 \cdot 5$ array is negligible. The total charge spreads among a cluster of 21 layout boxes.

It is possible to find a relation between charge deposition and Linear Energy Transfer (LET): in silicon, a LET of $97\,\mathrm{MeV{\cdot}cm{\cdot}mg^{-1}}$ corresponds to a charge deposition of $1\,\mathrm{pC{\cdot}\mu m^{-1}}$. Therefore based on particle energy, the particle species and the target material, it is possible to calculate the total value of parasitic charge that is generated.

The total value of generated parasitic charge will be divided among boxes with (5.4):

$$Q_{b,k} = Q_{tot} \cdot w_{b,k} \tag{5.4}$$

where Q_{tot} is the total charge and $w_{b,k}$ is the weight of each box.

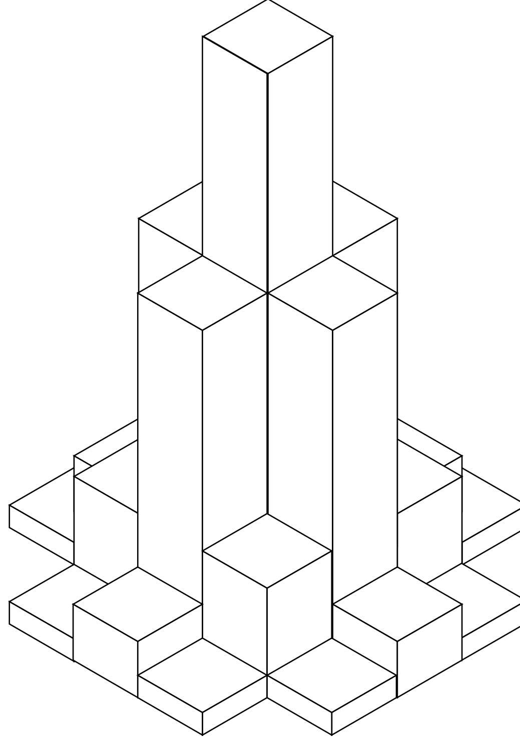

Fig. 5.11: 3D discrete gaussian distribution of charges.

For each box, the generated charge $Q_{b,k}$ is divided between nodes, in proportion to their junction capacitance. To obtain the p-n junction capacitance of each box node, area and perimeter values are multiplied with the unit junction capacitance specified in the transistor models. The amount of charge $Q_{n,b,k}$ collected by the node n inside the box b referring to a window k is:

$$Q_{n,b,k} = Q_{b,k} \cdot \frac{C_{b,n}}{\sum_{m \in b} C_{m,b}} \tag{5.5}$$

where $Q_{b,k}$ is the charge generated in the box b in the window k, $C_{b,n}$ is the capacitance of the node n inside the box b, and the sum is calculated for all nodes lying within the box b. The calculation to find the portion of total charge of each node $Q_{n,k}$, is repeated for each node n and for each box inside the collision area.

The irradiated part of single cell memory layout include more sensitive nodes of the SRAM single memory cell circuit and the SEU simulation performed in worth-case condition. The internal node of due latches in DICE SRAM architecture are more sensitive nodes because the change of voltage in

these nodes can cause the flipping of storage bit.

5.3.3 FISAR Simulation Procedure

FISAR simulation method is used to estimate the singe effects tolerance of radiation hard SRAM blocks. The simulation describes the collision of a 210 MeV Chlorine ion to radiation hard SRAM block. The total charge of 1 pC is generated by Chlorine ion in Silicon target of SRAM block. The most sensitive area of a single memory cell of SRAM block that contains more nodes is selected as strike point for the particle. The hypothesis is that the generated charge is dispersing in an area of 1.94 µm diameter within a 5×5 box in 3-D gaussian distribution.

The figure 5.11 shows schematically the charge dispersion distribution of collision area.

The charge that is generated in each box because of n-diffusion and p-diffusion is divided in transistor nodes and can be calculated using (5.5). The p-n junction capacitance of each node is given by:

$$C = (C_j \cdot A) + (C_{jswg} \cdot P_g) + (C_{jsw} \cdot P_a) \tag{5.6}$$

where A is the geometrical area of the diffusion region, P_g is the perimeter for the diffusion region along the poly-silicon gate and P_a is the perimeter for diffusion region that is not along the poly-silicon gate. C_j is the unit capacitance for area diffusion. C_{jswg} is the unit capacitance for perimeter diffusion along the poly-silicon gate. C_{jsw} is the unit capacitance for perimeter diffusion not along the poly-silicon gate. It is remarkable that in advanced CMOS technologies as TSMC 65 nm the capacitance of gate perimeter has a higher value compare to the other kinds of junction capacitance.

The next step is to implement the FISAR simulation in circuit-level simulator (e.g., SPICE, Spectre). Therefore a Polynomial Voltage Controlled Current Source (PVCCS) generator is added to each circuit node inside the ionized region. These current generators are labeled `Gn` and the tool adds to the Netlist a node `chargen` which stores the total charge to inject in p-sub/n-diff junctions and a node `chargep` which stores the total charge to inject in p-diff/n-well junctions. The total charge are stored by means of a capacitor `Csn` (for p-sub/n-diff juctions) and a capacitor `Csp` (for p-diff/n-well junctions). As it is explained before, the diffusion time is chosen by means of independent current generator which generates a current impulse that is

ideally a Dirac's delta. In the netlist the delta is modeled as a short triangular pulse with a duration of 20 ps. The beginning of the pulse matches the start of the Single Event Effect. An example of netlist is:

```
Csn (chargen 0) capacitor c=100f
Rsn (chargen 0) resistor r=1G
Isn(0 chargen) isource type=pulse val0=0 delay=75n \
rise=10p fall=10p width=0 val1=-1.000000e-001period=1
Csp (chargep 0) capacitor c=100f
Rsp (chargep 0) resistor r=1G
Isp(0 chargep) isource type=pulse val0=0delay=75n \
rise=10p fall=10p width=0 val1=-1.000000e-001period=1
G0 (chargen net20 chargen 0 net20 0) pvccs \
gain=0.093473 coeffs=[ 0 0 0 0 1 0]
G1 (chargen net15 chargen 0 net15 0) pvccs \
gain=0.033179 coeffs=[ 0 0 0 0 1 0]
G2 (chargen Y chargen 0 Y 0) pvccs \
gain=0.063027 coeffs=[ 0 0 0 0 1 0]
G3 (chargen VDD chargen 0 VDD 0) pvccs \
gain=0.092545 coeffs=[ 0 0 0 0 1 0]
G4 (chargen VSS chargen 0 VSS 0) pvccs \
gain=0.248775 coeffs=[ 0 0 0 0 1 0]
G5 (chargep net03 chargep 0 net03 0) pvccs \
gain=0.081435 coeffs=[ 0 0 0 0 1 0]
G6 (chargep VSS chargep 0 VSS 0) pvccs \
gain=0.085565 coeffs=[ 0 0 0 0 1 0]
```

5.3.4 FISAR simulation results

Simulation of single event effect with FISAR approach is performed for the radiation hardened SRAM block.

The figure 5.12 shows the layout of a single DICE memory cell. The red area is the collision area of a 210 MeV Chlorine ion. The extension of the ionization effect is approximated to 1.94 µm. The array of red boxes (called window) corresponds to the ionization region and the intensity of red color represent the portion of injected charge of each box respect to total charge injected due to ionization effect.

The plot in the figure 5.13 shows the simulation results of SEU tolerance of

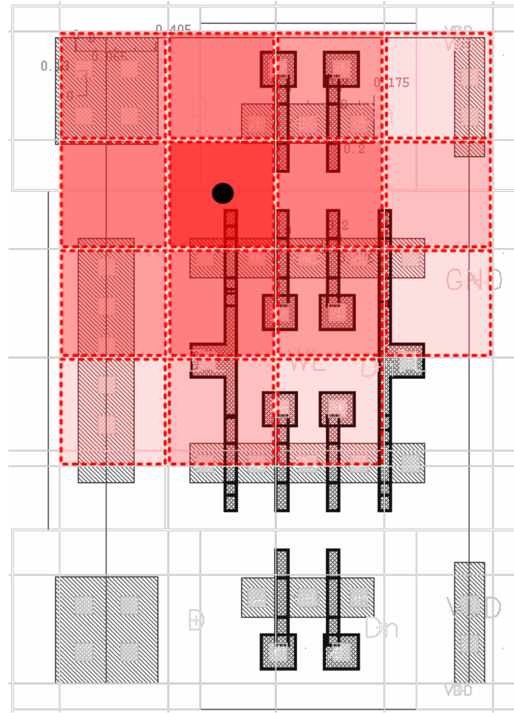

Fig. 5.12: Ionized charge distribution from the interaction of a particle with single memory cell: the intensity of the red color indicates the level of charge density.

radiation hard SRAM block. In the plot of simulation results the graphs have the same color as their related nodes in the schematic in the figure 5.13. The voltage value at node D and Dn are equivalents to storage bit and negative bit in one of tow identical parts of DICE SRAM cell and the voltage value at node D1 and Dn1 to other identical part. As explained in Chapter 2, DICE SRAM cell in stable condition has two identical parts with same storage bit and their related nodes have the same logic values. The plot of figure 5.13 shows that at the collision time (2900 ns) the voltages of all nodes start to change because of single event effect. The voltage in node D1 goes down and crosses the voltage of node D1n, therefore the storage bit ‘1’ in one identical part of DICE SRAM cell is changing to bit ‘0’. At the same time the node D and Dn voltage related to other identical part of DICE SRAM cell is changing but the voltage of nodes D and Dn are not crossing, it means the storage bit is still ‘1’, after 3 ns the voltage value of nodes of both identical parts of DICE SRAM return to the initial value. The reason is that the change of the

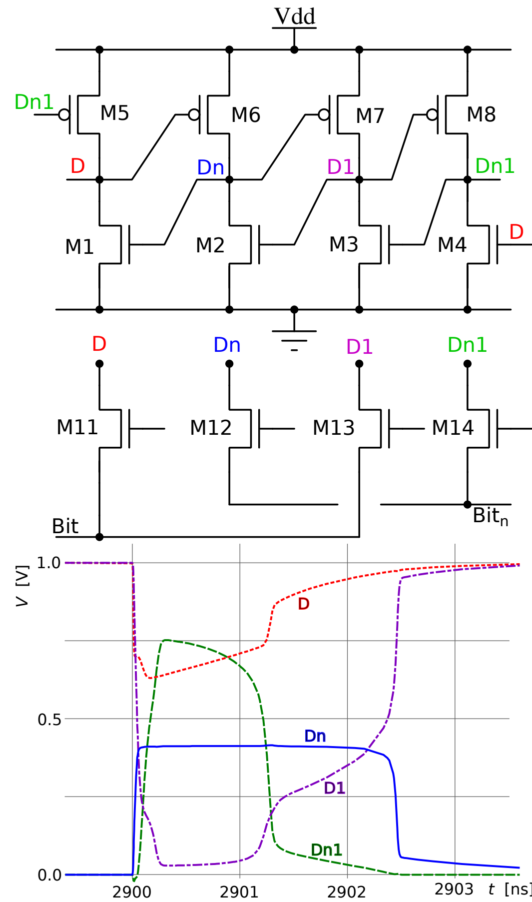

Fig. 5.13: SEE simulation on single memory cell layout

bit stored into a DICE single memory cell requires the change of bit in both parts simultaneously, which actually is not occurring during the simulation. The simulation results of single event effect from FISAR technique shows that the radiation cause a single event transient in a single memory cell of block and no single event upset occurs and it confirms the high level of radiation tolerance to single event upset.

6. CHARACTERIZATION

The next step after submission of the SRAM prototype is to develop a test system to characterize the prototype. In additional to the test in laboratory environment, another test under radiation will be performed to characterize radiation tolerance of design to Single Events Effects such as SEU and SEL, and Total Dose Effects.

6.1 Test Set-up

The developed test set-up has mainly three parts:

1. Mother-board with FPGA.
2. A passive board where SRAM prototype chips are assembled and fixed on (Figure 6.1).
3. An intermediate board between mother-board and the passive board (Figure 6.2).

A KINTEX-7 FPGA is implemented by VHDL firmware on a XILINX mother-board. The FPGA sends and receives data to the chip and control different functions during the prototype test. The on-board buttons of mother-board are employed to change the function modality of the chip. Radiation test of the prototype with this approach can be done without exposing the mother-board and the PC to the radiation beam.

The radiations can damage electronic components of mother-board such as FPGA and cause malfunction. Therefore the mother-board should be kept out of radiation environment during the test of chip prototype, exposed to the radiation in the vacuum chamber.

The plastic package of chip prototypes prevents the radiation to reach the chip and make impossible to characterize the chip with radiation effects. Therefore the plastic package of SRAM prototype chip is not closed and the

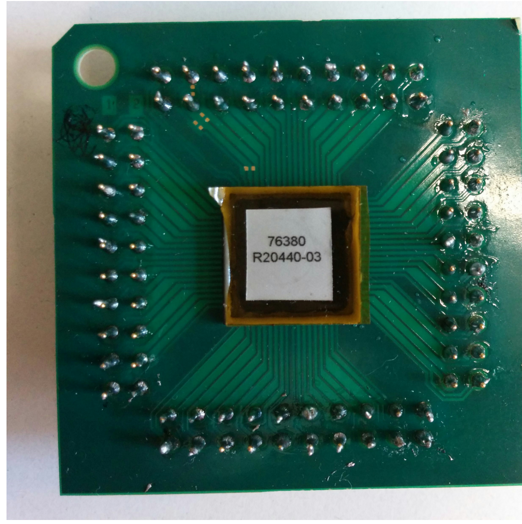

Fig. 6.1: Developed passive board with mounted chip.

top part can be easily removed. It is impossible the use of a standard socket between chip and test board, as it would prevent us from opening the chip package. Therefore a small passive board is developed for every chip and the chips are mounted on these boards (Figure 6.1).

The passive board is connected to the mother-board by a home-made intermediate board. The intermediate board has two connectors, DSub-50, FMC and extra interconnection pins for the signals generated by FPGA. The interconnection pins give the access to generated signals by FPGA and the possibility of external measurement by an oscilloscope or a multimeter (Figure 6.2). The FMC connector on the intermediate board is connecting to the mother-board by the FMC connector to characterize the chip prototype in laboratory environment (Figure 6.4) and the DSub-50 connector is provided to characterize the chip prototype exposed to the radiation in vacuum chamber. The INFN Legnaro radiation test laboratory, the chip inside the vacuum chamber can get connected to the external components through a D-sub50 connector (Figure 6.3). The figure 6.5 shows schematically the set-up of prototype radiation test in Legnaro.

The test board has two power suppliers of 1.2 V for core and 2.5 V for pads of the chip. The blocks of chip prototype mentioned below are supplied independently by 5 jumpers which are provided on intermediate board:

- Write and Read circuit : VDD-general;

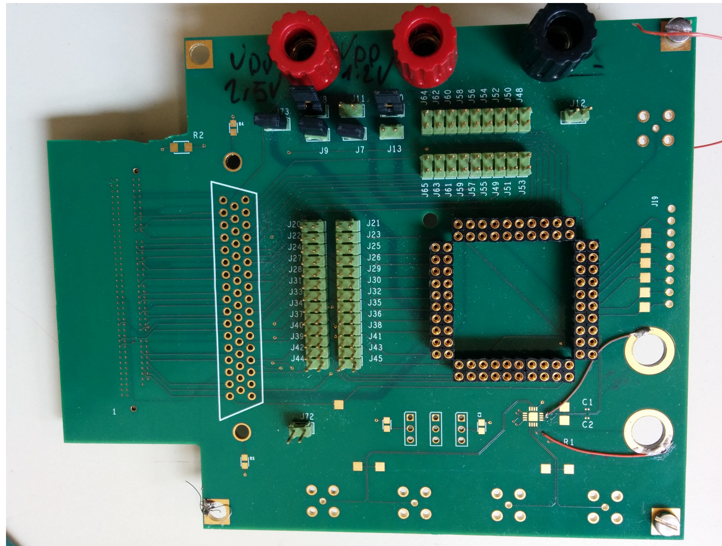

Fig. 6.2: Intermediate board with two connector options of Dsub-50 and FMC, and pins for control of each input and output signals of the chip.

- SRAM first version design;
- SRAM second version design;
- SRAM third version design;
- PAD powering.

Moreover the test setup gives the possibility of connecting and disconnecting separately each of power supplies.

6.2 VHDL architecture

The schematic in figure 6.6 shows the architecture of developed firmware written in VHDL to perform the prototype characterization with the FPGA, both in laboratory and in radiation environments. The approach of VHDL firmware architecture is to execute the radiation test in an automatic way because of the particular environment in vacuum chamber where the chip is exposed to the radiation. The firmware has no need to interact with an external PC during the test.

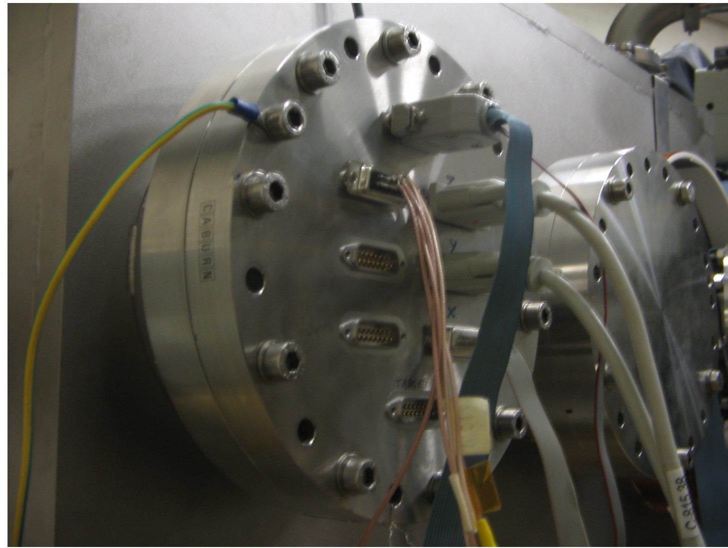

Fig. 6.3: Legnaro laboratory vacuum chamber and interface connectors between inside and outside.

The SRAM prototype has three function modes: write, read and standby which can be chosen using button on the mother-board. The VHDL architecture gives also the possibility of changing the type of written bits in three modes: write cells with alternative bit '1' and '0', with bit '0' or with bit '1'. The clock frequency has three options: 5, 10 and 20 MHz and they are optional during the test by the bottoms on the mother-board. The output bits can observed by ChipScope IP-Core through the JTAG (Joint Test Action Group) interface of the FPGA. The ChipScope tool integrates the measurement hardware components with the target design inside the FPGA device. The tool communicates with VHDL components and provides the designer with a logic analyzer solution.

Therefore the firmware architecture implement the FPGA to generate optional types of wire and read bits and frequencies of the clock.

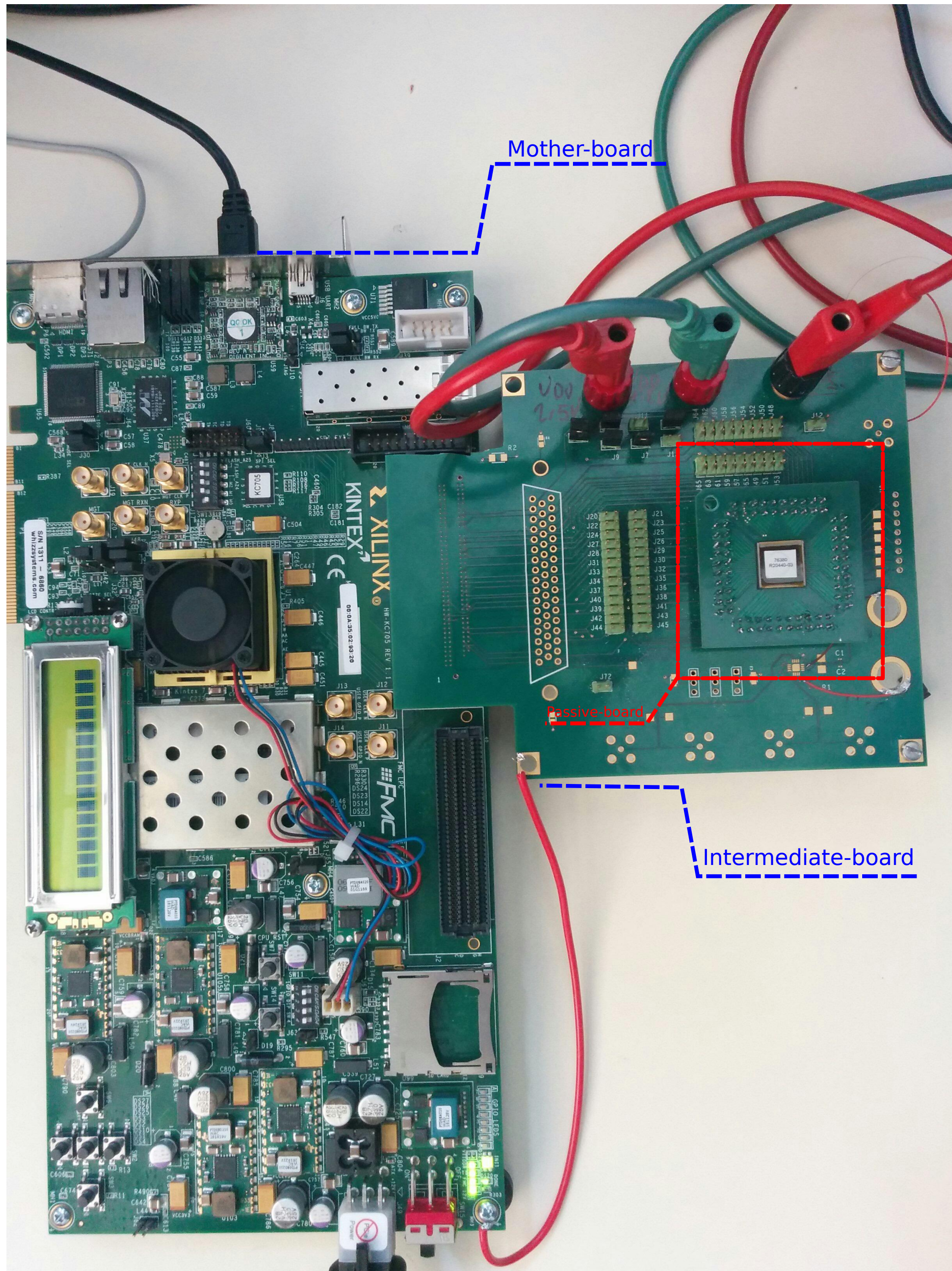

Fig. 6.4: Test System Setup in laboratory environment.

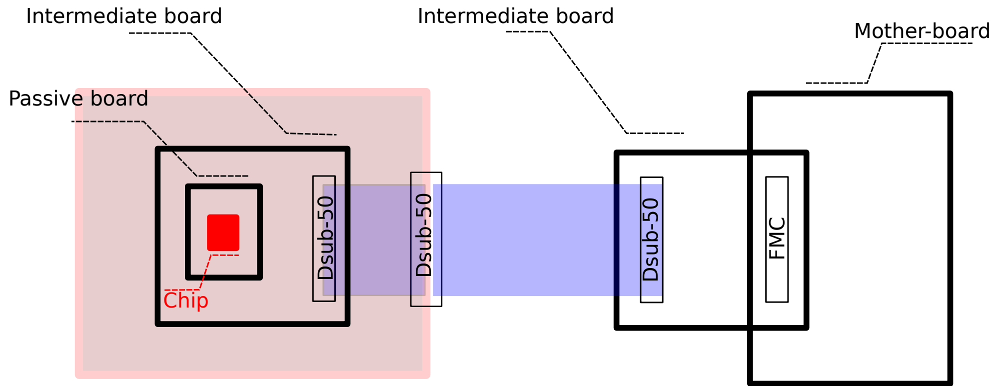

Fig. 6.5: (Schematic of test setup in Legnaro Laboratory for radiation tests.

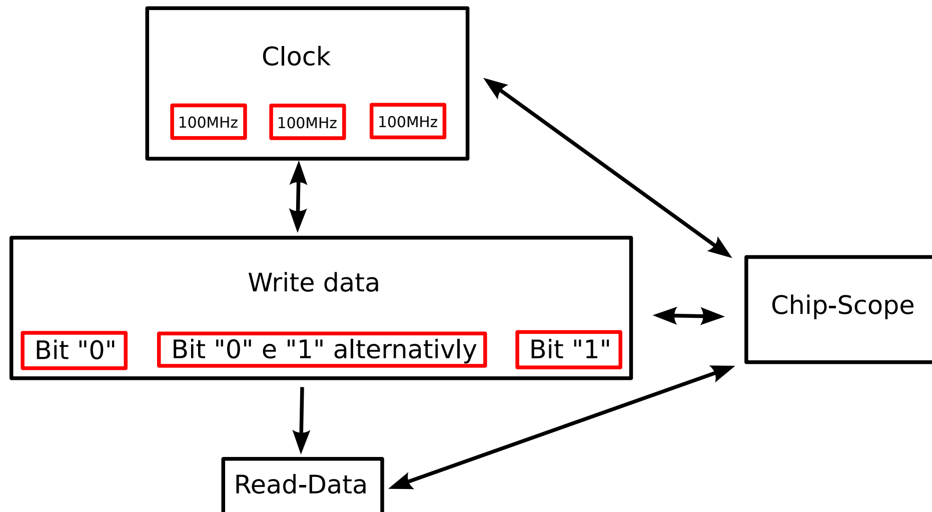

Fig. 6.6: Architecture of VHDL firmware.

7. FAST TRACKER TRIGGER SYSTEM

7.1 ATLAS and Triggering system

The luminosity of the Large Hardron Collider (LHC) at CERN is increasing to achieve a higher physics output in the next years. Higher luminosity requires more complex trigger system. Trigger system in LHC reduces event rate to just interesting events for physicist and has three main levels. Several upgrading of triggering and Data acquisition system (TDAQ) in ATLAS is going on to achieve an efficient event rate reduction at future LHC higher luminosity. The Fast TracKer (FTK) processor is an important part of trigger system upgrading in ATLAS. The FTK processes all events selected from level 1 of trigger system and pass to level 2 of trigger system, the rate of event coming from level 1 is up to 100 kHz with a latency in order of 100 ms [42].

7.2 Fast TracKer Trigger System

The block diagram shown in Figure 7.1 illustrates the function of the FTK system.

The pixel (PIX) and strip detectors (SCT) data are transmitted from the Readout Drivers (RODs) and received by the Data Formatters (DF). The Mezzanine cards on each DF perform cluster finding before the data are reorganized into η-ϕ towers and the DF transmits the cluster centroids of the eight layers to the processing units. The Data Organizers (DO) store hits from the DFs at full resolution and also convert them to coarse resolution superstrips (SS) which are appropriate for pattern recognition in the associative memory (AM) system. The DOs hold smart databases where full resolution hits are stored in a format that allows rapid access based on the pattern recognition road ID and then retrieved when the AM finds roads with the requisite number of hits. The associative memory (AM) system contains AM chips which contain a very large number of pre-loaded patterns, corresponding to the possible combinations for real tracks passing through a SS in each silicon

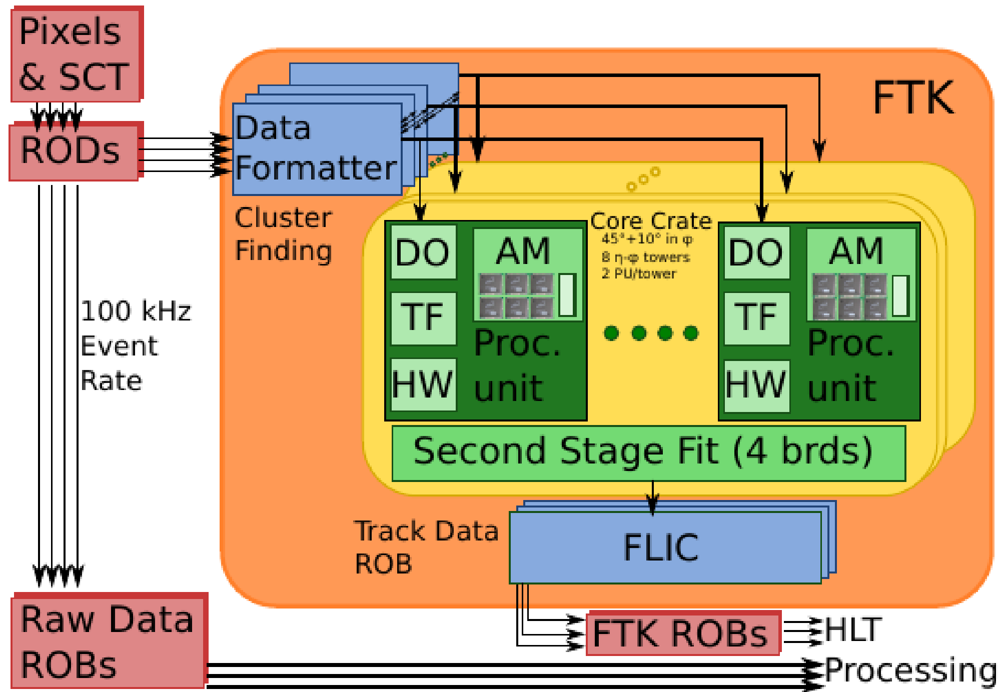

Fig. 7.1: FTK architecture.

layer. These are determined in advance from a full ATLAS simulation of single tracks using detector alignment extracted from real data. The AM system is a massively parallel system in that each hit is compared with all patterns simultaneously. After being found by the AM system, roads are returned to the DOs, which immediately fetch the associated full resolution hits and send them, together with the road, to the Track Fitter (TF). Because each road is quite narrow, the TF can obtain helix parameters with high resolution from a linear fit using the local coordinates in each layer. Such a fit is extremely fast and a modern FPGA can fit approximately 109 track candidates per second. Following fitting, duplicate track removal is carried out by the Hit Warrior (HW) for those 8-layer tracks in a road.

When a track passes the quality cuts of the 8-layer fit, the road number and hits are sent to the Second Stage Board (SSB). The track is extrapolated into the 4 additional layers, nearby hits are found, and a full 12-layer fit is carried out.

Duplicate track removal is again applied. SSB output data consisting of

the hits on the track and the helix parameters of the track are sent to the FTK Level 2 Interface Crate (FLIC). The FLIC formats and organizes the tracks and sends them to the HLT using the standard ATLAS data transmission protocols, and carries out monitoring functions [43].

The AM chip is the core of FTK system. The whole AM system stores 10^9 patterns with 128 k patterns stored in each chip.

AMchip compares stored patterns to input data received as 16 bit words at a 100 MHz rate in parallel over 8 input channels. At maximum speed the system will be able to perform $8 \cdot 10^{17}$ comparisons per second in parallel between 16-bit words.

The AMchip design is a very challenging because:

- the high number of stored pattern requires a large silicon area;
- the I/O signal congestion at the board level;
- the power limitation due to cooling system.

The FTK system contain 8000 AM chips in 8 VME crates and 4 racks and the power consumption should not exceed (da chiedere) per AM chip. for this reason the power consumption of chip is very critical for FTK system.

In this dissertation a new architecture of fully CMOS Content Addressable Memory (CAM) is proposed to reduce the power consumption of FTK AM chip. This architecture is integrated in the version 5 of AMchip (AMchip05).

The test results of AMchip05 confirm the simulation results successfully. The proposed architecture is integrated in final version of FTK AMchip (AMchip06).

The AMchip06 prototype has been fabricated and its characterization is going on.

7.3 New Content Addressable Memory

Content Addressable Memory (CAM) is an electronic device which compares input data with stored data and returns the address of matching data [44]. AM chip architecture in FTK system is based on an array of CAMs. The CAM array in AM chip has 18 bus and compares 18 bits coming from inner detector related on a single event with 18 stored bits. Output of the CAM array is the address of storage events which matches with one of the incoming events.

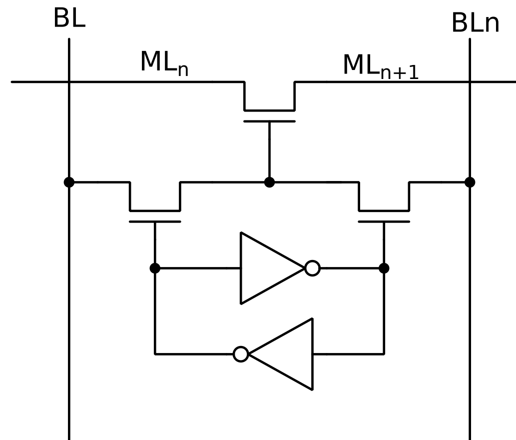

Fig. 7.2: Schematic diagram of a NAND single-bit CAM cell.

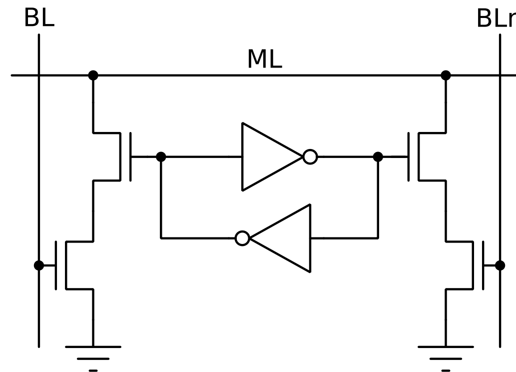

Fig. 7.3: Schematic diagram of a NOR single-bit CAM cell.

7.3.1 Conventional CAM cells

The figures 7.2 and 7.3 illustrate two examples of conventional CAM single cells based on NAND and NOR architecture, which are the most used of CAM cells.

In the FTK application, to achieve a match result for a 18-bit word, 18 CAM single cells must be employed. The 18 single cell CAM in NAND and NOR architecture can be connected together as illustrated in figures 7.4 and 7.5.

In both architectures, the match-line gains high voltage value before every comparison operation piloted by P-MOS transistor with ′pre′ control signal on the gate. CAM single cells discharge, the match-line if input bit does not match the storage bit and therefore the match-line discharges if all of input

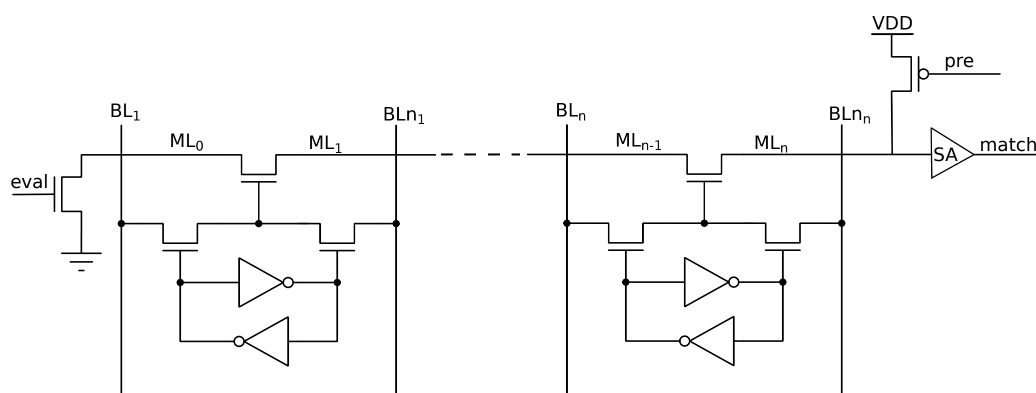

Fig. 7.4: Schematic of a NAND-based n-bit word CAM.

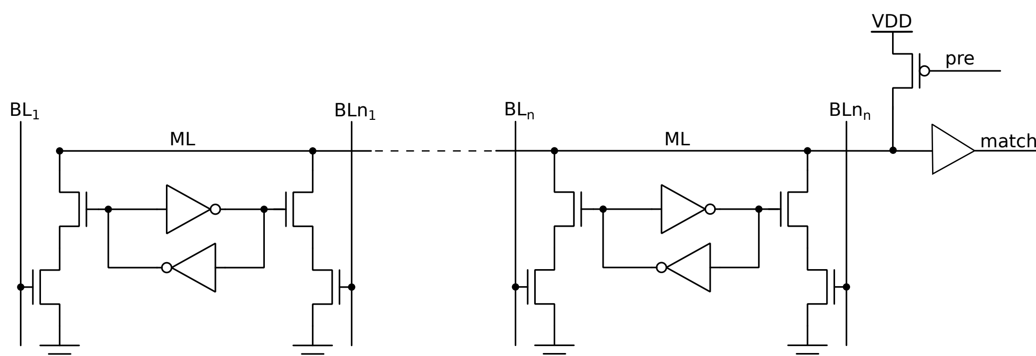

Fig. 7.5: Schematic diagram of a NOR-based n-bit word CAM.

18 bits of same work does not match with storage bit in all 18 CAM Single Cells of an array.

Pre-charging of the match-line is a power consuming operation since it happens in most of comparison operation (when all 18 bits from the same work does not match with storage bit of 18 single cells of the same array).

7.3.2 The new XORAM cell

The undesired power consumption of conventional CAMs in case of no match can be avoided by using a new CAM architecture proposed in this chapter. The architecture of proposed CAM is based on the XOR boolean function, although a CAM cell based on XOR (XNOR) boolean function was already proposed by Kadota in 1985 [45] and it is not widespread. The original architecture has 4 NMOS pass transistors. A suitable trade-off between the number of transistor, high robustness of design and low power consumption, a

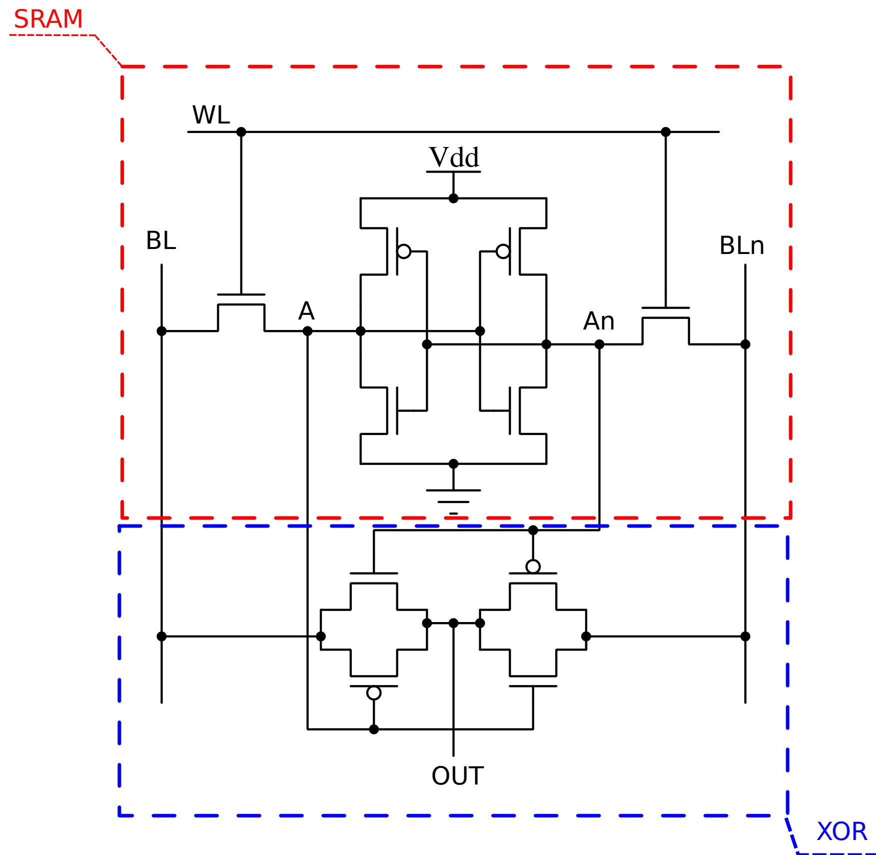

Fig. 7.6: Schematic diagram of the XOR-based single-bit CAM cell.

new architecture is proposed in this dissertation. The new cell called XORAM, consist of a 6T SRAM cell merged with 6T-XOR gate. Since SRAM provides both (A) and the inverted bit ($\bar{A}$), the XOR gate can be made using only 4 MOS transistors. The schematic diagram is shown in the figure 7.6 and developed layout design of single cell in 65 nm TSMC technology in the figure 7.7. The output signal of XORAM cell is equal to '0' when stored bit match the bit-lines and it is equal to '1' if it does not match the bit-line.

7.3.3 The 18-bit Word CAM

The 18-bit CAM is made with a 18-input NOR logic gate in three stages (Figure 7.8):

- six 3-input NOR cells;
- two 3-input NAND cells;

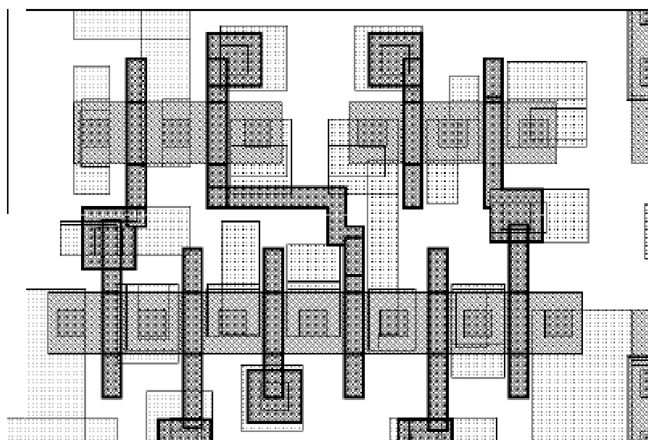

Fig. 7.7: Layout of the XOR-based CAM cell in 65 nm CMOS technology.

- one 3-input NOR cell.

In this new architecture the output (O) of the 18-bit CAM must have a high logic value when all input bits match the stored data, and a low logic value if at least one bit does not match. This operation can be performed by a simple 18-input NOR logic.

To avoid spurious glitches at the output during write operation, the write signal (WL) is used as an additional input to the last stage of the 18-input NOR gate.

7.3.4 Simulation Results

The layout of an 18-bit CAM has been designed and simulated after parasitic extraction. Simulation results confirm that write and compare operations is perfectly functional up to 1 GHz frequency. However, the printed circuit board designed for the track recognition system works at a frequency which cannot exceed 100 MHz. For this reason, simulations were performed with a 100 MHz clock frequency.

Table 7.1 summarizes the results of corner analysis and shows the output delay, the average current and the peak value of the current drawn from the VDD supply. The simulations for worst speed (WS), worst power (WP), worst one (WO) and worst zero (WZ) conditions are performed by using appropriate parameters of transistors, Temperature (T) and supply voltage

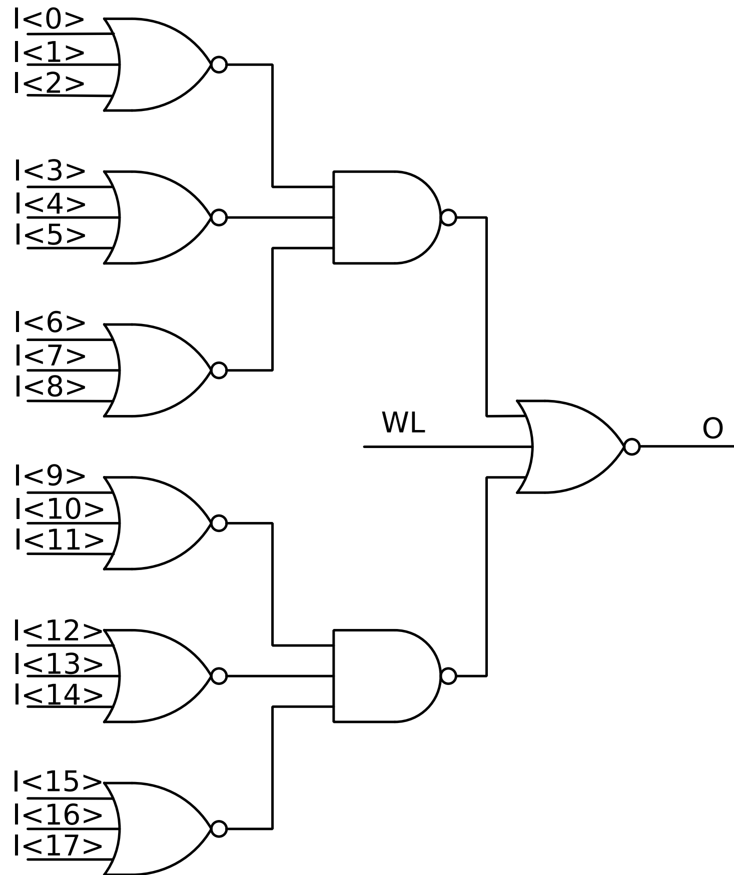

Fig. 7.8: Schematic diagram of the 18-bit NOR logic gate.

(VDD) in each cases. The simulation results are shown in the table 7.1.

In typical conditions, the average current required by the 18-bit XORAM-based CAM is 0.7 µA during read operation (at 100 MHz). The largest current consumption occurs with worst power MOS parameters and the average current is 1.3 µA. The previous conventional NAND or NOR-based CAMs architecture requires an average current of 6 µA and the proposed scheme achieves a current reduction by a factor of 8 in typical case.

The XORAM architecture is integrated in AMCHIP06. The AMCHIP06 is final prototype chip of FTK and it is under characterization in our laboratory at INFN-Milano 7.9.

Tab. 7.1: Simulation results at 100 MHz: delay time, average current and peak current in different conditions.

	T (°C)	V_{DD} (V)	$t_{clk,match}$ (ps)	$avg(\mid i_{DD} \mid)$ (nA)	$peak(\mid i_{DD} \mid)$ (µA)
TM	27	1.20	928	707.6	637.3
WS	125	1.08	1741	650.1	340.1
WS	−50	1.32	928	768.8	744.9
WP	125	1.08	909	1310.0	604.5
WP	−50	1.32	576	836.0	1163.0
WO	125	1.08	1177	743.3	259.6
WO	−50	1.32	687	788.0	901.7
WZ	125	1.08	1358	851.3	429.6
WZ	−50	1.32	760	779.0	903.0

Fig. 7.9: AMCHIP05: final prototype chip of Fast TracKer project.

8. CONCLUSION AND RESULTS

In this section the results of research activities of this dissertation are discussed and the contribution of these results in different projects is presented. Moreover the presented research activities and their results are published in the literature, and the bibliography of these articles are listed in the final part of this section.

8.1 Radiation Hard SRAM

The three versions of radiation hard SRAM were designed and simulated in worth-case conditions, including different types of radiation effects. This activity is supported with a great interest by INFN and RD53 collaboration at CERN and was integrated in CHIPIX65 project funded by INFN.

The first prototype chip, which integrating all three versions of radiation hard SRAM block, has been designed and submitted in TSMC 65 nm technology. Furthermore, The test set-up which was requiring two home-made boards for further test of chip prototype in vacuum chamber and exposed to the radiation is developed.

The first prototype is characterized in laboratory environment and the results show that the Write and Read operations of SRAM blocks do not have a proper functionality.

More studies are, been carried out to find the reason of not proper functioning and after different investigations, the solution is proposed for the next version of prototype design.

As explained in chapter 3, the DICE SRAM architecture is not sensitive to not simultaneous changes, and disturbs of redundant pair stored bits, but it is very sensitive if both stored bits are changed or disturbed in the same way simultaneously. The position of single memory cell of array, which is selected by multiplexers, is the interconnection point of selected bit-line and word-line of memory array. During Write and Read operations, in addition of selected single memory cell, all the single memory cells of array which has in common

the selected word-line (all cells of related row), have pass-transistors in "on" state with connected bit-line and negative bit-line in floating state. The hypothesis was that the floating bit-line and inverted bit-line connected to the feedback of SRAM circuit which have the pass-transistors in "on" state, do not disturb the storage bit of SRAM single memory cell. This hypothesis is the base of regular type of design for simple SRAM memory arrays architecture. However, the high sensitivity of SRAM DICE architecture to simultaneous disturbs of both redundant stored bits, combined with parasitic voltage differences between bit-line and negative bit-line in floating state, because of high length of wires in 64 k bits array, causes the change of stored bit in some cells with pass-transistors in "on" state and bit-line and negative bit-line wires in floating state.

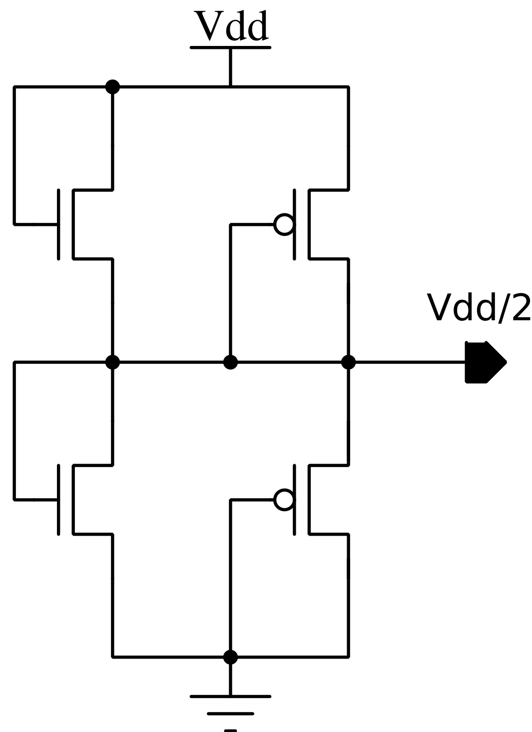

Fig. 8.1: Voltage generator circuit.

More investigation of DICE SRAM architectures through different simulations confirms that if the bit-line and negative bit-line are biased at half of high voltage value after every Read and Write operation, the difference of voltage required in the bit-line and negative bit-line nodes to flip the stored bit changes from 200 mV in case of floating wires, to at least 400 mV with

the reference voltage at half voltage value, which is 0.6 V in our case. To realize this idea an analog circuit of voltage generator is added to the Write and Read circuits of the first prototype design (Figure 8.1). The circuit drives all bit-line and negative bit-line wires at half supply voltage value after every Read and Write operation. The simulations results confirm that the SRAM block Write and Read operations work properly in this approach.

The second prototype of radiation hard SRAM which is including the corrections is under development and will be integrated in the next submission of CHIPIX65 project.

8.2 Dual-rail Logic

The DICE architecture increases the tolerance of Single Event Upset (SEU) in memories, however the Single Event Transient (SET) in combinational logic needs different architecture methods to mitigate. For instance SET effects in multiplexer circuits which are used to codify the addresses of memory cells in SRAM array, can cause the write or read of wrong memory cells.

Double-Rail Redundant Approach (D2RA) is proposed to develop the standard cells for further development to increase the SET tolerance of combinational logic.

In D2RA approach the same logic information stores in two different nets (the bit and the inverted bit), which are spaced at layout level. If a SET occurs, the bit and the inverted bit will assume the same logic value, i.e., '00' or '11', which indicates that data is invalid. Hence, a new logic state which can implemented by a flip-flop is proposed to detect and to stop SET propagation in combinational and sequential logic. In this way, a SET propagation will not trigger a SEU (Figure 8.2).

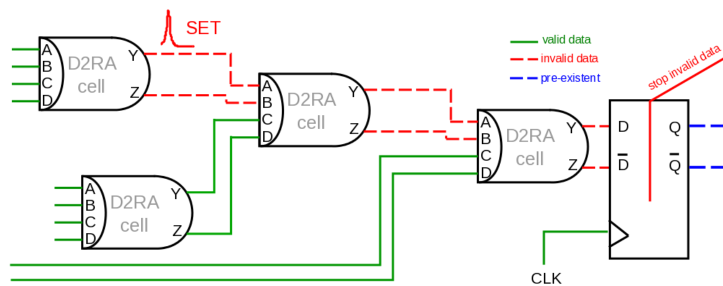

Fig. 8.2: Example of logic chain, with a SET propagation.

A test chip, containing trees of AND-NAND and XOR-XNOR cells, and shift registers has been designed. The simulations in worth-case condition including radiation effects demonstrate the proper function of the circuits. The designs are submitted in the context of CHIPIX65 project in RD53 collaboration and the characterization will be made in next months.

We have the plan of integrating the D2RA cells with DICE memory cells to have the final circuit architecture with high tolerance to SEUs and SETs. This circuits can be used in harsh radiation environments as high energy physics experiments and space.

8.3 Fast Tracker Trigger

In the Fast TracKer (FTK) project the alternative architecture of XORAM was successfully characterized in AMchip05 and integrated in the final chip version (AMchip06). The AMchip06 is under characterization and it will be an important part of the next generation of trigger system for Run 2 of ATLAS experiment at CERN.

8.4 Published Papers And Presentations

This dissertation has contributions in: Advanced European Infrastructures for Detectors at Accelerators (AIDA) project, Fast Tracker Trigger (FTK) project for ATLAS experiment at CERN and CHIPIX65 project in RD53-CERN collaboration. The results and progress of dissertation activity are presented in different meetings and conferences, and the contributions are published in some articles:

1. A Andreani, A Annovi, R Beccherle, M Beretta, N Biesuz, W Billereau, R Cipriani, S Citraro, M Citterio, A Colombo, et al. The associative memory serial link processor for the Fast TracKer (FTK) at ATLAS. *Journal of Instrumentation*, 9(11):C11006, 2014.

2. Alessandro Andreani, Alberto Annovi, Roberto Beccherle, Matteo Beretta, Nicolo Biesuz, Mauro Citterio, Francesco Crescioli, Paola Giannetti, Valentino Liberali, Seyedruhollah Shojaii, et al. Characterisation of an associative memory chip for high-energy physics experiments. In *International instrumentation and measurement*

technology conference (I2MTC), pages 1487–1491. IEEE, 2014.

3. Matteo Beretta, A Annovi, A Andreani, M Citterio, A Colombo, V Liberali, S Shojaii, A Stabile, R Beccherle, P Giannetti, et al. Next generation associative memory devices for the FTK tracking processor of the atlas experiment. *Journal of Instrumentation*, 9(03):C03053, 2014.

4. Alessandra Camplani, Seyedruhollah Shojaii, Hitesh Shrimali, Alberto Stabile, and Valentino Liberali. CMOS IC radiation hardening by design. *Facta universitatis-series: Electronics and Energetics*, 27(2):251–258, 2014.

5. Valentina Ciriani, Luca Frontini, Valentino Liberali, Seyedruhollah Shojaii, Alberto Stabile, and Gabriella Trucco. Radiation-tolerant standard cell synthesis using double-rail redundant approach. In 2014 21st IEEE International Conference on *Electronics, Circuits and Systems (ICECS)*, , pages 626–629. IEEE, 2014.

6. N Demaria, G Dellacasa, G Mazza, A Rivetti, MD Da Rocha Rolo, E Monteil, L Pacher, F Ciciriello, F Corsi, C Marzocca, et al. Chipix65: Developments on a new generation pixel readout asic in CMOS 65 nm for hep experiments. In *IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, on pages 49–54, 2015.

7. Natale Demaria, F Ciciriello, F Corsi, C Marzocca, G De Robertis, F Loddo, C Tamma, V Liberali, S Shojaii, A Stabile, et al. RD53 collaboration and CHPIX65 project for the development of an innovative pixel front end chip for HL-LHC. In *INFN Workshop on Future Detectors for HL-LHC (IFD2014)*, page 10, 2014.

8. Luca Frontini, Seyedruhollah Shojaii, Alberto Stabile, and Valentino Liberali. A new XOR-based content addressable memory architecture. In IEEE International Conference on *Electronics, Circuits and Systems (ICECS)*, pages 701–704, 2012.

9. Pierluigi Luciano et al. The Serial Link Processor for the Fast TracKer (FTK) processor at ATLAS. *International Conference on Technology and Instrumentation in Particle Physics, 2014.*

10. Seyedruhollah Shojaii, Alberto Stabile, and Valentino Liberali. A radiation hardened static ram for high-energy physics experiments. In International Conference on *Microelectronics Proceedings (MIEL)*, pages 359–362, 2014.

11. I am CERN authorship member and co-author of 100 articles in ATLAS collaboration.

BIBLIOGRAPHY

[1] A. Camplani, S. Shojaii, H. Shrimali, A. Stabile, and V. Liberali, "CMOS IC radiation hardening by design," *Facta universitatis-series: Electronics and Energetics*, vol. 27, no. 2, pp. 251–258, 2014.

[2] G. Abadir, W. Fikry, H. Ragai, and O. Omar, "A new semi-empirical model for funneling assisted drain currents due to single events," in *15th International Conference on Microelectronics*, pp. 391–394, IEEE, 2003.

[3] A. Stabile, V. Liberali, and C. Calligaro, "Design of a rad-hard library of digital cells for space applications.," in *ICECS*, pp. 149–152, 2008.

[4] J. Srour *et al.*, "Basic mechanisms of radiation effects on electronic materials, devices, and integrated circuits," tech. rep., DTIC Document, 1982.

[5] J. R. Schwank, "Basic mechanisms of radiation effects in the natural space radiation environment," tech. rep., Sandia National Labs., Albuquerque, NM (United States), 1994.

[6] J. P. Mitchell, "Radiation-induced space-charge buildup in MOS structures," *IEEE Transactions on Nuclear Science*, vol. 14, no. 11, pp. 764–774, 1967.

[7] F. B. McLean and T. R. Oldham, "Basic mechanisms of radiation effects in electronic materials and devices," tech. rep., DTIC Document, 1987.

[8] T. Granlund and N. Olsson, "SEUs induced by thermal to high-energy neutrons in SRAMs," *IEEE transactions on nuclear science*, vol. 53, no. 6, pp. 3798–3802, 2006.

[9] P. McWhorter and P. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors," *Applied physics letters*, vol. 48, no. 2, pp. 133–135, 1986.

[10] J. Aitken and D. Young, "Avalanche injection of holes into SiO_2," *IEEE Transactions on Nuclear Science*, vol. 24, no. 6, pp. 2128–2134, 1977.

[11] P. Winokur, H. Boesch Jr, J. McGarrity, and F. McLean, "Field-and time-dependent radiation effects at the SiO2/Si interface of hardened MOS capacitors," *IEEE Transactions on Nuclear Science*, vol. 24, no. 6, pp. 2113–2118, 1977.

[12] N. Saks, M. Ancona, and J. Modolo, "Radiation effects in MOS capacitors with very thin oxides at 80â° k," *Nuclear Science, IEEE Transactions on*, vol. 31, no. 6, pp. 1249–1255, 1984.

[13] F. McLean, "A framework for understanding radiation-induced interface states in SiO_2 MOS structures," *IEEE Transactions on Nuclear Science*, vol. 27, no. 6, pp. 1651–1657, 1980.

[14] M. Gaillardin, V. Goiffon, S. Girard, M. Martinez, P. Magnan, and P. Paillet, "Enhanced radiation-induced narrow channel effects in commercial 0.18 μm bulk technology," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 2807–2815, 2011.

[15] G. Baccarani and M. R. Wordeman, "Transconductance degradation in thin-oxide MOSFET's," *IEEE Transactions on Electron Devices*, vol. 30, no. 10, pp. 1295–1304, 1983.

[16] J. Schwank, F. Sexton, M. Shaneyfelt, and D. Fleetwood, "Total ionizing dose hardness assurance issues for high dose rate environments," *IEEE Transactions on Nuclear Science*, vol. 54, no. 4, pp. 1042–1048, 2007.

[17] M. V. O'Bryan, K. A. LaBel, S. D. Kniffin, C. Poivey, J. W. Howard Jr, R. L. Ladbury, S. P. Buchner, T. R. Oldham, P. W. Marshall, A. B. Sanders, *et al.*, "Recent single event effects results for candidate spacecraft electronics for NASA," in *IEEE Transactions on NSREC Radiation Effects Data Workshop*, 2005.

[18] A. Johnston, "The influence of VLSI technology evolution on radiation-induced latchup in space systems," *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, pp. 505–521, 1996.

[19] T. G. Northrop and E. Teller, "Stability of the adiabatic motion of charged particles in the earth's field," *Physical Review*, vol. 117, no. 1, p. 215, 1960.

[20] R. Selesnick, M. Looper, and R. Mewaldt, "A theoretical model of the inner proton radiation belt," *Space Weather*, vol. 5, no. 4, 2007.

[21] M. Looper, J. Blake, and R. Mewaldt, "Response of the inner radiation belt to the violent sun-earth connection events of october–november 2003," *Geophysical Research Letters*, vol. 32, no. 3, 2005.

[22] D. V. Reames, "Particle acceleration at the sun and in the heliosphere," *Space Science Reviews*, vol. 90, no. 3-4, pp. 413–491, 1999.

[23] M. Menouni, M. Barbero, F. Bompard, S. Bonacini, D. Fougeron, R. Gaglione, A. Rozanov, P. Valerio, and A. Wang, "1-Grad total dose evaluation of 65 nm CMOS technology for the HL-LHC upgrades," *Journal of Instrumentation*, vol. 10, no. 05, p. C05009, 2015.

[24] P. Valerio, "65 nm technology for HEP: Status and perspective," in *Proceedings of the The 23rd International Workshop on Vertex Detectors (VERTEX2014)*, vol. 1, p. 43, 2014.

[25] S. Diehl, P. Dressendorfer, R. Koga, W. Kolasinski, *et al.*, "Error analysis and prevention of cosmic ion-induced soft errors in static CMOS RAMs," *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 2032–2039, 1982.

[26] S. J. Heileman, W. R. Eisenstadt, R. M. Fox, R. S. Wagner, N. Bordes, and J. M. Bradley, "CMOS VLSI single event transient characterization," *IEEE Transactions on Nuclear Science*, vol. 36, no. 6, pp. 2287–2291, 1989.

[27] L. T. Clark, K. C. Mohr, K. E. Holbert, X. Yao, J. Knudsen, and H. Shah, "Optimizing radiation hard by design SRAM cells," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2028–2036, 2007.

[28] M. N. Liu and S. Whitaker, "Low power SEU immune CMOS memory circuits," *IEEE Transactions on nuclear science*, vol. 39, pp. 1679–1684, 1992.

[29] D. Bessot and R. Velazco, "Design of SEU-hardened CMOS memory cells: the HIT cell," *RADECS-93*, pp. 563–570, 1994.

[30] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Transactions on Nuclear Science*, pp. 2874–8, 1996.

[31] E. Petersen, P. Shapiro, J. Adams Jr, and E. Burke, "Calculation of cosmic-ray induced soft upsets and scaling in VLSI devices," *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 2055–2063, 1982.

[32] J. Abraham, E. S. Davidson, J. H. Patel, *et al.*, "Memory system design for tolerating single event upsets," *IEEE Transactions on Nuclear Science*, vol. 30, no. 6, pp. 4339–4344, 1983.

[33] M. S. Gorbunov, P. S. Dolotov, A. A. Antonov, G. I. Zebrev, V. V. Emeliyanov, A. B. Boruzdina, A. G. Petrov, and A. V. Ulanova, "Design of 65 nm cmos sram for space applications: A comparative study," *IEEE Transactions on Nuclear Science*, vol. 61, no. 4, pp. 1575–1582, 2014.

[34] H. Barnaby, "Total-ionizing-dose effects in modern CMOS technologies," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103–3121, 2006.

[35] I. S. Esqueda, H. J. Barnaby, and M. L. Alles, "Two-dimensional methodology for modeling radiation-induced off-state leakage in CMOS technologies," *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2259–2264, 2005.

[36] G. Messenger, "Collection of charge on junction nodes from ion tracks," *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 2024–2031, 1982.

[37] B. Narasimham, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, M. J. Gadlage, O. Amusan, W. T. Holman, A. F. Witulski, W. H. Robinson, J. D. Black, *et al.*, "Characterization of digital single event transient pulse-widths in 130-nm and 90-nm CMOS technologies," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2506–2511, 2007.

[38] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 583–602, 2003.

[39] J. M. Hutson, J. D. Pellish, G. Boselli, R. Baumann, R. Reed, R. D. Schrimpf, R. Weller, L. W. Massengill, *et al.*, "The effects of angle of incidence and temperature on latchup in 65 nm technology," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2541–2546, 2007.

[40] A.Stabile, "Design metodologies for radiation-hardened memories in CMOS technology," in *Ph.D. dissertation*, Milan University, 2009.

[41] P. Dodd, O. Musseau, M. Shaneyfelt, F. Sexton, C. D'hose, G. Hash, M. Martinez, R. Loemker, J.-L. Leray, and P. Winokur, "Impact of ion energy on single-event upset," *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2483–2491, 1998.

[42] M. Beretta, A. Annovi, A. Andreani, M. Citterio, A. Colombo, V. Liberali, S. Shojaii, A. Stabile, R. Beccherle, P. Giannetti, *et al.*, "Next generation associative memory devices for the FTK tracking processor of the ATLAS experiment," *Journal of Instrumentation*, vol. 9, no. 03, p. C03053, 2014.

[43] A. Andreani, A. Annovi, R. Beccherle, M. Beretta, N. Biesuz, W. Billereau, R. Cipriani, S. Citraro, M. Citterio, A. Colombo, *et al.*, "The associative memory serial link processor for the fast tracker (FTK) at ATLAS," *Journal of Instrumentation*, vol. 9, no. 11, p. C11006, 2014.

[44] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 3, pp. 712–727, 2006.

[45] H. Kadota, J. Miyake, Y. Nishimichi, H. Kudoh, and K. Kagawa, "An 8-kbit content-addressable and reentrant memory," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 5, pp. 951–957, 1985.