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Oxide-based memristive devices by block copolymer self-assembly

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Cover illustration:

Moiré pattern produced by superimposing a regular grid over a pattern created by self-assembled block copolymer lamellae. The appearance of the Moiré pattern denotes the regularity of block copolymer nanostructures, with a constant spacing among features. This pattern can also be used to visually distinguish among different domains in which lamellae have parallel orientation. Moiré patterns are routinely observed during scanning electron microscopy analysis due to the horizontal scan lines and can also be visualized in monitors whenever the pixel grid spacing approaches the periodicity of block copolymer features.

OXIDE-BASED MEMRISTIVE DEVICES BY BLOCK COPOLYMER SELF-ASSEMBLY

Oxide-based memristive systems represent today an emerging class of devices with a significant potential in memory, logic, and neuromorphic circuit applications. These devices have a simple capacitor structure and promise superior scalability together with favorable memory performances. This thesis presents a study of resistive switching phenomena in HfO_x -based nanoscale memristive devices, with focus on material properties and development of bottom-up approaches for the fabrication of structures with dimension down to the nanoscale.

One of the main issues for practical applications regarding device variability is first assessed by doping hafnium oxide films with different concentrations of aluminum atoms. Testing devices are analyzed by physico-chemical and electrical techniques in order to define the effect of oxide doping on the device properties. In the following part of the thesis, the scalability limit is explored in very high density arrays of nanodevices produced exploiting a lithographic approach based on the bottom-up self-assembly of block copolymer templates. This technique allows a tight control over the size and density of the defined features, and the possibilities offered by block copolymer patterning are here discussed. Electrical measurements of the nanodevices are performed through conductive atomic force microscopy. The device variability is examined and related to the inherent oxide non-homogeneity at the nanoscale, while a non-volatile switching of the resistance of the nanodevices is demonstrated. Further, this analysis draws the attention to a crosstalk phenomenon occurring at the nanoscale in a continuous thin film geometry. This result suggests to select different system configurations. A promising technique based on selective reactions with one copolymer block is finally discussed which allows the direct production of oxide patterns from block copolymer templates avoiding a pattern transfer process. In conclusion, the results reported in this thesis highlight the high scalability potential of oxide-based memristive devices, providing a missing piece of information for the understanding and practical development of very high density arrays.

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Motivation and objective of the activity

The increasing number of connected devices and mobile applications, together with the development of internet-based services such as cloud computing and data centers, are boosting the demand for massive data storage and manipulation. In server applications, memory is responsible for a substantial part of the overall energy consumption, while mobile devices also pose stringent requirements in terms of energy efficiency. On the other hand, memory latency is a key factor in enabling a number of possible applications. A substantial gap of 3 to 5 decades in capacity and latency exists between the leading technologies for low-latency but volatile memory (DRAM) and the long-latency but nonvolatile technologies used for massive data storage (mainly flash and magnetic hard drives)¹.

Current memory technologies are facing several challenges. Leading nonvolatile memories are based on a floating gate or charge trapping layer, which stores the memory bits as charge carriers trapped inside the cell². This technology allows the relatively inexpensive manufacturing of large amount of memory. However, the high voltage required to store the information and reliability issues prevent a further scaling of the cell dimension. Integration is now proceeding exploiting the third direction in a stacked 3D approach that further enhances the fabrication complexity³, while a further improvement of memory latency and energy efficiency are hardly achievable with this technology⁴. The increasing need for high density data storage is driving the development of alternative concepts, established to overcome some of the limitations imposed by charge-based memories⁵. The exploitation of these new technologies requires the investigation of new physical mechanisms and new materials, shifting the interest from silicon-based chemistry toward a plethora of new elemental combinations.

¹G. Atwood et al., "A semiconductor memory development and manufacturing perspective", in European solid state circuits conference (ESSCIRC), ESSCIRC 2014 - 40th (Sept. 2014), pp. 1–6.

²P. Pavan et al., "Flash memory cells-an overview", *Proceedings of the IEEE* **85**, 1248–1271 (1997).

³K.-T. Park et al., "Three-dimensional 128 gb MLC vertical nand flash memory with 24-WL stacked layers and 50 MB/s high-speed programming", *Solid-State Circuits, IEEE Journal of* **50**, 204–213 (2015).

⁴*International technology roadmap for semiconductors*, version ITRS 2013 edition, (2013) www.itrs2.net.

⁵D. Wouters et al., "Phase-change and redox-based resistive switching memories", *Proceedings of the IEEE* **103**, 1274–1288 (2015), Y. Fujisaki, "Review of emerging new solid-state non-volatile memories", *Japanese Journal of Applied Physics* **52**, 040001 (2013).

In this context, the development of new non-volatile memory technologies combining high density with low latency is of paramount importance for the real-time manipulation of large amount of data. At the same time, new computational paradigms recently emerged which can provide enhanced efficiency for selected tasks and algorithms. The application of devices with memristive functionality can be of uttermost importance for the development and practical implementations of reconfigurable circuit designs that embed logic along with memory functionality as well as systems that can mimic neuronal functionality⁶.

Among others, resistive switching memories (RRAM) are one of the most promising concepts for the next generation of nonvolatile memory technologies thanks to their superior scalability, fast switching time, and low power consumption⁷. RRAM devices are based on a simple two-terminals capacitor structure which is easily integrable in high density arrays. As a proper voltage is applied between the two metal electrodes sandwiching the insulating material, the memory cell can change its resistance between at least two resistance values, which correspond to distinct memory states. On the contrary, by applying a low voltage the resistance level can be probed without altering the memory state. This category of devices was associated with the generalized definition of memristive systems⁸, based on a new class of passive devices first termed memristor from a contraction of the words memory and resistor⁹. This definition was adopted since it depicts a passive device with variable resistance and memory functionality.

A large number of combinations of electrodes and insulating materials shows resistive switching characteristics, and different mechanisms were associated with the resistance variation property¹⁰. A short overview of the main mechanisms and type of RRAM cells can be found in Chapter 1. In this thesis, a special focus is devoted to RRAM based on hafnium oxide, since they are currently considered one of the most promising options for a future application in high density memory arrays. These cells possess very high scalability thanks to the nanometric size of the conduction path that establishes in the insulating material and is responsible for the resistance variation¹¹. However, the stochastic processes involved in the filament formation and partial dissolution at each cycle also entail a marked variability. This variability issue constituted one of the main hindrances for a practical application of this new memory technology¹². In this respect, oxide doping with trivalent atoms was identified as a possible method to mitigate the variability. In this thesis, the properties of RRAM cells based on HfO₂ films doped with Al atoms are investigated as a function of Al concentration. While a moderate Al concentration around 4% was found to improve the variability among different cells and for repeated cycles, a higher concentration led to a marked deterioration of the retention properties even at low temperature.

⁶J. J. Yang et al., "Memristive devices for computing", *Nature Nanotechnology* **8**, 13–24 (2013).

⁷D. Ielmini et al., eds., *Resistive switching: from fundamentals of nanionic redox processes to memristive device applications* (Wiley Vch, 2016), 784 pp., Y. Nishi, *Advances in non-volatile memory and storage technology* (Elsevier, 2014), 551 pp.

⁸D. B. Strukov et al., "The missing memristor found", *Nature* **453**, 80–83 (2008).

⁹L. O. Chua, "Memristor-the missing circuit element", *Circuit Theory, IEEE Transactions on* **18**, 507–519 (1971).

¹⁰S. Menzel et al., "Redox-based resistive memory", in *Emerging nanoelectronic devices*, edited by A. Chen et al. (John Wiley & Sons Ltd, 2014), pp. 137–161.

¹¹U. Celano et al., "Imaging the three-dimensional conductive channel in filamentary-based oxide resistive switching memory", *Nano Letters* **15**, 7970–7975 (2015).

¹²L. Baldi et al., "Emerging memories", *Solid-State Electronics, Selected papers from ESSDERC 2013* **102**, 2–11 (2014).

Despite fully functional RRAM devices down to a few nm were demonstrated, the nanoscale switching mechanism and the ultimate scalability limit are not fully understood¹³. Alongside isolated test devices with dimension of a few nanometer, multiple nanoscale memory cells arranged in very high density arrays need to be tested for an investigation of the possible effects arising in high density arrays. However, the fabrication of a large number of devices with dimension and spacing down to the nanoscale entails several fabrication difficulties. As the critical feature size shrinks, a reliable patterning increases in complexity and cost. In this context, the application of new bottom-up approaches holds the potential to overcome the limitations imposed by standard lithographic techniques based on top-down approaches¹⁴. Bottom-up techniques exploit the self-organizing nature of particular systems in order to produce regular features with high degree of order. Block copolymer is an example of self-assembling system in which two chemically immiscible polymer units covalently bonded together can self-assemble in periodic nanopatterns upon thermal treatment¹⁵. This class of polymers recently established as a tool that can simplify the patterning process and offers further scalability potential for technology nodes down to 5 nm¹⁶.

The objective of the work presented in this thesis is to exploit the possibilities offered by bottom-up fabrication techniques for the patterning of very high density device arrays with feature size down to the nanoscale. On one side, this approach offers the opportunity to test bottom-up fabrication methods for functional device patterning, evidencing limitations and strengths. On the other side, at the laboratory scale bottom-up templates offer a relatively inexpensive way of overcoming the limits of top-down lithography. In this way, patterning of extremely small features and very high densities becomes under reach, enabling the study of the resistance switching phenomenon in nanoscale devices in order to assess the potential scalability.

In this thesis work, asymmetric block copolymers forming cylindrical domains perpendicular to the substrate are selected for the bottom-up formation of regular nanoporous templates with hexagonal symmetry. A study is carried out in order to control block copolymer self-assembly on top of the hafnium oxide surface for the patterning of very high density arrays of metal electrodes. The selective contact of the nanodevices with nanoscale dimension can be performed at the laboratory level through the sharp conductive tip of the conductive atomic force microscope (C-AFM). This technique allows electrical characterization to be performed in conjunction with morphological maps of the surface, thus it allows to locate the nanodevices avoiding demanding alignment and contacting techniques.

Block copolymer-based lithography is a promising technology for high throughput and relatively inexpensive patterning of highly scaled features. However, from a practical point of view several challenges need to be addressed for a full exploitation of this class of polymers in patterning processes. One of the main difficulties relies in the pat-

¹³D. S. Jeong et al., "Emerging memories: resistive switching mechanisms and current status", Reports on Progress in Physics **75**, 076502 (2012).

¹⁴S. Spiga et al., "Bottom-up approaches for resistive switching memories", in *Resistive switching: from fundamentals of nanionic redox processes to memristive device applications*, edited by D. Ielmini et al. (Wiley Vch, 2016).

¹⁵F. S. Bates et al., "Block copolymer thermodynamics: theory and experiment", Annual Review of Physical Chemistry **41**, 525–557 (1990).

¹⁶M. A. Morris, "Directed self-assembly of block copolymers for nanocircuitry fabrication", Microelectronic Engineering, Micro and Nanofabrication Breakthroughs for Electronics, MEMS and Life Sciences **132**, 207–217 (2015).

tern transfer process. An interesting alternative would be to directly transform one of the created nanodomains in a functional material, avoiding any transfer process. This is the objective of the last part of this thesis. A technique called sequential infiltration synthesis (SIS) based on precursors typical of the atomic layer deposition is investigated for the direct formation of functional oxide nanostructures from block copolymer templates. By means of electron beam lithography, the oxide nanowires produced by SIS technique can be contacted for an investigation of the electrical and switching properties of the patterned material. The main goal of this activity is the fabrication of a test RRAM device in which both lateral and vertical dimensions of the switching oxide are scaled down to a few nanometers. This analysis can provide useful contributions for a further comprehension of the nanoscale switching mechanism and scalability potential.

Brief introduction to the chapters

The thesis is organized in self-standing chapters related to the main topics of the PhD activity. The first two chapters provide a general background on the properties of RRAM devices and an overview of previous articles on nanoscale RRAM devices fabricated by bottom-up approaches, while next chapters present the experimental work performed during the PhD activity. Finally, last chapter concludes the thesis with future perspectives based on recently achieved results and a conclusion is provided which summarizes the main findings of the PhD work.

Chapter 1 illustrates the concept of resistive switching memories and provides a classification according to switching behavior and mechanisms responsible for the resistance variation. A particular focus is devoted to RRAM based on hafium oxide in section 1.4, since this material is adopted as switching medium for the experimental work presented in this thesis. In this section, a few concepts are first introduced which are recalled in the following experimental chapters. In particular, the important role of metal electrodes and the oxide doping are here tackled based on previous literature on these subjects. Finally, this chapter briefly presents possible applications and integration schemes of RRAM devices. This final section also contains a short overview of the hallmarks of memristive systems and why they have also been identified with resistive switching memories.

Chapter 2 describes the main techniques used in the literature for the fabrication of nanoscale features from the bottom up. These methods are contextualized in the framework of resistive switching testing devices, and weaknesses and strengths of each technique are provided in order to set the basis for the choice of the fabrication method used during the PhD activity. A following section provides a review of electrical analysis and resistive switching in oxide nanostructures fabricated by bottom-up approaches. In this section contacting methods and experimental techniques used during the thesis work are here introduced for the first time in describing works from the literature.

Chapter 3 presents the experimental characterization of μm -scale RRAM devices based on HfO_2 films and Pt and TiN electrodes. This chapter is essentially divided in two main parts. First, the deposition of materials is reported and the stack is characterized by XPS analysis. Then, the chapter continues with the electrical characterization of the RRAM devices. A following section reports the effect of doping the HfO_2 film with different concentrations of Al atoms on the memory characteristics. The XPS and elec-

trical characterization of Pt/HfO₂/TiN devices was published in ref.¹⁷, while the results on Al doping of HfO₂ films were published in ref.¹⁸.

Chapter 4 addresses nanofabrication by means of block copolymer self-assembly. The chapter begins with an introduction of the block copolymer physics and self-assembly thermodynamics. Theoretical considerations lead to the diblock copolymer phase diagram, which describes the available morphologies that can be produced by block copolymer self-assembly. In this introductory part, information is given about the specific block copolymer and system configuration used during the PhD activity in order to set a background for the following description of the experimental work. The introductory sections are followed by a description of the procedure used for the patterning of ordered arrays of metal nanoparticles on the HfO₂ surface exploiting block copolymer templates. Most of the experimental results of this chapters were published in ref.¹⁹.

Chapter 5 describes the electrical characterization of nanoscale RRAM devices with controlled dimension and spacing. The production of these devices takes advantage of the block copolymer-based patterning method described in the previous chapter for the fabrication of ordered arrays of Pt/Ti nanoelectrodes. Due to the high density of the patterned features, the electrical characterization of the devices is provided by C–AFM. At the beginning, a C–AFM characterization is performed on the bare HfO₂/TiN film in order to highlight the inherent oxide variability. Afterwards, it is reported the C–AFM characterization of the patterned nanoscale devices. In this devices a crosstalk among different devices is identified during switching of the resistance. The detailed analysis of this phenomenon is the subject of the following section which concludes the chapter. Most of the results on the C–AFM characterization of nanoscale devices was published in ref.²⁰.

In **Chapter 6**, an alternative approach is investigated for the direct patterning of the functional oxide without relying on pattern transfer processes. This chapter reports preliminary data on the sequential infiltration synthesis technique after block copolymer self-assembly. This method results in oxide nanowires that can be contacted using advanced top-down techniques like electron beam lithography. These first results serve as an outlook of future works on innovative fabrication approaches based on block copolymer self-assembly for nanoscale RRAM devices.

At the end of the thesis, all the experimental techniques used throughout the previous chapters are grouped in **Appendix A**. The first sections of the appendix describe material deposition and processing methods, while the following sections briefly present the characterization techniques.

¹⁷S. Brivio et al., "Role of metal-oxide interfaces in the multiple resistance switching regimes of Pt/HfO₂/TiN devices", *Applied Physics Letters* **107**, 023504 (2015).

¹⁸J. Frascaroli et al., "Effect of Al doping on the retention behavior of HfO₂ resistive switching memories", *Microelectronic Engineering, Insulating Films on Semiconductors* **2015** **147**, 104–107 (2015).

¹⁹J. Frascaroli et al., "Fabrication of periodic arrays of metallic nanoparticles by block copolymer templates on HfO₂ substrates", *Nanotechnology* **26**, 215301 (2015).

²⁰J. Frascaroli et al., "Resistive switching in high-density nanodevices fabricated by block copolymer self-assembly", *ACS Nano* **9**, 2518–2529 (2015).

Resistive switching memories

1.1 Introduction

The continued improvement of MOS transistor performance and fabrication technology over the past decades triggered the continuous advancement of memory devices [1]. DRAM established as the standard for fast but volatile memory, while floating gate-based memories recently deep-rooted as non-volatile, massive data storage memory. Both memory types faced a tremendous improvement in cost, power consumption, and density [2]. However, memories based on traditional MOS transistors are affected by unavoidable constraints that in a mid-term perspective can severely limit their sustained development. In particular, the aggressive scaling can no longer continue in the lateral dimension due to reliability limitations and is now shifting to 3D integration [3]. Additionally, in Flash applications program times and memory wear are inherently limited by charge injection processes [4]. From an application perspective, big data centers are pushing further the demand for new application-specific memory performances that can process a huge amount of data in a short time, while on the other side mobile applications like the forecast Internet of Things demand highly low power, low cost memories [5].

To find solutions for the aforementioned demands, in the last decades there was growing interest on alternative non-volatile memory concepts. New memory solutions promise to overcome the limitations of transistor-based memories, combining fast programming with high density and low cost. A number of favorable candidate memories were proposed based on different physical mechanisms. To name a few, two (or more) logic states are associated to a change in the volume property of the switching medium from crystalline to amorphous in phase change memories (PCM), a polarization reversal in ferroelectric memories (FeRAM), and a change in magnetization in magnetic memories (MRAM) [6–8]. Among others, resistive switching memories (RRAM) emerged as a promising candidate. RRAM devices are based on a two-terminal capacitor structure, which meets the requirement of sustained scalability in particular when placed in cross-point memory architectures. RRAM are also non-volatile and offer excellent memory performance in many aspects, such as endurance and power consumption [9].

Due to the large variety of materials and mechanisms involved in different memory concepts, a large variety of device properties exists in the literature. Every type of memory has its strengths and specificities, while posing significant challenges on other sides. The novelty of these approaches is that the focus is increasingly shifting from silicon-based architectures to new materials which could offer unexplored functionalities based on new physical mechanisms. Finally, new circuit architectures based on these novel

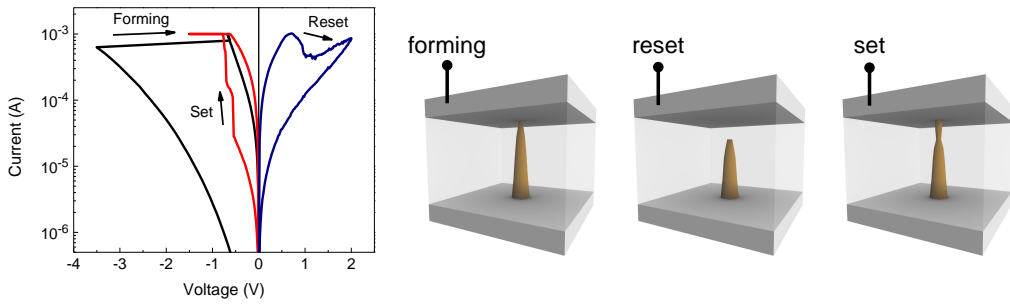


Figure 1.1: Resistance switching operations in a Pt/HfO₂/TiN cell and related pictorial view of the conductive filament formation and dissolution.

devices were developed that can perform computational tasks more efficiently than current Von Neumann paradigm. These envisioned chips can embed memory together with logic functionality or mimic the synaptic plasticity in the connection among artificial neurons for a hardware implementation of artificial neural networks [10, 11].

Resistive random access memories RRAM devices are two terminal devices with a capacitor structure in which an insulating material is enclosed between two metal electrodes, forming a Metal–Insulator–Metal (M–I–M) structure. With the application of a potential difference at the two terminals, it is possible to modify the resistance of the system in a reversible way. The switching transition from the high resistance state (HRS) to the low resistance state (LRS) is called set, while the opposite process from the LRS to the HRS is called reset. For switching to occur, the application of a potential difference above a certain threshold is required, while reading is performed by sensing the current passing through the device at a lower voltage which does not perturb the memory state. The two non volatile resistance levels can store information associated with the '0' and '1' logic states, while in case of multiple stable resistance levels also multi-bit storage is possible.

This chapter will focus on resistive random access memories (RRAM) in which the resistance switching (RS) property is due to interfacial or local change in resistivity of a restricted portion of the insulating material. In these cells, the persistent but reversible change in resistance is usually associated with the formation and partial disruption of conductive filaments inside the insulating material (see Figure 1.1 for a sketch of the filamentary model and an example of corresponding I–V switching characteristics.)

In the RS phenomenon, a dominant role is played by redox electrochemical reactions and ionic transport. Additionally, thermally-activated processes induced by joule heating can play a role, as well as electrical transport phenomena at the interfaces [12]. Filamentary RRAM devices exhibit high scalability down to 10 nm, promising write time down to the deca-nm regime, a limited amount of energy necessary to switch the cells (0.1 – 3 pJ), high stability (retention >10 years and endurance up to 10¹² cycles were demonstrated), and stackable 3D capability [1, 13].

All the aforementioned properties make RRAM a particularly interesting candidate for future high density memory applications. Further, many proposed materials can be easily integrated in the CMOS process workflow. Transition metal oxides (TMO) in par-

ticular were already actively researched as gate oxide in MOSFETs for logic and memory applications and materials like hafnium and zirconium oxide are already integrated. For this reason, hafnium oxide was chosen as switching layer for the work presented in this thesis and section 1.4 is dedicated to RRAM based on HfO_2 films.

A coarse-grained classification of the types of RRAM devices will be first made based on the voltage polarity necessary to induce the set and reset transitions. In the second instance, a subdivision will be based on the switching mechanisms associated with the variety of material stacks showing RS behavior [14, 15].

1.2 Resistive switching memories: switching behavior

Various modes of operation exist for RRAM devices. In the first instance, the switching operation can be classified in unipolar and bipolar type according to the polarity required during set and reset processes as portrayed in Figures 1.2 (a) and (b). In addition to these two broad classes, complementary resistive switching mode (CRS) sketched in Figure 1.2(c) exhibits highly non linear I-V curves that could prove useful for the integration of RRAM devices in crossbar arrays.

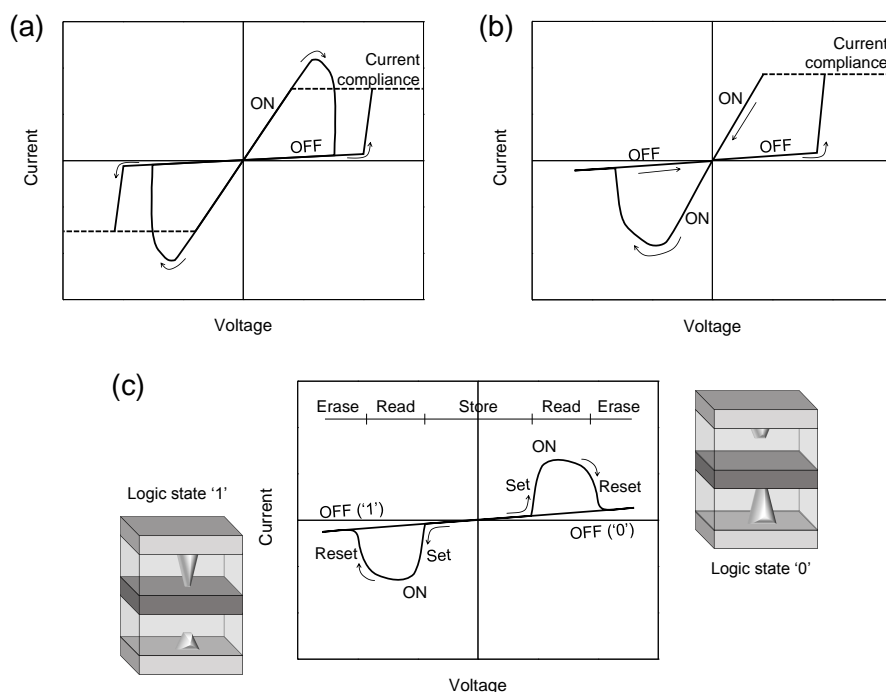


Figure 1.2: Schematic I-V curves of unipolar resistive switching (a), bipolar resistive switching (b), and complementary resistive switching (c). On the sides of picture (c), schematic representation of a physical implementation of the two logic states with two RS elements connected in series back-to-back.

1.2.1 Unipolar or non-polar

In unipolar mode, switching depends uniquely on the magnitude of the applied bias and not on its polarity. In other words, it is possible to change the resistance of the memory cell using the same bias polarity for both set and reset transitions.

In unipolar cells, usually thermochemical redox processes dominate over purely electrochemical processes, and the influence of the specific voltage polarity is less significant [16]. In most cases, an initial electroforming step is necessary to create a conduction filament (CF) in the insulating medium, as shown in the experimental I–V characteristics of a unipolar device in Figure 1.3(a). The formation takes place by local oxide reduction assisted by joule heating, while a current compliance is necessary to avoid an irreversible breakdown process which would prevent the reversible resistive switching. The conductive path can then be partially disrupted by local joule heating during reset, without the need of any current compliance. During set, the filament can be restored again by local oxide reduction in the interrupted region. The application of an external bias should be accompanied to current limitation in order to avoid hard breakdown.

Unipolar-type switching is typically encountered in transition metal oxides and NiO established as a model material, even if unipolar RS can be also observed in HfO_x-based cells [17]. Besides TMOs, unipolar switching can be encountered in cells with a Si-rich oxide switching layer [18, 19]. It is worth to notice that the switching behavior is not uniquely dictated by the insulating material, as it also depends on the symmetry of the system and on the electrodes material.

The fact that the resistivity of the device can be changed using the same voltage polarity significantly simplifies the implementation of an external driving circuitry. In addition, it makes possible the formation of 1 diode – 1 resistor (1D–1R) structures with the diode serving as selector device for the memory cell. As will be discussed in more detail in section 1.5, the introduction of a selector device is of particular importance when large crossbar array architectures are defined in order to avoid unwanted sneak paths to interfere with the determination of the memory states during reading.

1.2.2 Bipolar

The switching mode is of bipolar-type when an opposite polarity is required for set and reset transitions to occur. Typically, only one combination of switching polarities exists, depending on the specific M–I–M structure. In addition, a certain degree of asymmetry in the device structure is typically necessary to induce the bipolar operation.

The mechanism at the core of bipolar RS changes significantly depending on the type of electrode and dielectric materials. The RS variation as a function of the voltage polarity underlies a mechanism reliant on the electric field. Redox reactions and ionic transport activated by the electric field, eventually assisted by thermal contribution, should be usually considered in order to model the RS behavior in bipolar switching devices [20].

Bipolar cells usually exhibit higher memory window and lower power operation when compared to unipolar devices [8]. Another advantage is that it is often easier to achieve multiple stable and well-separated resistance levels for multi-bit operation [21].

1.2.3 Complementary switching

The CRS is a switching mode in which for both voltage polarities a set transition takes place at a particular non zero voltage threshold, while further increasing the voltage the set process is followed by a reset transition [22]. Reversing the polarity, similar set and reset processes occur, as depicted in Figure 1.2(c). Usually during CRS operation the cell is self-compliant and no current limitation is needed. The peculiarity of CRS is that by alternating positive and negative sweeps the cell can be programmed in two different reset states with high resistance. As will be shown in section 1.5, passive crossbar arrays suffer from the appearance of sneak paths and the adoption of a selector device with high non linearity is required. In devices showing CRS behavior the inherent non linearity of the memory device provides self-selection during reading and writing, hence it is immune from sneak path effects [23]. However, it is worth to mention that reading is performed in the voltage region above the threshold voltage, as depicted in Figure 1.2(c), and erases the memory state.

The CRS behavior can be realized by connecting antiseriably two bipolar devices. Four overall transitions can be identified depending in which state the two antiseriably cells are, either LRS or HRS. The '0' and '1' bits can be coded by the two states corresponding to device 1 in the LRS and device 2 in the HRS and vice versa. The two devices are in the LRS at the same time (ON state) only when the memory is read. On the other hand, the OFF state with both devices in the HRS only occurs in the pristine state after device fabrication [24].

Besides devices composed of two antiseriably bipolar cells, CRS was also demonstrated in TiN/HfO₂/TiN cells [25] and even in Pt/HfO₂/TiN cells if a proper voltage operation is applied [26]. In these cases, the CRS behavior was explained by consecutive switching at the two metal/oxide interfaces in a way similar to what happens in two antiseriably connected bipolar cells.

1.3 Resistive switching memories: mechanisms and physics

This section presents the main mechanisms that cause the switching of the resistance. A particular focus is devoted to memories in which charge-transfer redox reactions and electrochemical processes play a significant role. In particular, memories subjected to filamentary switching are given a special attention due to their relevance for technological applications [27].

1.3.1 Thermochemical mechanism

In thermochemical memories (TCM), thermochemical processes and purely thermal effects dominate over electrochemical reactions. Since thermal effects induced by joule heating do not depend on voltage polarity, TCM cells are inherently unipolar. In addition, no electrochemically active electrode is required for the switching to occur. For this reason, structures composed only of chemically inert electrodes such as Pt/NiO/Pt cells established as a model structure. However, metal electrodes can have an impact on RS behavior depending on their thermal response, as electrodes are primarily responsible for heat diffusion out of the cell.

The resistance switching is usually initiated by a forming operation (Figure 1.3(a)), a process similar to dielectric breakdown. The process is initiated by the initial leakage conduction in the oxide. The current results in joule heating, which in turns induces

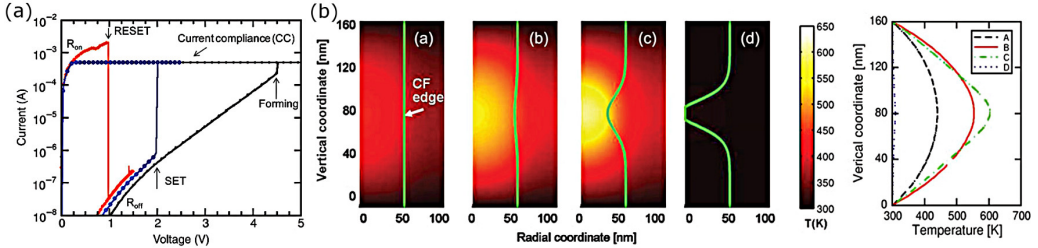


Figure 1.3: (a) Unipolar I–V curves of a Pt/NiO/Pt memory cell. (b) simulation of the thermal profile in a NiO-based cell during the reset process for increasing applied voltage, from 0.53 V to 0.87 V. Reprinted from [16].

an enhanced conductivity in a ripple effect. After a certain voltage threshold, a thermal runaway causes the creation of a highly localized conductive filament in the oxide. The main mechanisms that participate in the establishment of the filament are local thermally-activated redox reactions and phase transitions, which cause a local change in stoichiometry of the oxide. Furthermore, the strong temperature gradient between the conductive filament and the adjacent regions is likely to highly enhance the oxygen ions displacement. Redox reactions and ion movement contribute to the formation of a locally reduced and stable filament. Indeed, in many oxides *ab initio* calculations confirm the higher conductivity in the reduced oxide due to delocalized states [28].

If a proper current limitation is in place, the lateral extension of the CF can be controlled and an irreversible breakdown is avoided. During the reset process, the filament is at least partially disrupted by thermally-activated local reoxidation in the filament region. Surface tension at the filament surface may also contribute to its rupture once that an elevated temperature is reached (self-dissolution). A simulation of the temperature profile in a NiO cell during reset is reported in Figure 1.3(b) for increasing applied voltage, from 0.53 V to 0.87 V. The next set process occurs similarly to forming thanks to the high current density and temperatures achieved along the CF. Local heating results in a local thermal runaway process that reconstructs the conduction path between the electrodes [16].

1.3.2 Electrochemical metallization mechanism

Memory cells based on the electrochemical metallization mechanism (ECM), also commonly referred as conductive bridge (CB-RAM) or programmable metallization cells (PMC), are composed of an electrochemically active electrode (usually Ag or Cu), an insulating layer that serves as a solid electrolyte for the Ag/Cu ions migration, and an inert counter electrode. Figure 1.4 reproduces a typical I–V curve and a pictorial representation of the switching mechanism [29].

The basic ECM cell working principle is based on charge-transfer redox reactions taking place at the interfaces between the two electrodes and the insulating layer and on ion migration. During the initial electroforming step and the subsequent set operations, the active electrode is oxidized by the application of a positive potential. Subsequently, the positive cations migrate under the influence of the applied electric field toward the counter electrode, where they are reduced. This leads to the formation of a metallic filament made by atoms coming from the active electrode inside the insulating material, which is responsible for the cell switching to the LRS. During the reset process, the

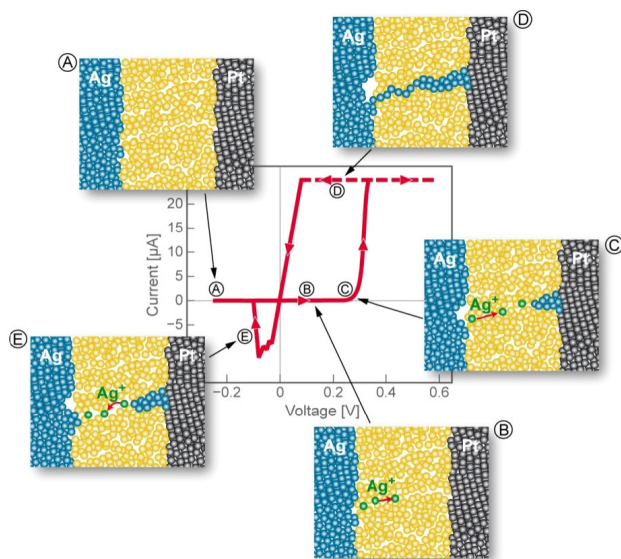


Figure 1.4: Typical I-V characteristics of an ECM cell and associated pictorial view of the filamentary processes involved in the resistance switching. Reprinted from [29].

application of an opposite voltage polarity induces the ions migration in the opposite direction, disrupting the conduction filament entirely or in part. The reset mechanism is supported by charge-transfer reactions taking place at the boundary of the metallic filament, causing its oxidation. However, depending on the current level reached during reset, also joule heating may occur, and thermal contributions may be responsible for the filament self-dissolution in a way similar as previously described for TCM cells. This mechanism was postulated since reset independent from the voltage polarity was obtained in some systems. In addition, redox reactions can be thermally-enhanced by joule heating once that a sufficient current density is established in the cells, marking the onset of the reset process.

ECM cells are inherently bipolar, since both charge-transfer and ion migration processes are activated by the electric field. However, also thermal contributions can be relevant due to the highly localized nature of the filament, which causes high current densities along its path. Other rate-limiting processes include the overcoming of an energy barrier for ions injection at the anode/insulating material interface, a nucleation process at the inert cathode prior to filament growth, and the overcoming of a mechanical stress during filament growth in the insulating matrix. All these processes can be the limiting factor for the switching time depending on the materials used and on the specific voltage range.

One of the advantages of ECM cells is the wide memory window. A ultrahigh ON/OFF ratio of 10^7 was reported [30]. Because of this wide window, multiple stable states for multi-bit data storage are easy achieved. LRS can be tuned by controlling the maximum current during the initial forming and the set operations. When a sufficiently low compliance current is applied, several indication exist that the filament does not extend throughout the film thickness, thus a galvanic contact between the two electrodes is not achieved. Indeed, a quantized conductance was measured for multiple LRS states,

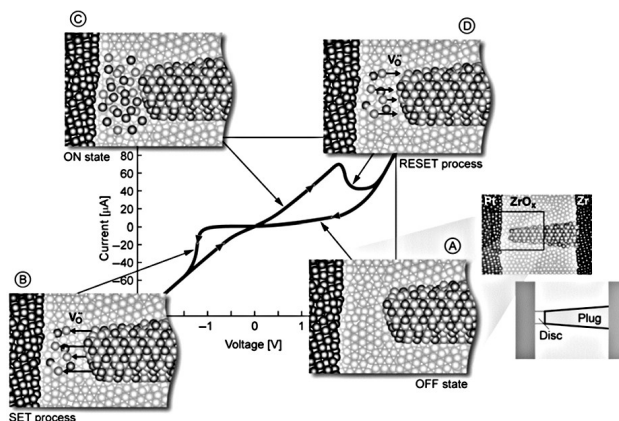


Figure 1.5: Typical I-V characteristics of a VCM cell and associated pictorial view of the filament formation and dissolution processes involved in the resistance switching. Reprinted from [13].

which points toward the existence of a tunneling gap between the metal filament and the active electrode. The modulation of this gap extension is responsible for the multiple stable resistance levels [13].

Another remarkable advantage of ECM cells is the comparatively low switching power. While the set current can be varied over almost 10 decades, extremely low set current down to 10^{-12} A was demonstrated in SiO_2 -based cells. Other advantages concern a fast switching time below 10 ns and possible scalability down to the atomic level. Indeed, a quantized conductance atomic switch was reported [31].

1.3.3 Valence change mechanism

Memories based on the valence change mechanism (VCM), similarly to ECM cells, are based on redox reactions and ion migration in the insulating dielectric material. Nevertheless, unlike ECM, in VCM cells no extrinsic material is diffusing in the dielectric layer, and the RS phenomenon is associated to a local valence change of the cation sub-lattice due to oxygen vacancies, highly enhancing the electrical conductivity [32, 33].

The VCM phenomenon was reported in oxide materials, principally transition metal oxides (TMO), and in perovskites. Among others, HfO_x and TaO_x -based cells are the most studied systems, in association with various electrode materials. Two main classes can be identified according to the localization of the conduction path: interface-type and filamentary-type switching. In the former, the RS switching phenomenon is due to formation and eventual migration of oxygen vacancies at the interface with the cathode, changing the potential barrier for electrons. Conversely, in filamentary-type VCM cells, the initial forming operation induces the creation of an oxygen-deficient filamentary path, with localized conduction [34]. This latter mechanism is the most commonly studied, due to the high scalability and thus potential interest for high density memory applications. A pictorial representation of the filament formation and disconnection inside the cell is reproduced in Figure 1.5 along with a typical bipolar I-V curve [13].

Even if filamentary-type cells are actively investigated and subject of great interest, many aspects of the actual physical processes involved in the CF formation and dissolution remain unclear. The enhanced conductivity obtained with forming operation is

explained as a recoverable electroforming step, also called soft breakdown. In many models, the filament formation is explained by formation of oxygen vacancies due to cation–oxygen bond breakage and subsequent vacancies migration in the film. An alternative picture deals with the migration of the oxygen interstitials, while vacancies are expected to remain fixed. The actual physical forming mechanism also depends on the temperature reached locally along the filamentary path, which could highly enhance bond breakage, charge-transfer reactions and ion migration [35].

As for ECM and TCM cells, a current limitation during forming and set transitions is able to control the lateral extension of the filament and avoids an irreversible hard breakdown, allowing the cell to revert to the HRS. The reset process consists of an oxidation of the reduced cation sub-lattice. This could either happen by motion of the oxygen vacancies (Figure 1.5) or by their recombination with oxygen ions. Since in most cases the HRS resistance is lower than in the pristine state, the filament is probably not completely annihilated during reset. Additionally, since the subsequent set voltage is almost independent from the thickness of the film, most models consider the opening of a small (<2 nm) tunneling gap in the CF upon reset [36]. During set, only this portion of the cell is involved in the recreation of the filament.

One of the main advantages of VCM cells is the stability of the achieved resistance states. Long retention times over 10 years even at fairly high temperatures were demonstrated, together with endurance exceeding 10^{12} switching cycle. Furthermore, fast switching times <10 ns and a low power consumption <0.1 pJ were reported. VCM cells are also suited for multi-bit operation in a similar way to ECM cells. However, for both types of cell the variability for repeated cycles and among cells still remains an issue and could possibly prevent the correct determination of the multiple resistance levels.

Finally, it is worth to mention that it was recently demonstrated that in many transition metal oxides the host metal cations can be mobile and be subjected to oxidation and reduction reactions similarly to ECM cells. This observation builds a bridge between ECM and VCM cells, with a competition between the two mechanisms depending on the cell structure and electrical operation. The same cell was also changed from VCM to ECM operation mode by adding a proper interlayer in the stack [37].

1.4 Resistive switching in hafnium oxide

Transition metal oxides (TMOs) are largely employed as switching material in RS devices based on cation diffusion from the anode or valence change mechanism [32, 34]. The deposition of many TMOs is now a mature technology thanks to the progress in physical and chemical deposition methods. Atomic layer deposition (ALD) established as one of the most interesting techniques since it allows an accurate thickness control, optimal film quality, and low temperature deposition. Not secondarily, the high conformality of ALD allows the deposition in patterned samples with high aspect ratio features and along vertical edges, which significantly extends the range of possible applications. Given its many advantages, ALD was the method chosen for the deposition of HfO_2 films during the PhD activity.

Many TMOs can be easily integrated with CMOS process technology and, when deposited at sufficiently low temperature, memory devices can be integrated in the back end-of-line (BEOL) of the integrated circuits processing. Two of the most mature TMO insulating materials for RRAM applications are hafnium oxide and tantalum oxide. In Table 1.1, a summary is drawn of the best performance values achieved for VCM and

ECM types of RRAM devices, in which both HfO_x and TaO_x memories are inserted for comparison.

Table 1.1: Comparison of best performance values reported for various RRAM cells. HfO_x and TaO_x memories were compared since they are the most mature insulating materials for oxide-based RRAM. The values are only exemplary since they also depend on the actual switching parameters and stack engineering. Data in the table is extracted from [13, 38, 39].

	HfO_x	TaO_x	Best ECM
Minimum feature size	~ 10 nm	~ 10 nm	< 10 nm
Switching time	~ 5 ns	< 200 ps	< 10 ns (Ag-MSQ)
Endurance	10^{10}	$> 10^{12}$	$> 10^{10}$ (Ag-GeSe)
Retention	> 10 y	> 10 y	> 10 y (Ag-chalcogenide)
Memory window	> 100	> 100	10^6
Max operation current	~ 25 μA	~ 20 μA	~ 10 μA
Minimum switching voltage	~ 1 V	< 1.5 V	< 0.5 V (Ag-chalcogenide)

HfO_2 among others recently established as a model material for VCM-based memory cells. The HfO_2 oxide was actively investigated for its integration as high- k gate material in field-emission transistors and, for this reason, a wealth of knowledge exist about the deposition and electrical properties of this material.

HfO_2 -based bipolar devices exhibit fast switching transitions, comparatively low power consumption, and high filament stability. Due to its many advantages and relevance for memory applications, the work presented in the following chapters uses HfO_2 as switching material. Before going into the details of the experimental characterization, it is worth to consider separately the many elements composing the M-I-M stack and the relative interfaces, taking examples from the literature. This will allow to better understand the peculiarities of HfO_2 -based RRAM devices and how it is possible to engineer its properties.

1.4.1 Evidences of filamentary switching

Several indications exist of filamentary conduction paths in RRAM memory cells. In the first instance, in filamentary-type cells the LRS resistance as well as switching parameters do not vary significantly as a function of cell area. Moreover, filamentary-based models can successfully reproduce I-V characteristics and dynamics [12, 40], explain the multiple memory states [41], and predict reasonable data for the filament lateral extension and profile [42]. Besides indirect confirmations, a direct experimental characterization proves difficult due to the highly localized nature of the CF, which requires advanced and high resolution techniques. Nevertheless, some experimental investigations confirmed the presence of a metal-rich regions in TMO-based cells and were able to determine shape and dimension of the conductive region.

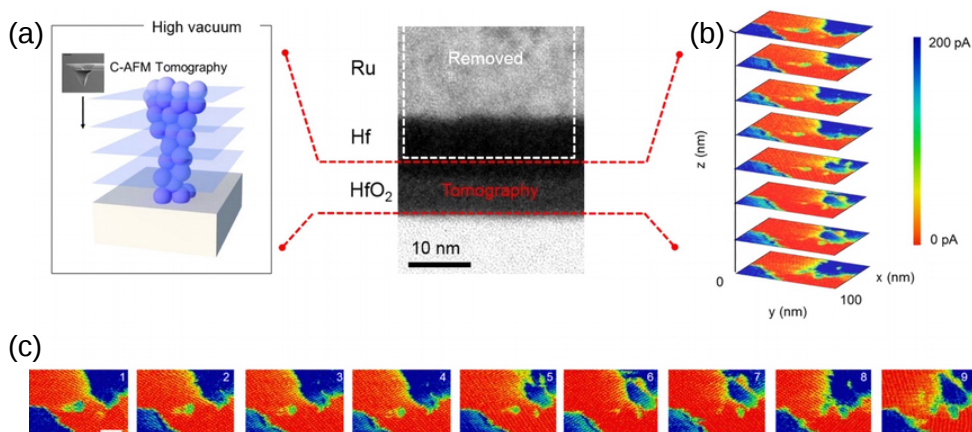


Figure 1.6: Evidences of filamentary CF in HfO₂-based memory cell by C-AFM-assisted 3D tomography. (a) Schematic of the C-AFM tomography procedure which uses a diamond tip to as a scalpel to remove thin layers of the oxide while acquiring current images of the conduction across the layer. (b) Stacked images of the conduction across the HfO₂ layer. The average spacing between slices is 0.2 nm. (c) Top view of current images through out the device. The scale bar corresponds to 20 nm. Reprinted from [46].

Many C-AFM investigations of the surface of HfO₂ and other TMOs confirm the presence of a localized conduction along grain boundaries in nanocrystalline materials or in localized spots in amorphous films [43]. Therefore, grain boundaries or local accumulations of defects in the oxide are expected to facilitate the soft breakdown process and concentrate the conduction in the dielectric. The local investigation of selected conductive regions of the surface by the sharp C-AFM tip allowed to obtain I-V characteristics similar to those obtained in μm -size cells and confirm the local nature of the RS phenomenon [44].

An investigation of the CF lateral size and shape however requires an analysis throughout the oxide thickness. At this scope, Celano et al. performed repeated scans using hard diamond-coated tips in order to remove the oxide in a layer-by-layer approach. Using this method, they were able to reconstruct 3D current maps throughout the oxide film thickness with nanometric resolution [45, 46]. Figure 1.6 shows current images obtained in a HfO₂-based cell in which a single conductive filament with conical shape is clearly visible. The filament has a lateral size below 10 nm and presents a constriction close to the oxygen-inert electrode.

Scanning tunneling electron microscopy (STEM) is probably the most advanced imaging technique for highly scaled devices and allows a resolution down to the atomic level. Additionally, when combined with electron spectroscopy techniques like EELS (electron energy loss spectra) it is possible to reconstruct 2D maps of the chemical composition and to investigate the chemical and electronic changes involved in the resistance switching mechanism. However, one of the key challenges is the localization of the CF in the cell. Calka et al. [47] took advantage of the C-AFM technique to induce electroforming in a HfO₂/TiN film and used the same instrument to detect the filament location for the subsequent preparation of the cross-section. Using the STEM technique they identified a protrusion in correspondence of the filament location (Figure 1.7(a)) and a localized oxygen deficiency in the HfO₂ layer (Figure 1.7(b,c)). Further punctual EELS

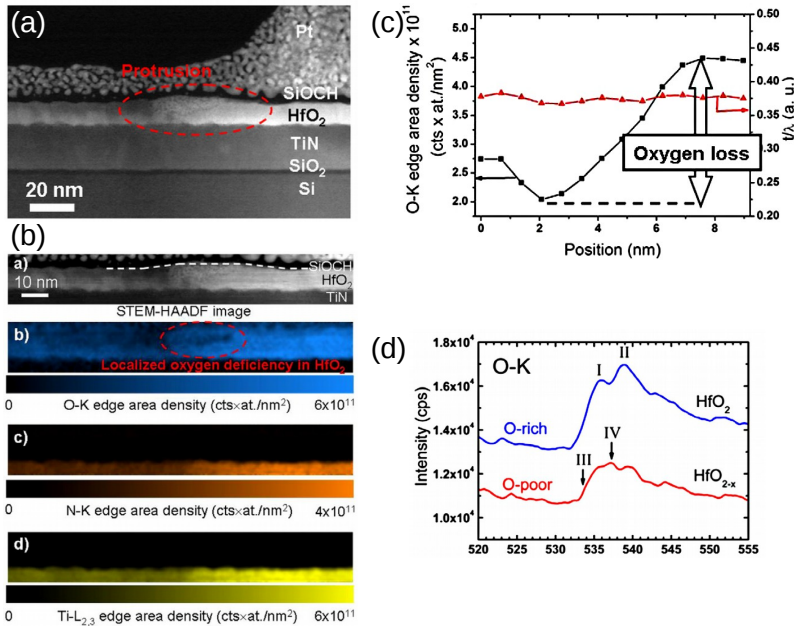


Figure 1.7: Evidences of filamentary CF in HfO_2 -based memory cell by STEM analysis. (a) STEM image of the region containing the conduction path. A protrusion can be evidenced after forming operation. (b) Detail of the conductive region. A localized oxygen deficient region can be identified in this area by EELS chemical analysis. (c) A graph of the EELS chemical map reported in (b) for the O-K edge further proves the oxygen deficiency. (d) Electron energy spectroscopy along the O-K edge can distinguish between O-rich and O-poor regions inspected by STEM. Reprinted from [47].

spectroscopy, reported in Figure 1.7(d), confirmed the existence of a sub-stoichiometric oxide in correspondence of the protrusion.

Privitera et al. performed a similar STEM and EELS analysis on nanoscale ($50 \times 50 \text{ nm}^2$) cells with 5 nm thick HfO_2 [48]. Even if the spatial resolution did not allow to establish the exact shape of the filament, a Hf-rich region roughly 10 nm in size was identified, which narrowed toward the cathode. Interestingly, also Ti diffusion in the HfO_2 layer could not be excluded.

1.4.2 Role of the metal electrodes

The metal electrodes constitute an active part of the ReRAM device stack and can determine the switching behavior. In bipolar devices, an asymmetric stack material is often required and the specific device stack can determine the switching polarity. As an example, when a noble metal is present at one side, forming and set operations occur for a negative voltage applied to this electrode [49]. The electrode type can additionally affect the device yield and the dispersion of the switching parameters [50].

An important aspect to be considered as regard to the switching operations is the electrodes work function, which contributes to the energy bands bending at the metal/oxide interfaces. High work function materials such as Pt can induce a barrier at the oxide interface and affect carrier injection, while low work function metals such a Ti can

establish an ohmic contact [51].

An important role is also played by the electrodes ability to dissipate thermal energy, especially when thermal effects are involved in the resistance switching. Indeed, the exponential dependence of activation on temperature implies that even small changes in the temperature dependence can have significant impact on switching. In general, a thermal conductivity that is inversely related to temperature is preferred for fast switching and long retention time. This desirable property can be found for example over a wide range of temperatures in the often applied TiN electrode, while in Pt thermal conductivity has the opposite trend [52].

Pt is commonly applied as electrode material in HfO₂ RRAM and offers good performance and low dispersion among devices when used as anode in the reset operation. This property could be related to its catalytic activity for redox reactions at the interface [49]. However, Pt was found to be permeable to oxygen during switching [53]. This peculiarity can cause reliability issue due to oxygen depletion without the insertion of a proper oxygen gettering interlayer.

An important effect is played by the oxygen scavenging ability of the metal electrode. Materials with high oxygen affinity like Ti or Hf can react with the oxide film and build-up an oxygen-deficient layer at the metal/oxide interface. This region facilitates the generation of oxygen vacancies and eventually serves as a reservoir for vacancies during switching [54]. RRAM engineered with an oxygen scavenging layer demonstrated a reduced forming voltage [55] and superior memory performance [56]. Additionally, the insertion of a Hf scavenging layer at the interface between the HfO₂ layer and the TiN bottom electrode was observed to have a significant impact on the electrons barrier height due to positively charged defects [57]. This effect can be used to lower the barrier height and improve resistance switching properties [58].

When designing the material stack, metal diffusion should be considered depending on the processing temperature. As an example, a Ti adhesion layer located below the Pt electrode was found to easily diffuse up through Pt after annealing, reducing the overall work function. When Ti arrived in contact with the oxide film, it locally seeded the filament formation [59].

1.4.3 Switching variability

One of the major drawbacks of filamentary resistive memories is the inherent variability caused by the stochastic mechanisms that control the filament growth and dissolution. The CF occupies only a very small portion of the device volume and the number of atoms in it is rather low, in particular when the device is operated at low current. For this reason, the chance that exactly the same filament is reconstructed and dissolved at every cycle is quite low. The problem is further complicated by the various stochastic processes involved in the switching of the resistance, that add randomness to the switching parameters and resistance levels. This issue is especially critical for the HRS distribution, since during reset no extrinsic limitation is applied to the cell, unlike set operation in which a current limitation is usually applied [61].

Various approaches were used in the literature to model the programming variability in filamentary HfO₂ RRAM devices. Ambrogio et al. [60] simulated the stochastic filament formation by assuming a random variation of the activation energy for vacancies diffusion and injection in the filament. Figure 1.8(a) displays the atomistic description of the filament at the basis of this model along with the random activation energies simulated for various defects.

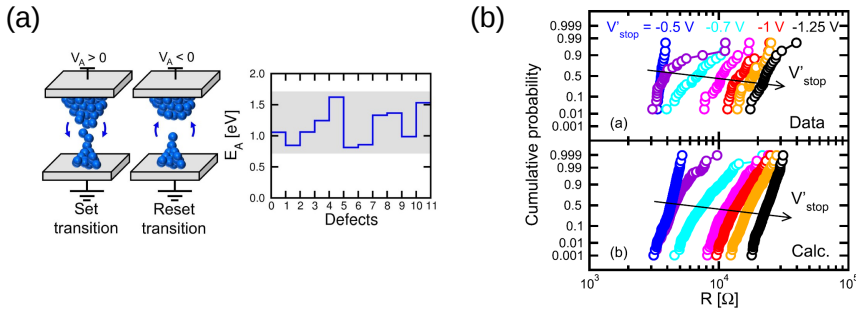


Figure 1.8: Monte Carlo simulation of the switching variability modeled by assuming a random variation of the energy barrier for defects (oxygen vacancies) injection in the filament. (a) Schematic of the filament during set and reset transitions and simulated activation energies. (b) This simulation can correctly reproduce the HRS log-normal distribution spreading for increasing reset stop voltage in HfO₂-based RRAM. Reprinted from [60].

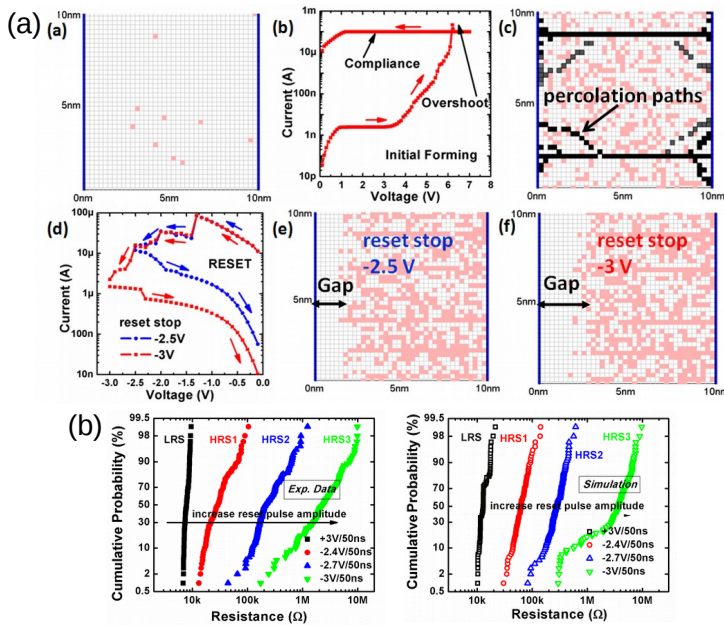


Figure 1.9: (a) Monte Carlo simulation of random filament formation in a $10 \times 10 \text{ nm}^2$ HfO₂ cell during forming and reset processes. (b) This model can reproduce the experimental log-normal resistance distribution spreading for increasing reset pulse amplitude in HfO₂-based RRAM. Reprinted from [62].

A different method was adopted by Yu et al. [62]. They used Monte Carlo simulations to directly model the formation of a random conduction path in a $10 \times 10 \text{ nm}^2$ two-dimensional cell in which oxygen vacancies can diffuse randomly. Figure 1.9(a) displays a sketch of the simulation results starting from the initial state, after set, and after reset with two different reset stop voltages.

Although based on different assumptions, both simulation approaches described

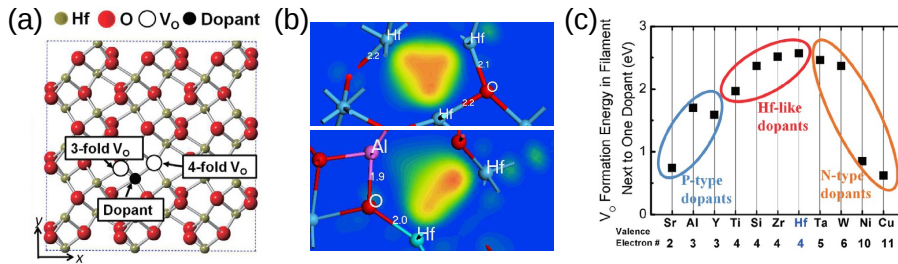


Figure 1.10: (a) HfO₂ supercell containing oxygen vacancies and a dopant atom. Reprinted from [66]. (b) Wave function contour plot for the gap-state in correspondence of oxygen vacancy sites in undoped (top) and Al-doped (bottom) HfO₂ films. Reprinted from [67]. (c) Average formation energy for oxygen vacancies in a CF for a HfO₂ film with different dopants. Reprinted from [66].

above are able to correctly simulate the log-normal resistance distribution that is experimentally measured for the HRS. In addition, they can reproduce the distribution spreading obtained by increasing the amplitude of the reset voltage (Figures 1.8(b) and 1.9(b)).

One method to reduce the device variability is to implement write–verify schemes. A similar approach is to carefully control the stress time during pulse programming by adjusting the pulse width [63]. These methods however highly complicate the external circuitry necessary to pilot the memory array and increase the overall write time.

1.4.4 Oxide doping

Doping the memory oxide is a viable way to engineer its property for improvement of the memory performance and reduction of device variability [64]. In particular, in HfO₂ films doping was actively investigated as a way to mitigate the variability issue and improve the filament stability [65].

Figure 1.10 shows a typical supercell containing a dopant atom and oxygen vacancies inside the HfO₂ lattice. This structure was at the basis of *ab initio* density functional theory (DFT) calculations in ref. [66]. For the special case of trivalent atoms, a charge transfer occurs to Hf valence orbitals and a delocalized band appears in the density of states as shown in Figure 1.10(b) [67]. The enhanced conductivity caused by delocalized states around doping sites can facilitate the formation of a stable conductive filament. As general selection rule in HfO₂ films, doping elements can be distinguished into p-type, n-type, and Hf-like dopants. The first two classes can be used to reduce the formation energy for oxygen vacancies, leading to more stable filaments and lower forming/set voltages [68] (Figure 1.10(c)). In case of a uniform distribution of doping atoms across the film, a reduced variability is also predicted due to the more reproducible filament formation [28].

The performance improvement associated with oxide doping should be verified with special care, since several side effects can arise upon doping. More specifically, in HfO₂ films Zhao et al. [66, 69] reported that a reduction of the forming voltage, probably associated with the easier formation of oxygen vacancies, is accompanied by a reduction of the ON/OFF ratio as a consequence of a reduced HRS resistance. This trend is reported in Figure 1.11(a) for various dopant atoms. Another cause of performance degradation can be caused by an enhanced vacancies mobility in the doped films. Figure 1.11(a) shows

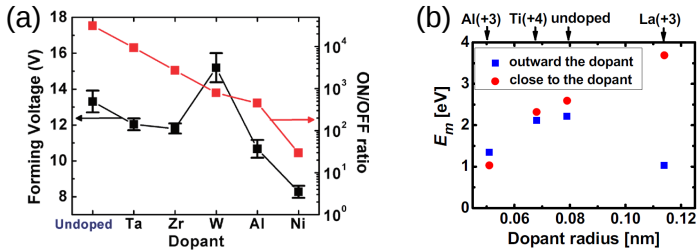


Figure 1.11: (a) Changing the dopant atom from Ta to Ni, as the forming voltage decreases, the ON/OFF ratio also reduces. Reprinted from [66]. (b) Doping the HfO₂ film also reduces the energy barrier for migration of oxygen species. Reprinted from [67].

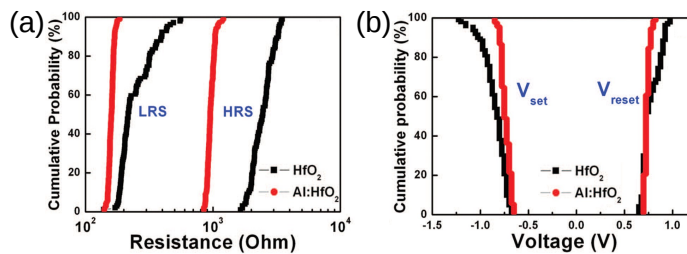


Figure 1.12: Improvement of resistance distributions (a) and switching voltages (b) by Al doping of a HfO₂ film during ALD growth. Reprinted from [70].

the result of DFT calculations for the energy barrier for the migration of oxygen species [67]. While an enhanced mobility can facilitate the filament formation, it can also be responsible for a faster loss of the memory state over time due to vacancies out-diffusion from the filament. These implications of oxide doping will be better discussed in chapter 3, in which a trade-off will be identified between uniformity improvement, ON/OFF ratio, and retention degradation as a function of Al doping concentration.

The trivalent Al atom was identified as one of the best choices for variability improvement in HfO₂-based memories due to its trivalent nature combined with a low atomic radius which reduces lattice distortion [67]. Various techniques were applied to introduce Al atoms in the oxide film. The annealing of Al/Hf/Al multilayers in O₂ ambient resulted in Al-doped HfO₂ films with almost uniform Al content [71]. The resulting memory cells exhibited a significant reduction of the switching voltages variability, together with a sizable improvement of LRS and HRS distributions. However, the HRS distribution was shifted to more than an order of magnitude lower values closing the memory window. A similar result was obtained doping the oxide layer during the ALD growth of the film by alternating Al₂O₃ and HfO₂ growth cycles, as reported in Figure 1.12 [70]. Moreover, after Al incorporation the LRS retention was greatly improved by an increased thermal stability of the filament [72]. The ALD technique used in these studies is preferable since it allows a more uniform incorporation of Al atoms across the film and permits an optimal film quality even for low thicknesses below 10 nm [73–75]. Moreover, a post deposition annealing can be avoided. For all these qualities, ALD deposition is the adopted deposition method for the experimental work presented in this thesis in chapter 3.

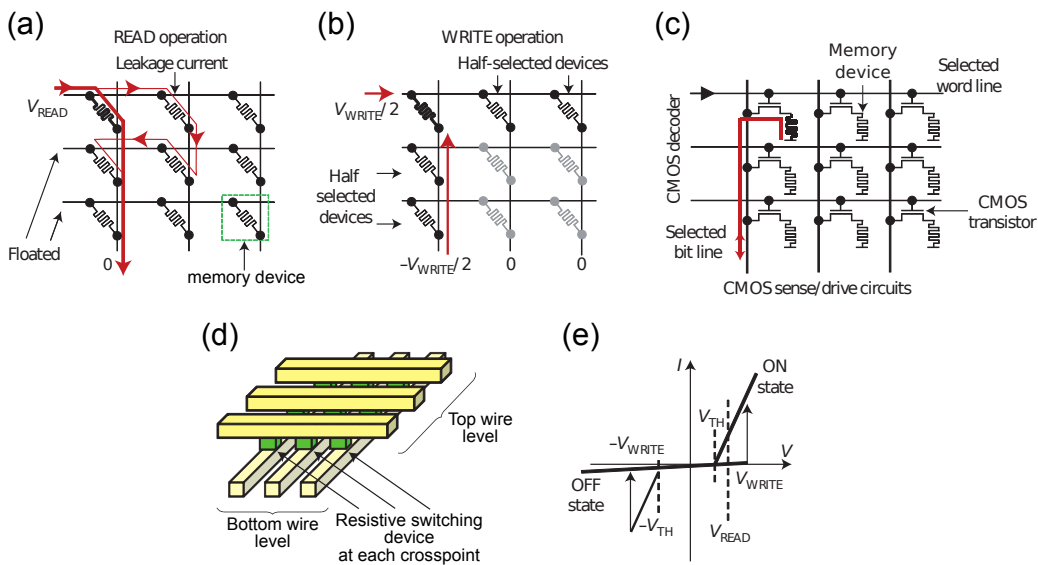


Figure 1.13: Crossbar array of resistive switching memory devices. (a) Without any selector device, a sneak path passing through other devices in the ON state is illustrated. (b) A disturbance can occur to other half-selected devices in the array during write operations. (c) Illustration of the 1T-1R architecture designed to avoid sneak paths and write disturbance issues. (d) Pictorial view of a crossbar array structure with memory devices at the crosspoint of top and bottom lines. (e) Illustration of a highly non-linear device that does not require a selector device. Reprinted from [11].

1.5 Applications and integration schemes

One of the biggest advantages of RRAM memories is the presence of only two terminals. For this reason, they can be easily integrated in crossbar array structures. For a given feature size (F) allowed by the given lithographic technology, the crossbar structure permits the highest possible device density, in which every device has a footprint of only $4F^2$. When filamentary-type memories are involved, F can be made as small as <10 nm, making in theory feasible densities up to 10^{12} devices/inch². Moreover, additional layers can be stacked in the vertical direction to further increase the areal density [76].

As sketched in Figure 1.13, large crossbar arrays however suffer from the appearance of sneak paths. In practice, when a small bias is applied between two selected word and bit lines to read the state of a cell, the presence of many devices in the LRS state causes additional possible sneak current paths that add up to the total current count, potentially causing a read disturb (Figure 1.13(a)). Moreover, in some occasions a disturbance can also occur during write operations as depicted in Figure 1.13(b).

The most straightforward solution to the sneak paths problem is to implement devices with an intrinsic high non linearity. As an example, CRS devices were proposed. However, as the number of devices in the crossbar array grows, the degree of non linearity should increase accordingly, which is hard to reproduce in practice. An additional solution involves the insertion of a selector device in series with the resistive memory (1S-1R), such as a diode (1D-1R) or a transistor (1T-1R). A scheme of the 1T-1R architecture is reported in Figure 1.13(c). While the insertion of a diode could retain the

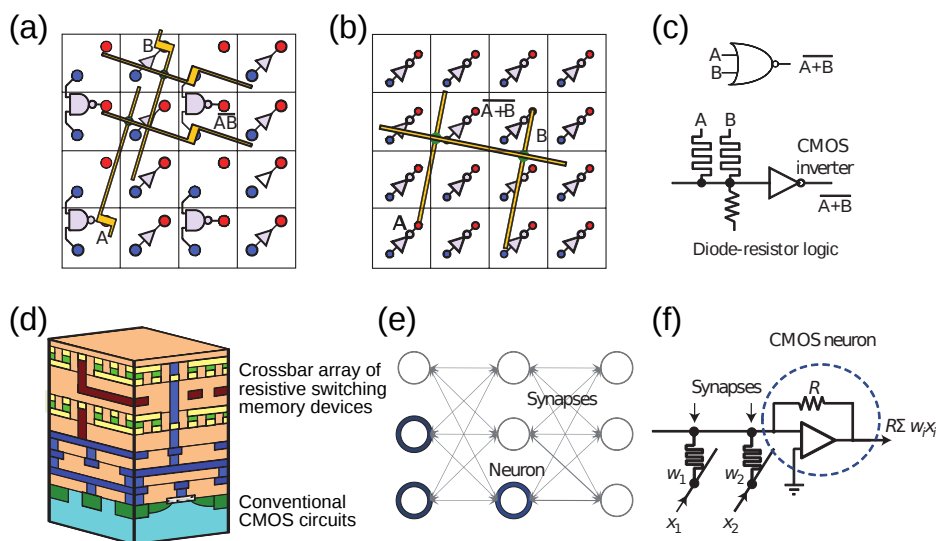


Figure 1.14: Illustrative applications of resistive switching devices. (a) Programmable logic array. A layer of RS devices serves as reprogrammable interconnects above a CMOS layer with logic gates. (b) In addition to serving as interconnects, RS devices can implement logic functionality alone or in combination with other devices. (c) Example of hybrid NOR logic gate. (d) Integration scheme of a crossbar array of RS devices on top of CMOS circuits. (e) Schematic of multiple interconnections with synaptic functionality between neurons. (f) Practical implementation of the interconnections between CMOS neurons with RS devices. Reprinted from [11].

high density of the crossbar design, the implementation of a series transistor inevitably increases the memory footprint, though it can reveal useful also as current limiting element during set operations.

Aside from memory architectures, RRAM devices can be integrated in other more advanced configurations for logic applications [24]. Some examples are shown in Figures 1.14(a–c). In many concepts, passive two-terminal RRAM devices are combined with active CMOS elements in a hybrid configuration to unite the benefits of both. As an example, reconfigurable logic circuits were proposed. As illustrated in Figure 1.14(a), RRAM devices are placed at the crosspoint between lines and serve as programmable interconnections above a CMOS layer with gate and buffer circuits [77]. A cross-section of this integration scheme is shown in Figure 1.14(d).

RRAM devices themselves can implement totally or in part the logic gate functionality [11]. In combination with one diode, the high non linearity of two RRAM devices can be exploited for the realization of the NOR logic gate (Figure 1.14(c)). Alternatively, arbitrary logic computation was demonstrated using only RRAM devices for the implementation of the NAND gate by combining material implication and not operations. In these schemes, the same devices can serve simultaneously for logic gates and on-chip memory, using the internal resistance as the physical state variable instead of voltage or charge [10]. This approach was recently extended to HfO_2 -based CRS crossbar arrays, which avoid the introduction of a selector device. multi-bit crossbar adders were experimentally demonstrated by performing addition and subtraction operations, proving that computing-in-memory architectures can achieve both high density and highly efficient computation [78].

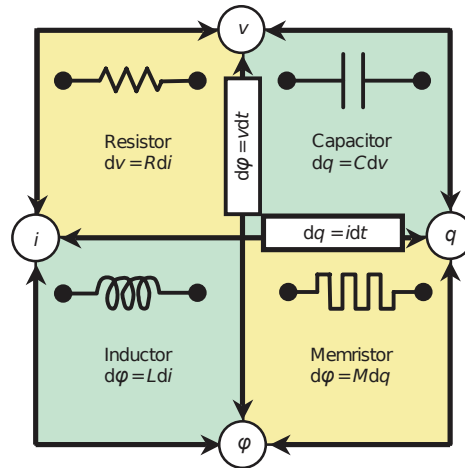


Figure 1.15: Conceptual symmetries of passive circuit elements: resistor, capacitor, inductor, and memristor. Reprinted from [81].

Finally, hybrid implementations were proposed for the formation of neuromorphic circuits. A schematic of this concept is reported in Figures 1.14(e,f). When RRAM devices are especially engineered to exhibit almost continuous multi-level states, they can reproduce the synaptic functionality [79, 80] and serve as variable weight at the interconnections between CMOS neurons. For this purpose, the very high density achievable by RRAM crossbar arrays is ideally suited for the fabrication of artificial neural networks.

1.5.1 Resistive switching device as memristor: the fundamental circuit element

A two-terminal passive element called *memristor* (*i.e.* memory resistor) was first theorized by Leon O. Chua in 1971, driven by symmetry argumentation [82]. This kind of fourth fundamental circuit element closes the relational circle between passive devices (resistors, capacitors, and inductors), establishing a relationship between the electric charge $q(t)$ and the magnetic flux-linkage $\varphi(t)$ of the device (Figure 1.15).

From symmetry reasoning, a link can be identified between $q(t)$ and $\varphi(t)$

$$d\varphi = M(q) dq$$

$M(q)$ is called memristance and is dimensionally equivalent to the electrical resistance. Since $d\varphi = v dt$ and $dq = i dt$, the integral relationship becomes

$$\int_{-\infty}^t v d\tau = \int_{-\infty}^t M(q(\tau)) i(\tau) d\tau$$

In case that M does not depend on q , the equation simply reduces to the linear relation of a time-invariant resistor, with $M = R$. However, since in general M is not constant but depends on $q(t)$, the above equation describes a non-linear device in which the time integral of the voltage is connected to the time integral of the current. The voltage across a charge-controlled memristor can be written as $v(t) = M(q(t)) i(t)$, with $M(q) = d\varphi(q)/dq$. The memristance changes over time according to the current that had

passed through the device, hence the memristor has a non-volatile memory effect which persists even when the external bias is removed.

In 1976, the basic definition by Chua was generalized to a broader class of non-linear dynamical systems, the so called *memristive systems*. Memristive devices are defined by a set of state variables describing its state and as a consequence the flux-linkage in is no longer uniquely defined by the charge passed through the device. The following set of equations needs to be satisfied for a charge-controlled memristive system:

$$v = M(w, i) i$$

$$\frac{dw}{dt} = f(w, i)$$

where M and f are in general variable in time and f is any linear or non-linear function. Being a generalization of memristors, memristive systems belong to the class of non-linear dynamical devices and the current state of the device depends on the history of the current through it. Additionally, the device state is completely defined only by assigning initial state conditions.

General features of memristive systems can be identified in the I–V characteristic and mark a distinction from other dynamical systems. First, the I–V curve should be pinched to the origin, since when the voltage goes to zero the current must go to zero accordingly. Further, the non linearity and the inherent memory of the system in many cases produce a hysteresis loop in the first and third quadrants of the graph.

From a practical point of view, bipolar RRAM devices show very similar I–V characteristics and were found conform to the generalized memristive model once that a correct set of state variables is defined. A direct connection between the memristive description and the physical properties of the system was first draw by Strukov et al. for a Pt/TiO₂/Pt memory device [81]. Many dynamical models proposed to describe the RS behavior are now based on the memristive system state equation [13], establishing a theoretical framework for research on RRAM and logic devices. In addition, these simple models make it possible to design and predict complex circuits, for example when implementing learning rules in neuromorphic circuits.

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Bottom-up fabrication approaches for nanoscale resistive switching devices

2.1 Introduction

The self-organization of features into organized patterns is of great technological relevance for a broad range of devices, notably in the field of nanoelectronics. As opposed to conventional and subtractive top-down lithography, the construction of devices from the bottom-up is based on self-assembling processes and laws which bring together constituting elements in regular patterns and can be found in nature at all scales, from crystal structures to galaxies[1].

Bottom-up fabrication approaches hold the promise of overcoming the limitations of lithography for the formation of circuits and devices at extremely small scales and with high density, eventually leading to molecular devices. At the laboratory scale, bottom-up methods offer the possibility to test novel materials and device concepts and to study the resistive switching (RS) properties at a scale not easily accessible by conventional patterning techniques [2].

Some of the most interesting building block for nanoscale resistive switching devices are nanowires (NWs), nanorods, and nanodots. They can be fabricated by a number of different bottom-up methodologies, either assisted by self-assembled templates or by growth techniques leading to the formation of the required element. The exploitation of these building blocks can bring novel physical properties. However, their assembly in original devices with new functionalities, in particular when high density structures are involved, is extremely demanding in terms of accurate positioning and external addressing of the individual features. In this contest, the synergistic integration of top-down and bottom-up techniques can speed up the integration of bottom-up technologies and allow advanced device structures combining the strengths of both methods [3, 4].

This chapter will first introduce some of the most promising techniques for the fabrication of ordered arrays of nanoscale structures by bottom-up techniques. At a later stage, the investigation of RS devices is considered, with a particular focus on nanoscale characterization. This chapter is preparatory to the work presented in this thesis and is intended as an overview of possible fabrication techniques and analysis of nanoscale devices from previous literature. Directed self-assembly (DSA) based on block copolymers is here anticipated in a brief paragraph and will be discussed in greater detail in chapter 4.

Toward crossbar array architectures For resistive switching memories, crossbar array structure is the ultimate structure of choice, since it allows the highest packing density allowed by the pattern resolution of the adopted technology. In addition, multiple superimposed layers of memory devices can be combined, exploiting also the third dimension and further enhancing the areal density.

NWs are promising building blocks for future high density applications. In particular, core-shell NWs can integrate both contact line (core) and switching layer (shell) in the same bottom-up process. However, several challenges remain to be solved. In large crossbar arrays, sneak paths due to active low-resistance cells rise the current passing between two considered lines, eventually hindering the reading capability. Furthermore, the correct addressability of each cell requires a precise definition and placement of all the memory elements, which is in general outside the possibilities of bottom-up approaches. To solve these issues, novel fabrication methods and device structures should be conceived. However, bottom-up RS memories can still allow the most highly scaled and high density testing devices, and can constitute ideal testing structures for the investigation of RS phenomena at the nanoscale.

2.2 Template assisted fabrication of oxide nanostructures

This section focuses on some of the most widely exploited bottom-up fabrication methods. A particular emphasis is given to techniques that can ensure an accurate control on the arrangement of the created structures in a periodic layout, given their technological importance.

2.2.1 Anodic alumina oxide (AAO) membranes

Among the methods to produce ordered arrays of metal, metal-oxide, and core-shell NWs or nanorods for RS applications, one of the most widely exploited in the literature is the templated-assisted deposition through anodic alumina oxide (AAO) self-assembled membranes.

AAO membranes are nanoporous hard masks with a hexagonally close packed (HCP) pores symmetry produced by a two-step anodic oxidation process of aluminum (Al) films originally developed by Masuda et al. [5]. The ordering of the pores occurs spontaneously by a self-assembly process during the AAO formation, driven by mechanical stress at the metal/oxide interface which causes repulsive forces between the neighboring pores and promotes the formation of the ordered HCP structure [6]. The template formation can be controlled by the applied voltage and the choice of the acid solution during the anodization process, resulting in AAO templates with variable pore size approximately between 15 to 300 nm, while the template thickness can be up to a few hundred μm [7].

The AAO formation is usually followed by deposition through the template pores by various physical or chemical deposition techniques in order to produce ordered arrays of nanostructures. However, because of the difficulty in depositing through pores with high aspect-ratio by PVD techniques, below diameters of ~ 50 nm electrodeposition is the preferred technique [8].

Due to their flexibility and easy manufacturing, AAO membranes were employed in several studies with the purpose of producing ordered arrays of metal NWs with a tight control over their diameter and spacing. However, AAO-based lithography suffers

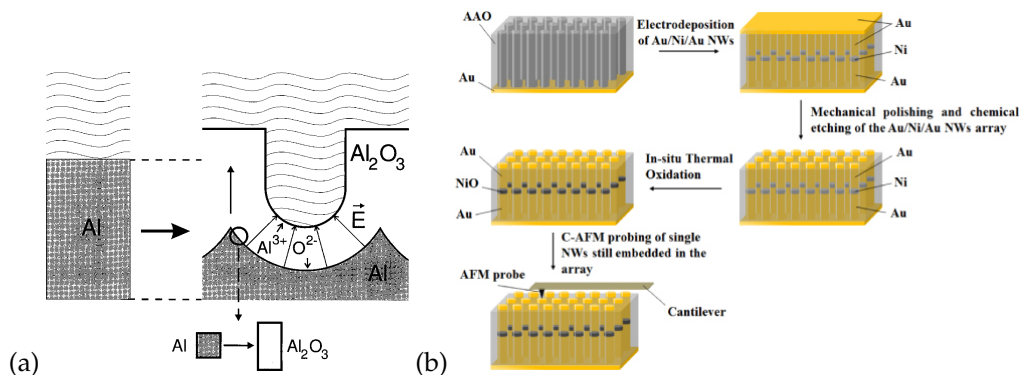


Figure 2.1: (a) AAO template formation. Reprinted from [6]. (b) Ordered arrays of NWs formed by electrodeposition through AAO template. Reprinted from [8].

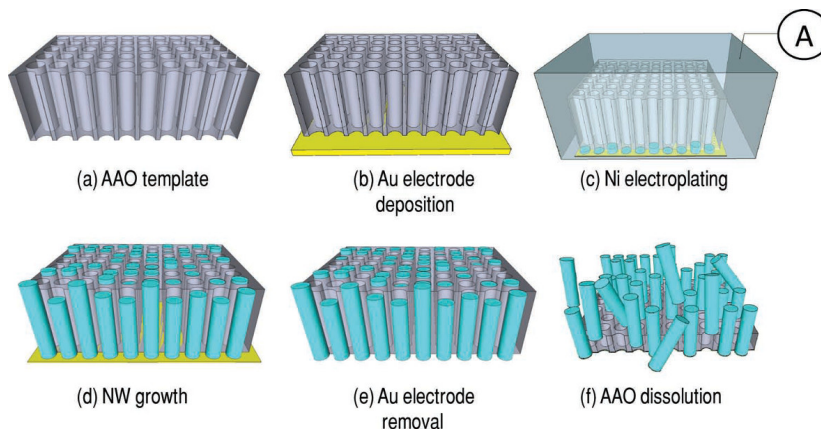


Figure 2.2: Schematic illustration of Ni NW synthesis by electrodeposition through AAO membranes, followed by AAO template dissolution, leaving free-standing Ni NWs in solution. Reprinted from [10].

from several drawbacks, as pattern registration is very hardly achievable and the AAO formation possesses poor compatibility with industrial CMOS processes.

AAO templates with variable pore size were used to define regular arrays of HfO_2 nanodots on conductive substrates by sputter deposition, forming sub-100 nm scale HfO_2 -based resistive switching devices (memory size around $2.01 \times 10^{-11} \text{ cm}^2$) [7]. Alternatively, Ni or Ni interleaved with Au or Pt was electrodeposited through high aspect-ratio AAO templates to form heterostructured NWs [9–12]. The formation of NiO or even Ni/NiO core-shell NWs was possible by a post-deposition oxidation process.

The RS behavior of multiple memory cells in parallel was examined by a direct contact of a tungsten probe [9] or by depositing a μm -size top electrode [12] over the AAO membrane containing the switching elements. Conversely, a selective contact of single NWs was achieved by conductive atomic force microscopy (C-AFM) by means of a conducting tip [7, 11]. Another possibility is to dissolve the AAO template in a basic NaOH solution and disperse the NWs over an insulating substrate, while selective contacts for

single NWs were defined by top-down lithography [9].

2.2.2 Nanosphere lithography (NSL)

NSL is a fabrication technique that allows to inexpensively produce ordered arrays of nanoparticle with tunable size in the 20–1000 nm range with HCP symmetry. NSL is inherently parallel and permits a high throughput production combined with a tight control over the particles size, shape, and spacing [13].

The first step in NSL is the self-assembly of a monolayer of monodisperse polymer nanospheres (usually made of polystyrene, PS) to form a two-dimensional colloidal crystal serving as deposition mask. PS nanospheres can be deposited from solution by diverse deposition methods. Once on the sample surface, the nanospheres freely diffuse across the substrate and rearrange in the lowest energy configuration. In order to achieve self-assembled periodic HCP patterns, on negatively charged surfaces the nanospheres surface requires a chemical modification by negatively charged functional groups. After solvent evaporation, nanospheres group together by capillary forces and reorganize in a HCP arrangement with long-range order. Various non-idealities like a finite nanosphere size distribution cause a number of defects: point defects, line defects, and polycrystalline domains.

After self-assembly, the selected material can be deposited through the nanosphere mask by various physical or chemical deposition techniques. The template mask can be afterward removed by sonication in solvent, leaving a periodic pattern of the desired material.

For research purposes, NSL allows an easy and inexpensive way of patterning large areas. However, NSL is essentially limited in the minimum resolution above 20 nm and the registration of the defined features requires pre-patterned substrates with relatively deep grooves and a proper functionalization. In any case, any additional patterning step would cancel the main benefit of NSL, which lies in the limited cost, and accurate positioning of the defined features is difficult to achieve with this method.

NSL combined with a deep Si etch process was applied for the fabrication of high density one diode–one resistor (1D–1R) nanopillar devices, without resorting to conven-

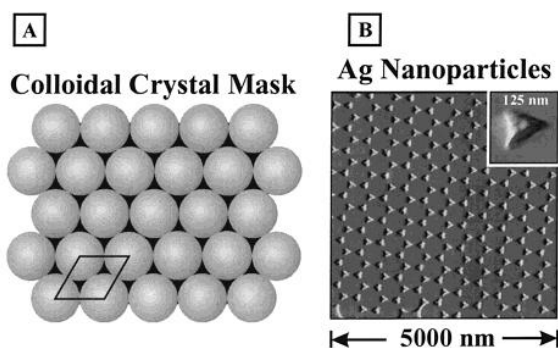


Figure 2.3: (a) Assembly of one monolayer of auto-organized colloidal nanospheres and (b) AFM image of thermally evaporated Ag metal through the colloidal mask after sonication in solvent for mask removal. Reprinted from [13].

tional photolithography. The resistive switching memory elements were based on a 60 nm SiO_x film, while the Si diode was produced from a $p^{++}/n^+/n^{++}$ epitaxial Si wafer [14]. In another paper, NSL was applied to create SiN nanorods with resistive switching properties. Variations in set and reset voltages in the nanostructured sample were highly reduced when compared to a SiN flat film [15].

2.2.3 Block copolymer templated self-assembly (TSA)

Block copolymers (BCPs) can self-assemble in periodic nanodomains when subjected to thermal treatment, owing to the immiscible monomeric units composing the distinct blocks of the macromolecule. The BCP molecules can be dissolved in a solvent and spin coated over the substrate in thin films. After thermal annealing above the glass transition temperature, the molecules rearrange in the most energetically favorable configuration, which under certain conditions leads to the formation of regular periodic domains with nanoscale dimension. The size of the nanodomains can be controlled by the length of the polymer chain (or, equivalently, by the molecular weight), while the ratio of the size of the different blocks controls the morphology of the self-assembled pattern [16]. The details about the thermodynamics of the BCP phase separation are given in chapter 4.

In di-block copolymers, which are composed of two polymer units, the equilibrium morphologies contemplate spheres with cubic symmetry, cylinders with HCP symmetry and lamellae, or layers, of one phase embedded in the other phase [17]. The segregation of the BCP blocks on the molecular scale permits the fabrication of features in the 5–100 nm range with diverse morphologies.

The implementation of BCP lithography however requires the alignment and registration of the BCP-formed patterns over the surface. This can be accomplished using pre-patterned substrates, in a combination of top-down and bottom-up technologies. This procedure is called *templated self-assembly* and can be divided in *chemoepitaxy* processes, when the BCP pattern is directed by regions of the surface with different affinity to the BCP blocks, and *graphoepitaxy*, when the BCP pattern is guided by the physical topography of the substrate [4, 18].

TSA possess high compatibility with standard CMOS technologies and when applied in combination with traditional top-down photolithography allows the pattern multiplication beyond lithographic limit and an accurate registration [19]. The patterns can be afterward transferred to the selected material by dry or wet etch process including lift-off, back-etch, and reactive ion etching. However, the limited selectivity of many all-organic BCP materials strongly limits the aspect-ratio of the defined features. The research is currently in progress on Si-containing BCP with higher selectivity, intermediate transfer to hard masks, or hardening of one of the BCP domains by selective incorporation from solution or gas phase to name a few examples [20, 21].

A detailed explanation of the possible applications of BCP lithography can be found in chapter 4. In brief, in the context of RS devices, BCP lithography was applied to nanostructure the contact area between the top electrode and the switching material in NiO-based resistive switching memory devices, improving the switching uniformity [24]. Alternatively, the RS device volume was patterned beyond the limit of conventional lithography by self-assembling a single BCP-formed pore inside a wider pre-patterned trench, thus achieving a memory lateral size below 20 nm [25]. Finally, a Si-containing BCP was self-assembled and etched by oxygen plasma to directly produce high density and periodically arranged SiO_x nanodevices without pattern transfer [26]. The resis-

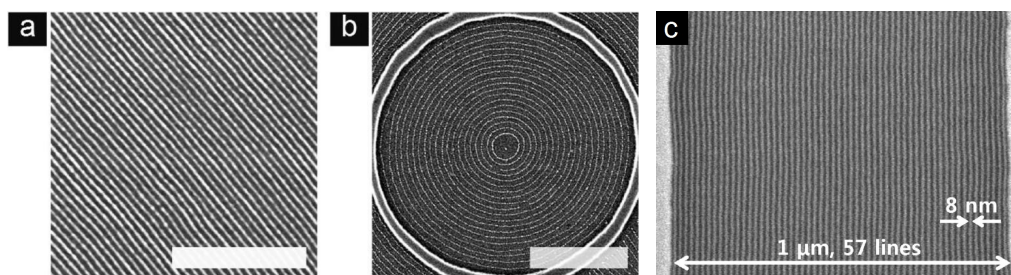


Figure 2.4: Examples of self-aligned patterns formed by block copolymer directed self-assembly. (a,b) Platinum lines from PS-*b*-P2VP block copolymer (molecular weight 34 kg mol^{-1}) in unpatterned substrate and in a circular SiO₂ topological feature (scale bars 500 nm). Reprinted from [22]. (c) Aligned tungsten NWs with 9 nm line width prepared using the 16 kg mol^{-1} PS-*b*-PDMS. Reprinted from [23].

tive switching property of the nanoscale memory elements was inspected by C-AFM as explained above.

2.2.4 Nanowire growth by bottom-up techniques

Bottom-up NWs can be grown by various methodologies, either in vapor or in solution. One key feature of these syntheses is the promotion of anisotropic crystal growth using metal nanoparticles as catalysts or driven by the substrate crystallographic orientation through epitaxial growth.

An example of NW bottom-up growth is represented by the *vapor-liquid-solid* (VLS) growth mechanism and related techniques. It can be exploited for a wide range of semiconductor or oxide NWs [27, 29]. The synthesis is initiated by a catalytic seed of Au or other metals which is alloyed in the liquid phase with the growth material. The NW growth subsequently nucleates with atoms coming from precursor in the vapor phase.

As an extension of the VLS mechanism, nanowires, nanorod, and nanobelts can be grown by solid-vapour phase processes. The source materials in powder or condensed form is thermally evaporated in a furnace, carried by an inert or oxidizing gas and then condensed on the sample surface to form the desired product. A notable example is the

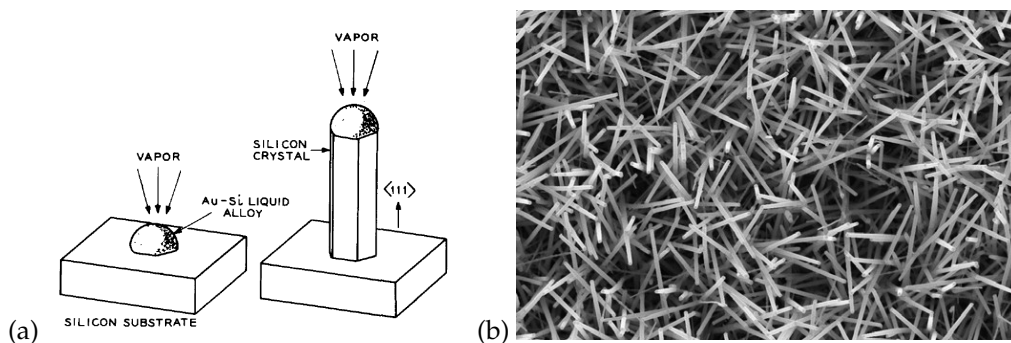


Figure 2.5: (a) schematic VLS mechanism. Reprinted from [27]. (b) ZnO nanorods grown using gold as a catalyst. Reprinted from [28].

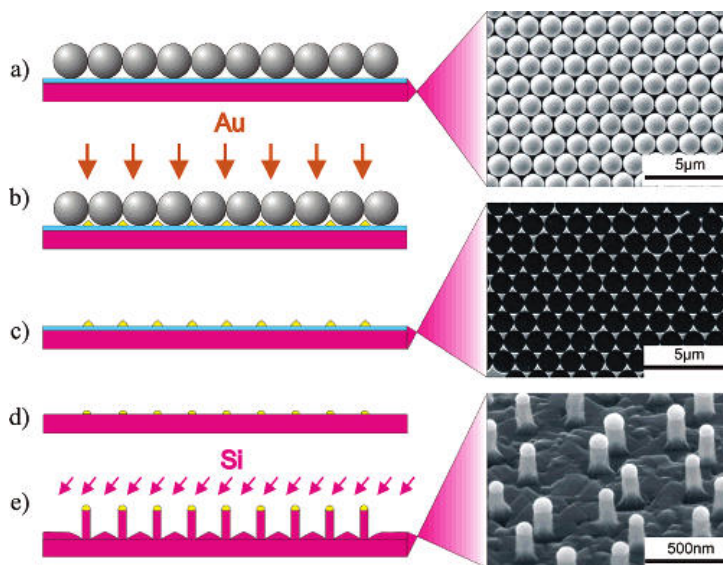


Figure 2.6: Example of fully bottom-up process for the growth of ordered arrays of NWs by VLS using periodic catalyst droplets patterned by NSL. Reprinted from [30].

fabrication of ZnO nanostructures [28].

The fabrication of bottom-up oxide NWs found interesting applications for the study of size and dimensionality-dependent chemical and physical phenomena, and the RS phenomenon makes no exception. In addition, NWs can be the driving element in the study of novel device concepts for 3D vertical RRAM integration for device scaling beyond lithography.

Nonetheless, for the integration of bottom-up NWs into functional systems, the NWs formation needs to be driven toward ordered arrays. A viable option is patterning the droplets of metal catalyst into ordered arrays prior to the VLS growth. To give an example of a fully bottom-up process, gold droplets were deposited through a mask formed by PS spheres in a procedure similar to NSL [30]. This method allowed a controlled and uniform assembly of bottom-up NWs with predefined symmetry, while the sharp size distribution of the gold droplets resulted in NWs with uniform diameter.

An alternative solution can be the controlled assembly after deposition. In a work by Whang et al., NWs were transferred to the surface after growth and simultaneously aligned exploiting the Langmuir-Blodgett technique to make a parallel array with uniform spacing. In this way, even crossbar or more complex array structures can be produced by repeating the process with different NWs orientation in the different layers [31]. An alternative alignment method is based on contact printing of a donor substrate containing a high density array of NWs over a receiver substrate with pre-patterned sliding steps to align the transferred NWs [32].

The exact positioning, alignment and distribution of NWs strongly depends on the procedure adopted. The NWs placement by organized seed catalyst arrays requires a high resolution technique, since minimum patterned feature should be at least comparable to the NW diameter, adding complexity to the process. While post-growth alignment methodologies seem promising, the registration accuracy and a viable application

of these techniques for device manufacturing are yet to be demonstrated.

For RS device patterning, bottom-up ZnO NWs were grown by a solid–vapour phase process catalytically activated by gold droplets and then transferred by drop-casting onto a SiO₂/Si substrate. For the determination of the ZnO NW RS properties, Ti electrodes were defined by top-down e-beam lithography [33]. A similar experiment was conducted on single crystalline ZnO NWs [34]. In this latter case, one of the electrode was composed of copper, which was found to easily diffuse along the NW surface and form Cu island, thus realizing a CB–RAM.

2.2.5 Synergistic combination of top-down and bottom-up approaches

Many of the aforementioned bottom-up techniques require combined top-down and bottom-up approaches in order to achieve a selective positioning of the defined features. Notable examples are NSL, TSA, and catalytically-activated NW growth. Without a proper external driving force or boundary condition imposed by top-down techniques, the self-organized templates are randomly aligned, while the nucleation of nanostructures proceeds with randomness during growth. Nevertheless, the integration of bottom-up techniques still can give some advantages in terms of process simplification and cost reduction. As in the case of block copolymers, very high patterning densities can be achieved avoiding complicated lithographic tools. As another example, bottom-up growths can allow *in situ* doping by selective incorporation of dopant atoms. This could avoid destructive techniques such as ion implantation and improve device properties [2]. In the ITRS roadmap [19] the synergistic combination of both approaches is forecast as one of the most promising solutions for sub-10 nm lithography. self-assembled nanostructures allow to reduce patterning cost and complexities, still permitting outstanding density, novel architectures and new functional materials.

Other techniques try to combine top-down with bottom-up. Crystal lattice is a beautiful example of self-assembly driven by inter-atomic interaction. Lee et al. reported the use of projections of the atomic lattice of a Si crystal in a TEM machine. Atomic resolution images of the Si crystal lattice were magnified and projected onto Hydrogen silsesquioxane (HSQ) films, creating arrays of periodic nanostructures. This technique can be further extended in combination with electron beam lithography (EBL) to increase the patterning throughput when periodic arrays of simple and structures are required [35].

2.3 Resistive switching in oxide nanostructures

Once that oxide nanostructures are formed, their RS properties should be analyzed by building M–I–M devices and contacting the two electrodes to an external Current–Voltage source. Various architectures were exploited in the literature, depending on the nanostructure assembly method and ease of device fabrication. For simplicity, the analysis can be divided into RS in multiple nanostructures or at the single nanostructure level. An additional point of interest can be found in metal/oxide core–shell NWs. In these systems, an internal metal core acts as the conducting electrode, while an external oxide shell possesses the resistive switching property, making them ideally suited for high density crossbar arrays.

Since most of the nanostructured RS devices reported in the literature concern NWs

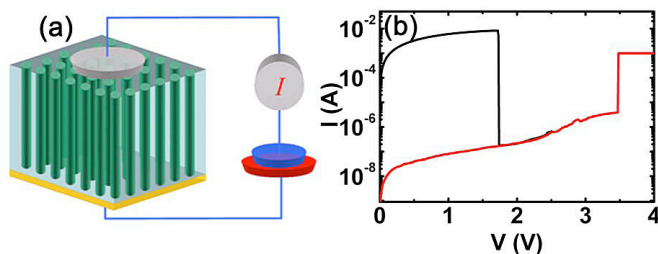


Figure 2.7: (a) Schematic of the measurement setup for an array of vertically aligned NWs in parallel. (b) I–V curves for an array of 13 μm long NiO NWs. Reprinted from [9].

and oxide materials constitute the prototypical switching medium, the following description will be limited to oxide or metal/oxide NWs.

2.3.1 Resistive switching in multiple nanostructures

When NWs or nanorods are aligned perpendicular to the substrate such as when the material is deposited through AAO membranes, a simple method to measure RS properties is to contact many nanostructures at a time. This can be accomplished by defining a top electrode or by placing a micrometric tungsten probe directly in contact with the produced vertical array. The reason to proceed with these experiments is that the nanostructured switching material can have a different switching behavior when compared to continuous films.

Kim et al. contacted an array of hundreds of oxidated Ni NWs in parallel by direct contact of a tungsten probe with a diameter of about 50 μm . The NWs were defined by AAO membranes and had a length of alternatively 13 or 25 μm and a diameter of 70 nm after oxidation. An Au film was deposited at the bottom of the AAO template prior to Ni electrodeposition to serve as bottom electrode. While an electroforming step was necessary to initiate the switching operations, interestingly it occurred at much lower electric fields than in continuous NiO thin films. Additionally, reproducible resistive switching was observed below 20 V even for the 25 μm -long NiO NWs, in contrast with what is in generally found with NiO films with thickness in the μm range.

For the investigation of the switching properties of a single NW, the AAO template was dissolved and selected NWs were contacted with an inter-electrode distance between 1 μm and 25 μm . As in NiO films, unipolar resistive switching was observed for both individual and vertically aligned NiO NWs [9]. A detailed discussion of the RS phenomenon in a single NW will be the subject of the next session.

The idea was further expanded in a work by Huang et al. A reliable multilevel resistive switching was obtained in a NW array formed by multiple NiO and Pt layers in the AAO template. The layered structure allowed to reach a resistance ratio (HRS/LRS) as high as 10^5 , a narrow distribution of switching voltages, and multilevel states by both unipolar and bipolar operations. The RS cells were tested by steady state voltammetry and train pulses, achieving multiple and reproducible stable states either by increasing and decreasing the applied potential. This original behavior was explained by a simple multiple resistor model considering many NWs in parallel and multiple switching layers in series in each NW [12].

Using NSL lithography, Ji et al. constructed an array of Si-based pillar structures

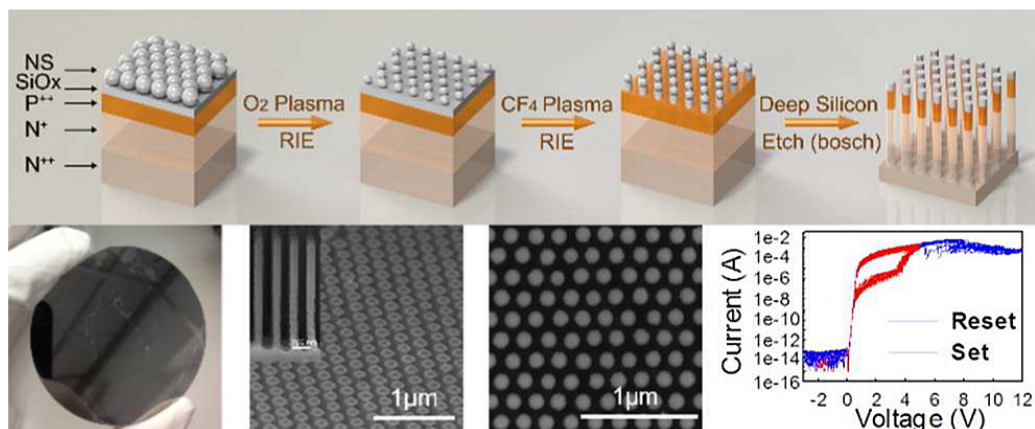


Figure 2.8: One diode – one resistor fabrication procedure using NSL self-assembled template and deep ion etching of the SiO_x memory elements and of the underlying $\text{p}^{++}/\text{n}^+/\text{n}^{++}$ Si wafer. Reprinted from [14].

containing a $\text{p}^{++}/\text{n}^+/\text{n}^{++}$ diode in series with a SiO_x RS device. As bottom electrode, the n^{++} Si substrate was used, while a tungsten probe tip (10 μm radius) was used as a top electrode, testing as many as ~ 7800 nanoscale devices in parallel. Excellent resistive switching characteristics and reliability were observed, with AC pulsed switching speed in the 50 ns regime and multibit operation [14].

A different approach was adopted by Bellew et al. A random network of NWs was interposed between two electrodes defined with top-down e-beam lithography. Each Ni wire was coated by a self-limiting NiO layer of 4 – 8 nm in thickness. The mesh of NWs contained a number of reversible switching junctions, realizing a random percolative network. In the work, Bellew and co-workers were able to demonstrate that such networks exhibit properties that not only evolve and adapt in response to electrical stimuli leading to controlled levels of connectivity and conductivity, but that the incorporation of RS elements introduces a level of programmability not available in conventional materials. The ability to reconfigure the distribution of ON and OFF junctions inside the network led to fault-tolerant and adaptive behaviours [36].

2.3.2 Resistive switching in a single nanostructure

In order to test the memory properties of nanoscale devices fabricated by bottom-up approach, a single memory element should be contacted at a time. Unless innovative integration schemes are conceived which include both bottom-up devices and contact lines, the task of contacting nanoscale devices could be extremely demanding in terms of lithography resolution and fabrication process. Indeed, high density 3D memory architectures are supposed to integrate vertically aligned NW arrays. However, the fabrication of *e.g.* a horizontal NW memory is a much less complex procedure. For the purpose of analyzing the switching properties of single devices, bottom-up fabricated NWs are commonly dispersed on an insulating substrate, usually SiO_2/Si , and then two or more contact electrodes are defined on selected NWs by top-down lithography techniques such as e-beam or conventional photolithography.

In a work by Nagashima et al., MgO/CoO core-shell NWs were grown by VLS

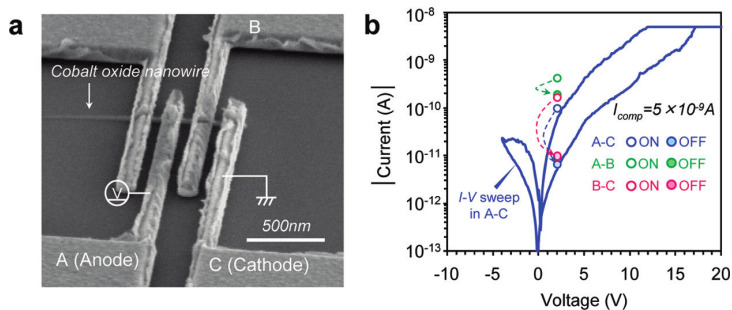


Figure 2.9: (a) SEM image of a single CoO Nw device contacted with a multielectrode configuration for the investigation of the switching location (gap spacing between electrodes is ~ 100 nm. electrode C was grounded for RS operations. (b) I-V characteristics obtained in the multiprobe NW devices. Reprinted from [37].

method, sonicated and dispersed in isopropanol, and then transferred to an insulating SiO_2 substrate. Nanoscale Pt electrodes were afterward defined by e-beam lithography on single NWs in various two electrode or multi gate configurations. Due to limitations of the planar top-down lithography, the gap spacing between the two electrodes defined a memory cell with an approximate size of 250 nm, in contrast with thin film-based RS memories in which the distance between the electrodes is usually limited to the deca-nm range or less. This implies switching voltages greater than 10 V, while the compliance current was set to 10^{-9} A. After an initial electroforming step, the CoO NWs exhibited bipolar RS characteristics and endurance up to 10^8 cycles, while the retention was found to depend on the gaseous ambient during switching.

The lateral switching configuration turns out useful for the investigation of the switching mechanism. First, it allows a uniform exposure of the switching medium to the environment. The insertion of an oxidizing gas in the chamber allowed to stabilize the NW cell retention, highlighting the importance of redox events in the bipolar RS of the CoO NWs. In addition, the planar configuration makes possible multi-probe measurements. Using three electrodes, the authors were able to identify that the RS region in CoO NWs is close to the cathode electrode [37].

Similar studies on ZnO NWs formed by various catalytically-activated bottom-up processes evidenced stable bipolar and unipolar RS characteristics. Single crystalline ZnO NWs with Cu and Pd/Au contact electrodes demonstrated large ON/OFF ratio $>10^5$, a long retention time $>2 \times 10^6$ s, and low threshold voltages <3 V. The switching mechanism was confirmed by electron dispersive X-ray spectroscopy to be related to the formation/annihilation of filaments of Cu island chains along the NW surface [34]. Similarly grown ZnO NWs contacted by lithographically defined Ti electrodes also demonstrated an ON/OFF ratio $>7 \times 10^5$. In this latter case, a TiO_x interlayer was found to form at the ZnO/Ti interface due to O atoms out-diffusing into the Ti electrode, while O vacancies are left in the region of the ZnO. The good RS performances were found to be related to the generation of this oxygen-depleted region [33].

RS in single ZnO NWs contacted by Ti electrodes were also investigated in a work by Lai et al. In this case, an argon plasma treatment procedure was applied to modify the defect density. The result was a general performance improvement and a multi-state capability. In addition, a marked reduction of the programming voltages was found after plasma treatment due to decrease of the barrier thickness at the Ti/ZnO interface:

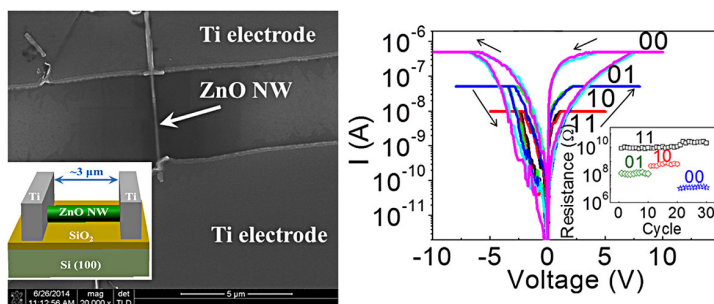


Figure 2.10: Single ZnO NW contacted by two Ti electrodes and relative multi-state switching operations after treating the sample in Ar plasma. Reprinted from [38].

switching voltages below 5 V were obtained even for an electrode spacing of 3 μm [38].

Studies on the RS phenomenon were also conducted on CuO_x NWs synthesized by a low-cost and large-scale electrochemical process which exploited electrodeposition through AAO nanotemplates followed by thermal oxidation. Instead of contacting multiple NWs, the AAO membrane was dissolved in a basic solution and a single NW was contacted. The Ni/ CuO_x /NW memory devices exhibited forming-free switching property and both unipolar and bipolar operations could be achieved. Even if the distance between the electrodes was about 2 μm , operations at low bias voltage around 1 V were obtained. This was explained by a significant amount of defects and the presence of Cu nanocrystals in the CuO_x NWs [39].

An alternative methodology for the selective investigation of single NWs is by using C-AFM, using a conductive tip as one of the contacting electrodes. The main advantage of this technique is that an advanced lithography fabrication method can be avoided. Moreover, high density arrays can be easily addressed as long as the sharp tip is able to distinguish among the different structures. The typical curvature radius of a conductive tip is between 10 nm and 30 nm, allowing structures as small as a few nm to be easily distinguished.

Brivio et al. analyzed regular arrays of heterostructured Au/NiO/Au NWs formed by electrodeposition followed by oxidation in AAO templates. Without the need to dissolve the template, by C-AFM it was possible to selectively contact the apex of individual NWs 50 nm in diameter. Switching operations in the high density array could be achieved without disturbing the surrounding NWs, with a switching power as low as 1.3 nW, which stands nearly an order of magnitude lower than previous analysis of NiO-based memories. However, in order to exploit the geometrical downscaling for power reduction, it was essential to limit the forming current in the deca-nA regime [40]. Interestingly, changing the NW structure from the symmetric Au/NiO/Au to the asymmetric Au/NiO_x/Ni/Au, the switching behavior changed from unipolar to bipolar [11].

Beyond NiO, a similar nanofabrication procedure based on AAO membranes followed by C-AFM analysis was employed by Lyu et al. on Au/HfO₂/Pt memory cells [7].

An alternative approach was reported by Oka et al. In their work, the measurement structure was fabricated by transferring the synthesized NWs onto a SiO₂ substrate, and a Pt electrode with a sharp edge was defined on one side of the NW. The C-AFM tip was then positioned about 1 μm apart to be used as second electrode. With this method,

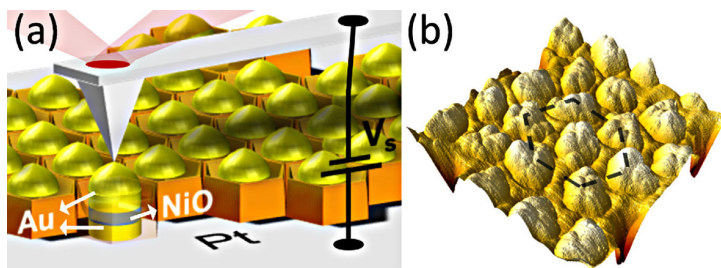


Figure 2.11: Schematic of the experimental set-up used to probe individual NWs by C-AFM. Reprinted from [40].

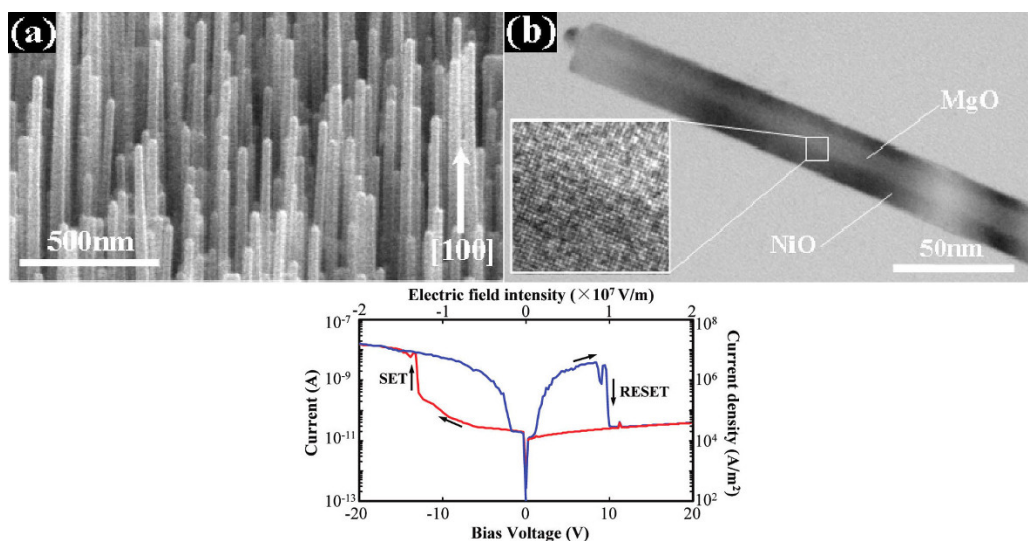


Figure 2.12: SEM image of NiO heterostructured NWs with single crystalline MgO core and NiO shell and relative I-V characteristics acquired using C-AFM. Reprinted from [41].

nonvolatile bipolar resistive memory switching was demonstrated in Single crystalline NiO heterostructured NWs.

Bipolar RS was also observed in heterostructured NWs composed of an epitaxial NiO shell (10 nm thickness) deposited by laser ablation from a NiO pellet target on top of MgO NWs (10 nm diameter) grown on crystalline a MgO substrate by the metal catalyst-mediated VLS mechanism. The bipolar type of RS found in the heterostructures NWs essentially differed from the unipolar typical of polycrystalline NiO thin films [41].

Finally, Park et al. observed unipolar switching in SiO_x nanodots with either Pt or graphene as bottom electrode and the C-AFM tip as top electrode. The isolated nanostructures were directly created on the selected electrodes by oxidation of a self-assembled PS-*b*-PDMS block copolymer film, without the need of a high-cost lithography and also avoiding a pattern transfer process. In a oxidizing dry etch process, the Si-containing PDMS polymer was transformed into SiO_x , while the all-organic PS was selectively etched away. This left a regular array of nanoscale SiO_x dots with HCP symmetry and defined dimension.

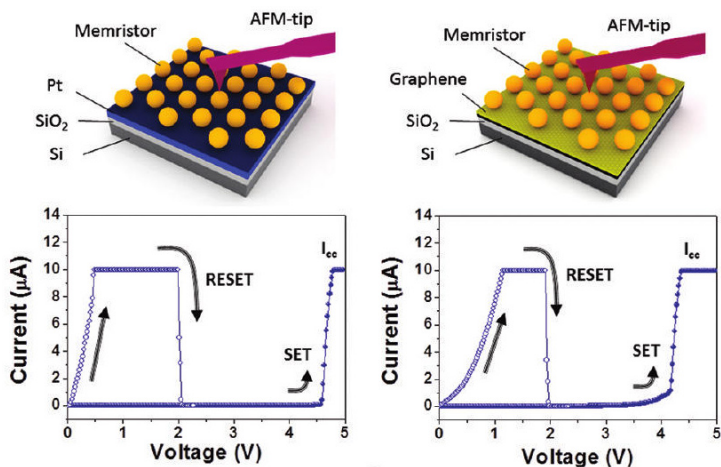


Figure 2.13: I–V measurements acquired with a direct contact of a conductive Pt C–AFM tip on top of a SiO_x nanodot array. As bottom electrode, a Pt film or a graphene sheet were alternatively applied. The regular array of SiO_x nanodots was fabricated by oxidation of a self-assembled PS-*b*-PDMS block copolymer film. Reprinted from [26].

2.3.3 Resistive switching in core–shell nanowires

In core–shell NWs composed of an internal conductive line covered by an insulating shell, the core part can serve as contact line, while the RS occurs radially in the shell at the intersection between two NWs. Core–shell NWs could be flexible building blocks with inherent high scalability for crossbar array structures, opening up the opportunity to explore non only the detailed nanoscale mechanism of RS operation, but also next-generation nanoscale nonvolatile memory devices with the potential for very high density integration and improved memory characteristics [42]. However, alternative contact fabrication methods must be envisaged if all the NWs in a high density crossbar array are to be individually addressed for external connection. Moreover, the existence of sneak paths, which is the preminent complication in large crossbar arrays, still needs to be solved.

The previously discussed and largely employed fabrication method based on AAO membranes can also originate core–shell NWs. Cagli et al. electrodeposited Ni through an AAO template with 10 μm thickness and self-ordered HCP pores of with a diameter of 200 nm, resulting in NWs with a length of 30 – 40 μm . Next, the AAO template was dissolved and the NWs were transferred in a pure ethanol suspension to prevent oxidation. To assemble a crossbar structures, a two-step alignment technique was developed. A first NW layer was deposited on a SiO_2 substrate from the liquid suspension and aligned using a magnetic field. Then, the same deposition and alignment procedure was executed for the top NW layer in a perpendicular direction. Resistance switching in RRAM devices based on core–shell Ni–NiO crossbar structures was demonstrated, and switching was unequivocally shown to take place at the NW–NW crosspoint junction [10].

A similar AAO-based procedure was adopted by He et al. Ni/NiO core–shell NWs with an average diameter of 75 nm and an amorphous NiO layer with a thickness of 4.5 nm were produced. In this case, the NWs dispersed on the SiO_2 substrate were first

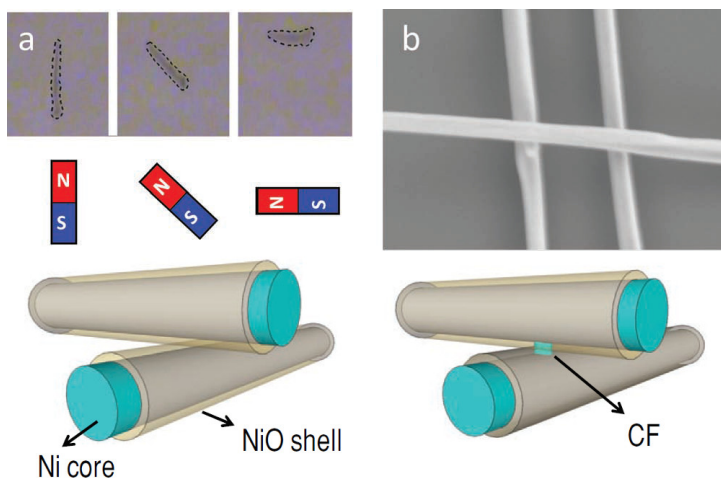


Figure 2.14: Alignment procedure using a magnetic field. Two perpendicular layers of core–shell NWs can be aligned, forming a crossbar array in which the NWs core act as carrier transport, while the RS occurs radially along the NWs shell. Reprinted from [10].

contacted by a perpendicular Au strip defined by e-beam lithography, then a controlled oxidation process was carried out to build the oxide shell. Another Au electrode was afterward defined in contact with the NiO shell [43].

An interesting and original fabrication method was proposed by Christesen et al. for the arbitrary creation of various high resolution morphologies along the NW axis. Starting from Si NWs grown by VLS mechanism, the silane (SiH_4) gaseous precursor was combined with modulated phosphine (PH_3) pulses in order to selectively encode varying levels of P substitutional doping atoms along the growth axis. Christesen and co-workers exploited the variable etch rate of Si NWs in KOH solution as a function of phosphorus doping to create various step-like, hourglass, and tapered features as small as 10 nm. An interesting application of the proposed fabrication method is the creation of a suspended constriction with a diameter of ~ 30 nm in a NW with a diameter of ~ 50 nm, highly confining the electric field within the narrow channel region. After thermal oxidation, a ~ 10 nm diameter Si core was embedded in a SiO_2 shell. As last step, two electrical contacts were fabricated on the segments adjacent to the intrinsic channel. An electroforming step was required to initiate the RS behavior, and the unipolar switching expected from Si/ SiO_2 systems was observed [44].

Finally, a similar concept to core–shell NW structures was exploited by Shim et al. for the development of programmable logic arrays (PLA). In this case, a semiconducting Si/Ge NW was deposited on the insulating SiO_2 film and covered by a top gate, followed by layers of dielectric (ZnO_2) and metal (Cr/Au) deposited sequentially on the NW. Additional layers of resistive switching material (SiO_2 , 30 nm) and metal (Cr/Au) were then deposited sequentially on top of the conventional gate to yield the M–I–M sandwich structure characteristic of RS devices. The incorporation in the same device of a RS structure combined with a dielectric gate on top of the semiconductor NW yields programmable active/inactive transistor nodes, in which the working principle is based on a variation of the capacitive coupling between the gate and the semiconducting NW. A prototype demultiplexer with non volatile property was fabricated to test the device

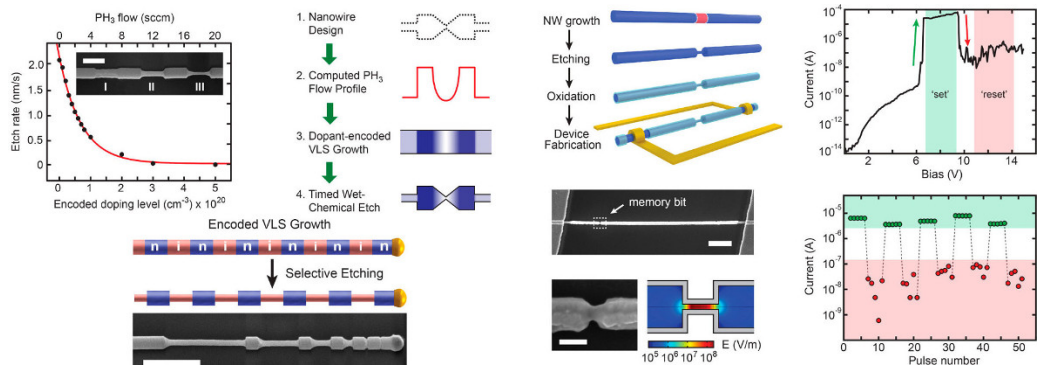


Figure 2.15: Differential etching technique used to pattern VLS-grown Si NWs. Etch rate depends exponentially on the P doping level and can be exploited to pattern various morphologies. On the right, a constriction is defined in an oxidated Si NW to define a nonvolatile resistive memory with switching occurring at the junction point. Reprinted from [44].

operation. The conceived structure can be further integrated into crossbar arrays for functional logic circuits, thus providing a new approach for fabricating high density PLAs [45].

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HfO₂-based resistive switching devices

3.1 Introduction

This chapter focuses on the experimental characterization of resistive switching devices based on HfO₂ thin films. HfO₂ was selected as switching material due to its promising switching performance and easy integration in standard electronic fabrication processes. Atomic layer deposition (ALD) technique was applied for oxide deposition. ALD allows to deposit high quality films with accurate control over the deposited thickness. A deposition procedure was developed to produce both plain HfO₂ films and HfO₂ doped with an uniform concentration of Al atoms across the film thickness. Oxide doping with Al atoms was proposed as a viable route to engineer the final device switching properties and to reduce switching variability. For this purpose, a set of samples with 4% and 7% Al concentrations was fabricated in order to test the device properties as a function of doping concentration.

The HfO₂/TiN stack was first analyzed by X-ray photoemission spectroscopy (XPS) to determine the actual structure and composition. In particular, a TiO_xN_y layer of 2 – 3 nm was found to form at the interface due to TiN oxidation, while the as deposited HfO₂ layer was found to be almost stoichiometric even in thin films of 3 nm and in the Al-doped films.

μ-size devices were fabricated by top electrode lithographic patterning in order to test the influence of material properties on the device switching behavior. The switching properties and retention characteristics were inspected as a function of Al concentration in the oxide film. A moderate Al concentration was found to produce a general improvement in variability while avoiding an excessive deterioration of the retention performance. Interestingly, a coexistence of various switching modes in the same device was related to the highly defective oxide interlayer found by XPS analysis at the HfO₂/TiN interface.

Finally, random telegraph noise (RTN) analysis was identified as a possible tool to investigate the electron trapping properties in HfO₂ devices on varying of the resistance state. A correlation was also identified between the trend of the noise power density and the Al doping concentration in the film.

3.2 Deposition and characterization of the materials

The electrode material is a fundamental part of resistive switching memories and has a profound influence on the device physics and switching mechanism. A detailed discussion about the role of the metal electrodes can be found in chapter 1. As common

bottom conducting material, a TiN film was first deposited on the Si wafer by sputter deposition. On top of it, HfO₂ and Al:HfO₂ films were deposited by ALD. A review of previous *ab initio* simulations and experimental works on the effect of impurity atoms in the oxide switching layer can also be found in chapter 1. The introduction of Al atoms was identified as one of the best choices for reduction of the switching variability. However, the effect of varying the Al concentration in the film was not discussed in detail. In this work, samples with two different Al concentrations were produced.

Bottom electrode A TiN/Ti film was deposited by RF sputter deposition on top of a Si wafer with native oxide. The deposition was carried out in a Kurt J. Lesker PVD75 machine equipped with four different 4.2" TORUS magnetron sources in confocal configuration. The available gases were Ar and N₂. Ar was used for plasma ignition, while N₂ was applied in conjunction with Ar for gas phase reaction during deposition. 10 nm Ti was first deposited as adhesion layer at room temperature with 100 W RF power and 40 sccm Ar flow. Then, 40 nm TiN was deposited at room temperature with 100 W RF power in a mixed Ar/N₂ environment with 40 sccm Ar/4 sccm N₂ flow. The calibrated deposition rate was 1 nm/min for both depositions. The base pressure before the deposition was at least 1×10^{-7} mbar, while during deposition the pressure was about 3×10^{-3} mbar.

The TiN film is composed of columnar crystalline grains extending throughout the thickness. This aspect can be evidenced by scanning electron microscopy (SEM) cross section analysis, as reported in detail in chapter 5. The presence of grains with an average grain size of 17.4 ± 0.7 nm was also visualized by atomic force microscopy (AFM) analysis. The columnar grains morphology is typical of TiN films grown by different techniques, both physical (as in the present case) and chemical depositions [1]. The vertical grain boundaries were found to act as fast diffusion paths for oxygen species, enhancing the oxidation of TiN surface [2, 3].

Oxide material ALD offers interesting properties in terms of uniformity, quality of the deposited film, and conformality to the surface features. These properties descend directly from the gas-surface limited reactions implied in the ALD process. Because of the high conformality of the ALD growth, the deposited film can readily follow the TiN surface roughness and a uniform film thickness is expected throughout the sample.

The cycling nature of ALD allows to alternate multiple ALD processes for the deposition of material compounds. In this work, alumina and hafnia cycles were alternated in order to produce samples containing HfO₂ and HfO₂ doped with Al atoms. The ratio between the HfO₂ and Al₂O₃ cycles was kept constant during the whole deposition, resulting in a uniform Al incorporation along the film thickness. The variation of the ratio between the two cycles in successive growths allowed to tailor the Al concentration.

The oxide growths were carried out by thermal ALD at 300 °C in a flow type hot wall Savannah 200 reactor from Cambridge Nanotech Inc. featuring an 8" deposition chamber with an inlet gas injection at one side and an exhaust outlet at the opposite side. The precursors applied as aluminum and hafnium source were respectively Trimethylaluminum (Al(CH₃)₃) (TMA) and hafnium cyclopentadienyl compound MeCp₂HfMe(OMe), denoted as HfD-04, from Sigma Aldrich. An H₂O source was used as oxygen source to complete the oxide growth cycle. TMA and water were kept at room temperature, while

HfD-04 was kept at 110 °C to ensure enough vapor pressure. The precursors were driven in the deposition chamber (0.8 mbar base pressure) by N₂ carrier gas, and a N₂ gas flow of 20 sccm was used during the purging steps [4]. The target thickness was set to 5.5 nm, while thinner films of 3 nm were also grown for an investigation of the Al:HfO₂/TiN interface by XPS. The actual thickness was measured by spectroscopy ellipsometry (SE) and X-ray reflectometry (XRR).

The ratio between the Al₂O₃ and the HfO₂ cycles was settled to 1:12 and 1:6, resulting in Al concentrations of respectively (4.0 ± 0.5 %) and (7 ± 1 %) as estimated by XPS analysis. It is worth noting that due to the high Al concentrations achieved, the compound obtained is sometimes referred as Al solid solution in HfO₂, rather than Al doping of HfO₂. The combination of HfO₂ and Al₂O₃ cycles used for the ALD deposition of the Al:HfO₂ films is represented in the schematic of Figure 3.1.

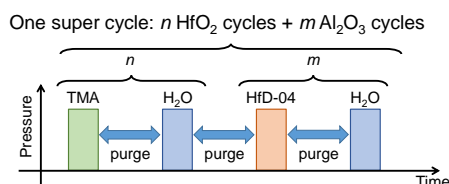


Figure 3.1: Schematic of the “super cycle” alternating the ALD cycles optimized for the growth of binary HfO₂ and Al₂O₃ oxides.

The deposited films were investigated by X-ray diffraction (XRD) analysis. As-deposited HfO₂ thin films of 5.5 nm reveal a mostly amorphous composition. Indeed, no clear peak is visible in the region of the spectrum corresponding to crystalline HfO₂, but a broad and shallow bump can indicate the presence of small crystallites. This is probably due to the low deposition temperature and low oxide thickness, while an annealing step at 500 °C for 1 min is sufficient to obtain a polycrystalline material. Conversely, Al-containing films are completely amorphous and an annealing at high temperature is necessary to induce the crystallization. The crystallization temperature however depends on Al concentration and film thickness. Al-containing films are completely amorphous since Al atoms suppress the formation of the monoclinic phase and a higher temperature is required to stabilize cubic and tetragonal phases.

It is worth to notice that all device analysis were performed using as-deposited films without a further annealing step. For this reason, all devices are expected to contain amorphous films and a consistent comparison can be performed between un-doped and Al-doped samples.

3.2.1 XPS characterization of the oxide film and of its interfaces

The chemical composition of the elements inside the inspected material, together with information about the bonding state of the chemical species and of their relative amounts can be extracted by XPS analysis. Due to the limited escape depth of the photoemitted electrons, the XPS analysis has a sampling depth reduced to a few nm below the surface. However, the sampling depth can be varied by adjusting the angle between the sample and the detector apparatus, also called take-off angle. Close to normal take-off angle values give the maximum depth sensitivity, while small take-off angles give information

from the superficial region.

XPS measurements were performed with a PHI 5600 ESCA system equipped with an Al K_{α} (1486.6 eV) radiation source followed by a monochromator to further decrease the line width and increase the energy resolution. The system is equipped with a hemispherical electron energy analyzer and objective lenses with an acceptance angle of 8° . The energy resolution depends on the choice of the pass energy and on the intrinsic line width of the photon source. The stage is provided with x, y and z manipulators to adjust the position of the sample and with an additional rotation degree of freedom for the selection of the take-off angle.

For broad energy spectrum surveys, electron energy was collected with a pass energy of 20 eV, resulting in an energy resolution around 0.6 eV. For the high resolution analysis of single regions of the energy spectrum, a pass energy of 11.75 eV was used, reaching an instrument energy resolution better than 0.1 eV. Measurements were calibrated based on the Ag $3d_{5/2}$ high resolution spectrum of a silver plate. All spectra were acquired at three different take-off angles: 45° , 55° , 75° , and 80° to check for depth variation of the sample chemistry.

A set of samples consisting of HfO_2/TiN and Al-doped HfO_2/TiN thin films was built in order to study the chemistry of the HfO_2 film and of the oxide interface with the bottom TiN electrode. In addition, a sample containing only the TiN bottom electrode was inspected to investigate the effect of the TiN exposure to air upon unloading from the sputtering chamber before the insertion in the ALD reactor. All the analyzed samples are summarized in Table 3.1. It should be noted that the oxide thicknesses measured by spectroscopic ellipsometry (SE) are referred to reference samples grown on native silicon oxide substrate. A different position in the ALD chamber and the different substrate can result in a slightly different thickness with respect to samples with TiN substrate. Conversely, XRR data was acquired on the actual samples measured by XPS. A large interface roughness of about 3 nm was detected in all samples by XRR data fitting, and it reflects in a certain degree of uncertainty on the oxide layer thickness estimation since no clear TiN/ HfO_2 boundary is identified. The effective roughness is large also in comparison with the physical roughness of about 1.5 nm measured by AFM topography on TiN and HfO_2/TiN films and is related to a density variation at the interface likely associated with TiN oxidation, as will be explained later in this section based on XPS analysis. This roughness is however similar in both Al-doped and un-doped samples and XPS data also indicates a similar chemistry in both cases, as will be shown in this section. In conclusion, the fact that a higher deviation between SE and XRR measurements is found for Al-doped samples does not seem to reflect in any chemical difference and should probably assigned to the measurement procedure.

Oxide film As reported in Table 3.1, two samples with an oxide thickness around 5.5 nm and comparable to the one used in the resistive switching memory devices were produced for the analysis of the oxide film. Sample SAV646 contains an HfO_2 film, while the oxide film of sample SAV656 was grown by alternating 1 cycle of alumina every 6 cycles of hafnia. In this way, a solid solution of Al inside the HfO_2 matrix can be achieved, also called oxide doping. The difference between the two samples can be identified in the Al 2s region of the spectrum survey reported in Figure 3.2, in which a detectable peak coming from the Al can be observed only in the Al: HfO_2 sample.

The high resolution Hf 4f spectrum of the HfO_2 film is reported in Figure 3.3(a). The

Table 3.1: Details of the samples analyzed by XPS. Thicknesses are reported based on fitting of both spectroscopic ellipsometry (SE) and X-ray reflectivity (XRR) data. The XRR roughness reported is also extracted from fitting of the XRR data. XRR data by courtesy of Claudia Wiemer (CNR-IMM).

Sample	Oxide	Oxide thickness (SE)*	Oxide thickness (XRR)	Interface roughness (XRR)
SAV646	HfO ₂	5.3 nm	5.5 nm	2.6 nm
SAV647	HfO ₂	2.6 nm	3.1 nm	3.1 nm
SAV656	Al:HfO ₂ (1:6)	5.9 nm	6.7 nm	2.7 nm
SAV655	Al:HfO ₂ (1:6)	2.8 nm	4.0 nm	3.0 nm
TiN22	Bottom electrode (40 nm TiN/10 nm Ti) after exposure to air, without any oxide on top			

*SE measurements were acquired on a reference sample with native silicon oxide substrate.

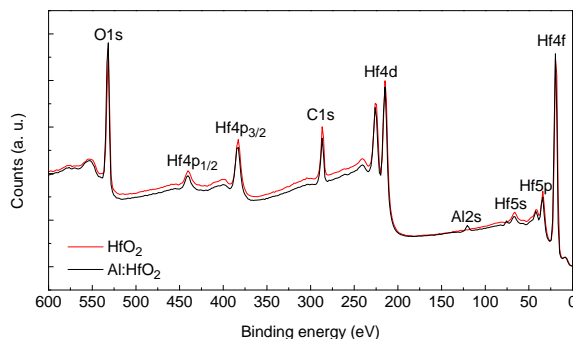


Figure 3.2: Spectrum survey of the two thick HfO₂ and Al:HfO₂ samples acquired with a take-off angle of 45°.

spectrum reports the typical double-peak feature due to the 4f_{7/2} and 4f_{5/2} spin-orbit splitting, and can be fitted by a double Voigt function (Lorentzian convoluted with a Gaussian peak) to extract peak position and width. The Hf 4f_{7/2} and 4f_{5/2} peaks are located respectively at 17.6 eV and 19.3 eV, with a peak width of 1.28 eV. These values are in agreement with a chemical bonding between the hafnium and the oxygen atoms as reported in previous analysis on stoichiometric HfO₂ film [5–7], with no detectable contributions from Hf–N bonds or metallic Hf, while the small width of the peaks points toward a single bonding state. In summary, we can exclude the presence of substoichiometric HfO_x components within the oxide film.

For poorly conducting oxide films, a noticeable charging can occur starting from as low as 3.5 nm [7], which would lead to a rigid shift of the whole energy spectrum and a wrong estimation of the binding energy. However, also considering the distance between the Hf 4f and the O 1s main peak (located at 530.8 eV, reported in Figure 3.3(b)), we found an agreement with previous analysis [6, 7].

The deconvolution of the O 1s spectrum of Figure 3.3(b) by two Voigt peaks further reveals the presence of a shoulder at higher binding energy contributing to 17% of the total integrated peak area. While the O 1s main peak can be ascribed to the Hf–O bonding and is in general described as *lattice oxygen*, the shoulder is usually called *non-lattice oxygen* and can have various origins, as C–O contributions from carbon contaminants

and interstitial oxygen. Additionally, the Hf 4s photoemission line is also located in this region around 530 eV, even if its cross section is rather small.

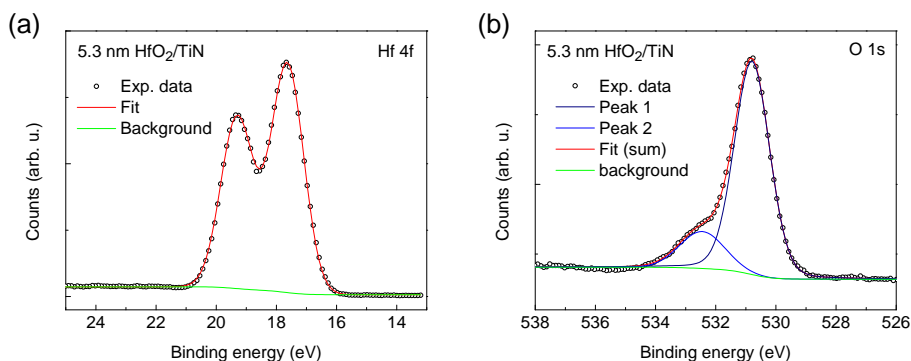


Figure 3.3: (a) High resolution Hf 4f core level spectrum of the 5.3 nm thick HfO_2 film. (b) High resolution O 1s core level spectrum of the same film.

The Hf 4f and Al 2s high resolution spectra coming from the Al: HfO_2 film are reported in Figure 3.4. The introduction of Alumina cycles during the ALD oxide growth results in the Al 2s peak located at 119.9 eV (width 1.96 eV), compatible with Al–O bonding in sub-stoichiometric Al_2O_3 . Apart from this, the Hf 4f double peak is rather similar to the one of the HfO_2 film, and the distance between the O 1s and the Hf 4f main peaks is also compatible with the previously found distance within 0.1 eV. This is a further indication that, within the measurement sensitivity, the introduction of Al atoms with a 1:6 growth ratio does not noticeably change the Hf stoichiometry.

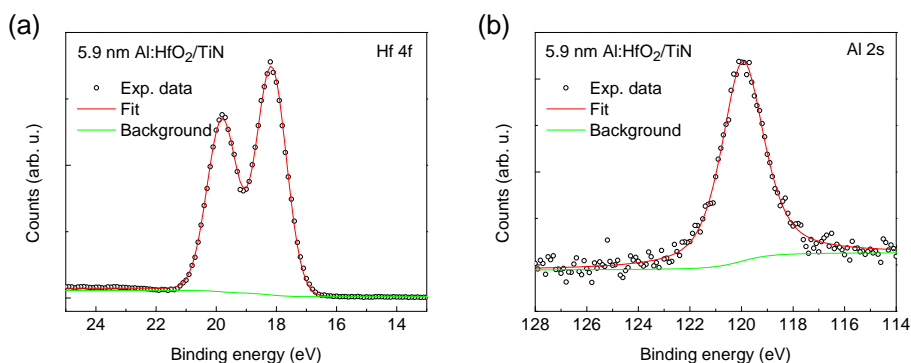


Figure 3.4: (a) High resolution Hf 4f core level spectrum of the 5.9 nm thick Al: HfO_2 film. (b) High resolution Al 2s core level spectrum of the same film.

All the previously shown spectra were acquired with a take-off angle of 80° in order to get the maximum depth sensitivity. It is however worth to note that all the aforementioned values are in agreement with values estimated from spectra acquired at lower angles, meaning that within the measurement sensitivity the grown films exhibit an almost uniform composition throughout the film thickness.

Interface with the TiN bottom electrode Given the limited mean free path of the photoemitted electrons through the oxide layer, chemical information on the oxide/TiN interface was acquired using thin films of 3 nm HfO₂ and Al:HfO₂ on top of the TiN substrate (samples SAV647 and SAV655 reported in Table 3.1). In the thin HfO₂ sample, the signal coming from the Hf 4f (Figure 3.5(a)) is similar to the one obtained from the thicker sample (same O 1s – Hf 4f energy difference and 1.68 eV peak width), with also a similar O 1s spectrum (not reported here for sake of conciseness). This means that in spite of the lower number of ALD cycles, the chemical composition of these thin films is similar to the one of the thicker films.

The Ti 2p_{3/2} and 2p_{1/2} signals coming from the bottom interface and acquired with 80° take-off angle for maximum depth sensitivity are reported in Figure 3.5(b). The spectrum displays major contributions at the line positions of the TiO₂ composition (458.6 eV, 1.44 eV peak width), which accounts for roughly 50% of the total peaks area. A pronounced and broad shoulder is visible at lower binding energy, which corresponds to the line positions of a broad range of sub-stoichiometric TiO_x and TiN_y compounds. The deconvolution of these shoulders with total width over 3 eV can be fitted with at least two additional double peaks with width of 1.44 eV, confirming the broad range of TiO_xN_y compounds which form at the oxide/TiN interface. On the contrary, no detectable signal can be found from the TiN film, probably due to the signal attenuation resulting from the thick oxide which forms at the TiN upper surface.

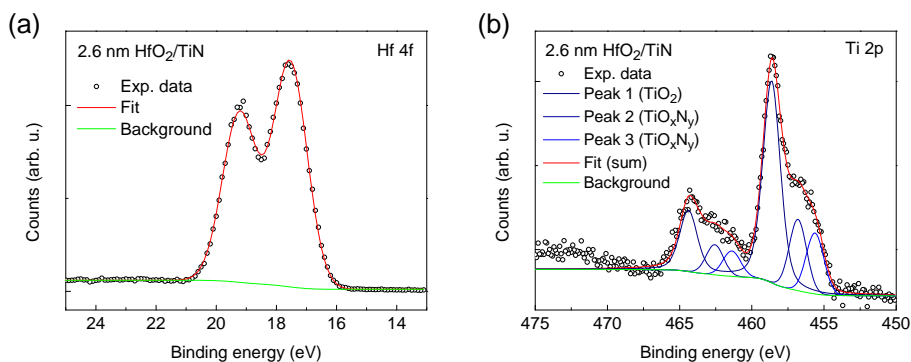


Figure 3.5: (a) High resolution Hf 4f core level spectrum of the 2.6 nm thick HfO₂ film. (b) High resolution Ti 2p core level spectrum of the same film.

As a comparison, the Ti 2p signal reported in Figure 3.6(a) was acquired on a TiN film prior to the deposition of the oxide film. This spectrum is similar to the one shown in Figure 3.5(b), with a similar content of TiO₂ and TiO_xN_y compounds. This is an indication that the formation of an oxide film over the TiN electrode occurs before the ALD deposition due exposure to air, even though an additional oxidation during the first ALD cycles cannot be excluded. In addition, also in this spectrum any contribution from stoichiometric TiN is not detected as a result of the presence of a layer with mixed TiO_xN_y composition. It is worth to note that all the reported spectra were acquired at nearly normal configuration (80° take-off angle). However, as an angle-dependent analysis did not reveal any major angle dependence, a uniform composition of the upper oxide film is expected throughout the depth probed by the photoemitted electrons.

Given the exponential signal attenuation, a lower bound for the oxide thickness can be estimated knowing the inelastic mean free path (IMFP) of the photoelectrons with

energy E_B . While the IMFP strongly depends on the metallic or insulating behavior of the material and changes according to the TiO_xN_y stoichiometry, for the TiO_2 and TiN materials it is limited in a range of 1.5 – 3 nm, and the thickness of the surface oxide layer can be at least estimated to be 2 – 3 nm. At least the same thickness can be expected also to develop at the HfO_2/TiN interface as a result of the TiN exposure to air and following ALD in oxidizing atmosphere.

Another indication of the broad range of sub-oxide and sub-nitride compounds at the upper TiN surface derives from the N 1s spectrum of Figure 3.6(b), in which three distinct peaks are clearly visible. The most intense peaks at 397.0 eV and 395.9 eV correspond to sub-stoichiometric TiN_x (with $x < 1$), while the broader peak at 398.7 eV could account for interstitial nitrogen or N–C bonds. A clear signal corresponding to the TiN stoichiometry would reside at the left of the main peak, around 397.8 eV, where no shoulder can be clearly identified.

A final consideration is required for the O 1s spectrum of the TiN substrate (Figure 3.6(c)). Two main peaks can be deconvoluted also in this case. The binding energy position of the main peak is similar to the one reported in Figure 3.5, since the HfO_2 and the TiO_2 stoichiometric oxides have similar O 1s peak positions. However, for the TiN substrate, the second peak at higher binding energy has much stronger intensity and accounts for 40% of the total area, probably due to a stronger lattice disorder and the presence of a bigger amount of interstitial oxygen. Since passing from an acquisition angle of 80° to an almost tangent angle (45°) the second peak integrated intensity increases to 42%, the *non-lattice oxygen* is found to increase next to the superficial region.

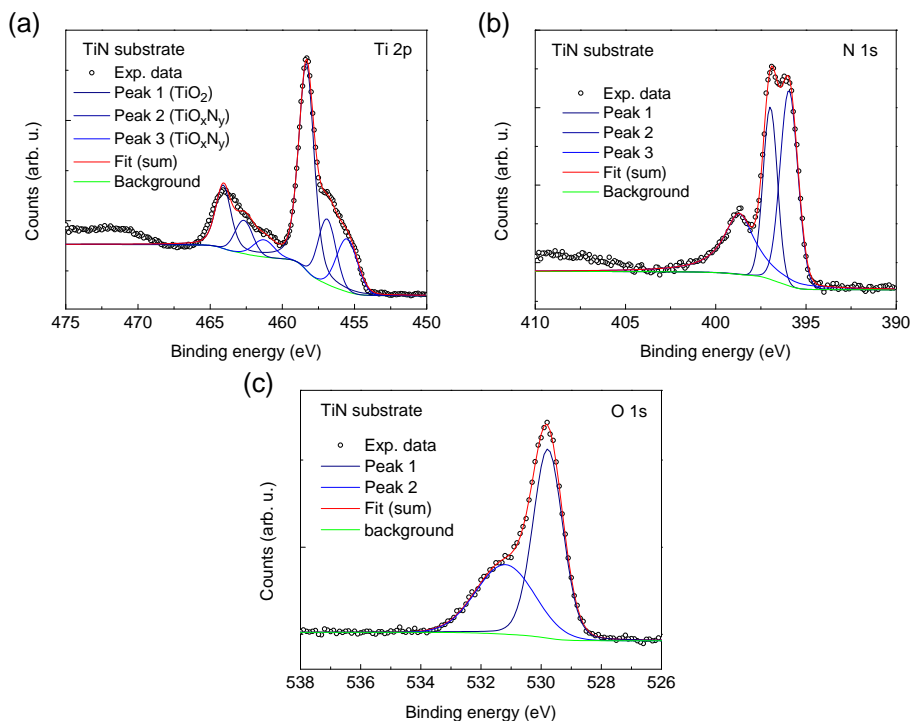


Figure 3.6: High resolution spectra of the TiN film. (a) Ti 2p core level spectrum; (b) N 1s core level spectrum; (c) O 1s core level spectrum.

In conclusion, the analyzed structure can be summarized as HfO₂/TiO_xN_y/TiN, where the TiO_xN_y layer includes all the aforementioned contributions from the oxidized TiN surface. In this contest, the interface roughness around 3 nm derived from fitting of the XRR data in Table 3.1 can be by a large extent explained by the presence of this sub-stoichiometric oxi-nitride compound at the interface between the HfO₂ and the TiN layer.

3.3 Electrical characterization

Electrical characterization of μm-size devices was performed using a B1500A semiconductor device parameter analyzer integrating four source/measure unit (SMU) modules, one semiconductor pulse generator unit (SPGU), and a ground unit (GNDU). The different modules were connected through triaxial cables to a metal box containing the probe station, which ensures electrical isolation and shielding from the external light. Inside the metal box, the signal was passed to the probe station, where three manipulators for the x, y, and z axes allow the precise positioning of tungsten needles on the surface of the devices, allowing for a proper contact.

A set of devices was built for the investigation of the electrical properties of RRAM cells based on Al:HfO₂ switching material. First, the fabrication of μ-size devices is presented. Pt metal electrodes were defined by UV lithography on top of the Al:HfO₂/TiN stack presented in the previous section (Figure 3.7). Afterward, different device characterization measurements are illustrated.

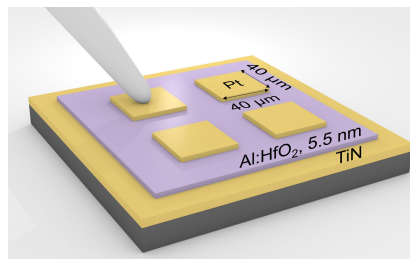


Figure 3.7: Pictorial view of the μ-size devices fabricated by Pt electrode patterning on top of the HfO₂/TiN stack.

Device fabrication As top electrode, a film of 50 nm Pt was deposited at room temperature by DC sputtering (100 W DC power; 40 sccm Ar flow) with a deposition rate of ~8 nm/min.

For electrical testing, the top electrodes of the memory devices need to be patterned with a defined area. To this purpose, a positive photoresist was spin-coated over the dielectric layer and exposed to UV light through the lithographic mask of Figure 3.8. After development, the exposed parts of the resist were removed and Pt was deposited on top. Finally, a lift-off process in acetone removed the residual photoresist and the excess metal to define the top electrodes.

The mask used for top electrodes patterning allows to produce capacitor structures with area between $1.6 \times 10^{-5} \text{ cm}^2$ and $1.6 \times 10^{-3} \text{ cm}^2$. While this dimension permits an

easy contact of the tungsten probes for an effortless electrical characterization, the study of the device properties at the nanoscale requires alternative patterning procedures. This aspect will be discussed in length in chapters 4 and 5, where an innovative lithographic approach based on block copolymer self-assembly will be presented.

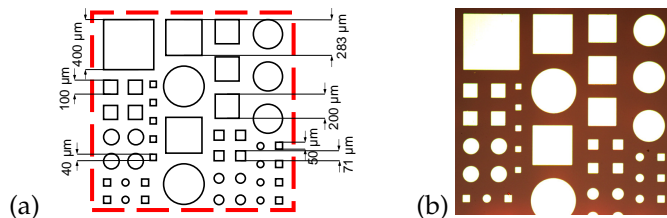


Figure 3.8: (a) Schematic of the lithographic mask applied for the top electrode patterning of the resistive switching memory cells. (b) Optical microscopy image of the patterned top electrodes.

3.3.1 Bipolar voltage sweeps

The application of ramped voltage sweeps while simultaneously measuring the current allows to probe the evolution of the memory cell resistance state as a function of the applied voltage. In the set-up configuration used, the top electrode of the selected memory cell was connected to one SMU in order to apply the required voltage and sense the current, while the bottom electrode was grounded through another SMU.

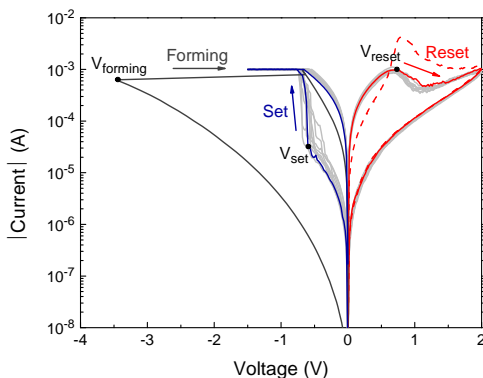


Figure 3.9: Bipolar voltage operations in a Pt/HfO₂/TiO_xN_y/TiN device. An initial forming step is required to establish the low resistance state and allow resistance switching operations (dark gray). The subsequent reset (dashed red line) leads to the high resistance state, while it exhibits an *anomalous current peak* not present in the following reset operations. A detailed discussion of this first reset is reported in section 3.3.3. In blue line, the first set process, which restores the low resistance state. The next 10 cycles are reported in light gray line to depict the dispersion among repeated cycles.

A typical current–voltage characteristic is reported in Figure 3.9 for a device composed of a TiN bottom electrode, an HfO₂ dielectric and a Pt top electrode. Starting from

a pristine state resistance of about 10 M Ω (measured at 10 mV), the application of a negative current-controlled voltage sweep allows to obtain a change in resistance down to about 3 k Ω by a process usually called *Forming* operation, leading to the low resistance state (LRS). The transition appears at roughly -3.5 V with an abrupt decrease of the voltage at almost equal applied current. A subsequent voltage sweep at positive voltage polarity leads to the restoration of a high resistance state (HRS) through the usually called *reset* process. Starting from about 0.7 V, the current gradually lowers, marking the onset of the *reset* transition. This lowering continues up to 1.2 V, when the current starts increasing again. The reset process operated with a reset stop voltage of 2 V leads to a final HRS of about 30 k Ω . It is interesting to note that the first reset process after forming, here reported with a dashed line, displays an *anomalous current peak*. In spite of this current overshoot, the final resistance state is very similar to the one obtained in the following reset processes. The nature of the current overshoot will be discussed in detail in section 3.3.3 in connection with the system structure. Reversing again the polarity and applying a negative voltage, the LRS can be restored by a *set* process. The transition displays a rather sharp increase of the current starting from -0.5 V, which continues until the current compliance set by the instrument is met. For a current compliance of 1 mA, a final resistance value of 800 Ω is obtained. The reversible nature of the resistive switching phenomenon is highlighted in Figure 3.9 by the following series of repeated resistance switching cycles.

Forming The forming process corresponds to a *soft breakdown* undergoing in the dielectric material and leads to the formation of a conductive path between the two electrodes. In HfO₂-based devices, the now widely accepted mechanism for resistance switching is related to the formation of one (or more) conductive filaments that short the two electrodes of the M–I–M stack [8, 9].

While operating the forming process, it should be avoided a *hard breakdown* that would irreversibly degrade the dielectric and prevent a reset process. Moreover, the maximum current allowed during the forming process is a fundamental parameter in determining the characteristics of the filament. In particular, once that a conductive filament has been established in the oxide, any additional current flow determines an enlargement of the filament and lowers the final LRS resistance. Therefore, the maximum current should be controlled in order to obtain reproducible results and reduce the operating power of the device.

One method to control the forming operation is to perform a current-controlled sweep. In this way, the maximum current allowed to flow through the device is easily controlled by the maximum value of the current ramp. Alternatively, a current compliance can be provided in a voltage-controlled sweep.

An alternative method to control the forming process is the use of a transistor in series with the device. In this case, the maximum allowed current is determined by the gate voltage applied to the transistor. The advantage of a series transistor is that the response to sudden changes in the current is supposed to be faster than the internal response time of the parameter analyzer, which should lead to a better control over the LRS. In Figure 3.10 it is reported an example of a forming operation and subsequent bipolar voltage cycles executed with a current limitation imposed by a JFET transistor in series with the device. Note however that the transistor in this case was placed in an external board and not directly integrated in the wafer of the RRAM devices. It should be noted moreover that cycles reported in Figure 3.10 operate the cell in a different regime at lower current

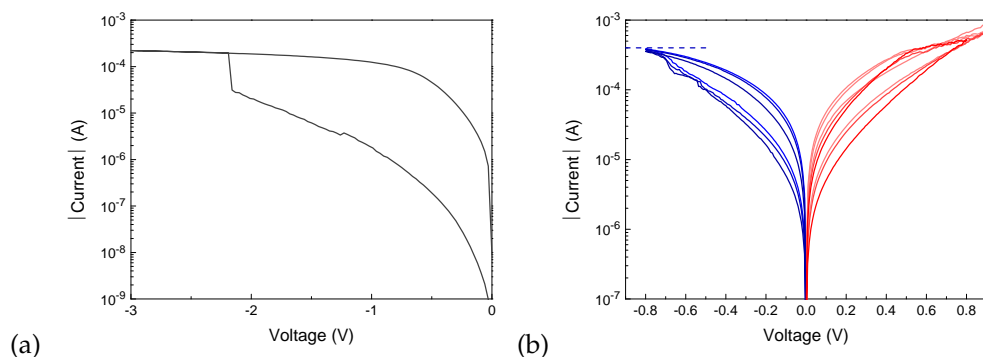


Figure 3.10: Forming and subsequent bipolar operations obtained with a current limitation set by a series JFET transistor. The maximum allowed current is $200\ \mu\text{A}$ during forming and $400\ \mu\text{A}$ during set operations. No current limitation is imposed during the reset operations.

and voltage with respect to Figure 3.9, producing in a narrower memory window.

Finally, another approach to limit the current is to build a resistive divider by placing a resistor in series with the resistive memory element only during forming/set operations. An interfacial layer such as a TiO_xN_y layer formed by electrode oxidation [10, 11] or other oxide layers interposed between the electrode and the switching oxide can also effectively limit the current flowing through the device. Complicated stacks containing multiple layers were designed to optimize the switching power during fast operations without sacrificing the retention and endurance properties [12].

Reset The final HRS resistance mainly depends on the maximum applied voltage. This can be visualized in Figure 3.11(a), in which consecutive positive voltage sweeps with increasing stop voltages are executed. Each reset cycle closely follows the previous curve, slightly increasing the final reset state with an almost exponential dependence on the reset stop voltage (Figure 3.11(b)). This fine tuning of the HRS resistance is possible thanks to the gradual reset transition that occurs in the system, as opposed to the rather sharp set transition.

The resistance increase during reset can be explained by a progressive filament thinning and eventual rupturing due to oxygen vacancies migration and electro-chemical reactions that lead to the filament partial reoxidation. When a gap is created in the filament, the electron tunneling current exponentially depends on the gap length. Even a small gap of the order of a few nm or less can explain the decrease of the resistance in the HRS.

Set Similarly to the forming step, during the set transition the maximum current passing through the device should be carefully controlled to avoid hard breakdown in the switching oxide. In Figure 3.11(c) and (d), a two decades variation of the LRS resistance was achieved by a similar variation over two decades of the current compliance imposed during the set process. This allows to fine tune the LRS resistance, with the boundary conditions that for a too low compliance current no set transitions occurs, while for a too high current an irreversible hard breakdown can be induced in the oxide. As discussed previously for the forming process, an alternative way to control the LRS resistance is to

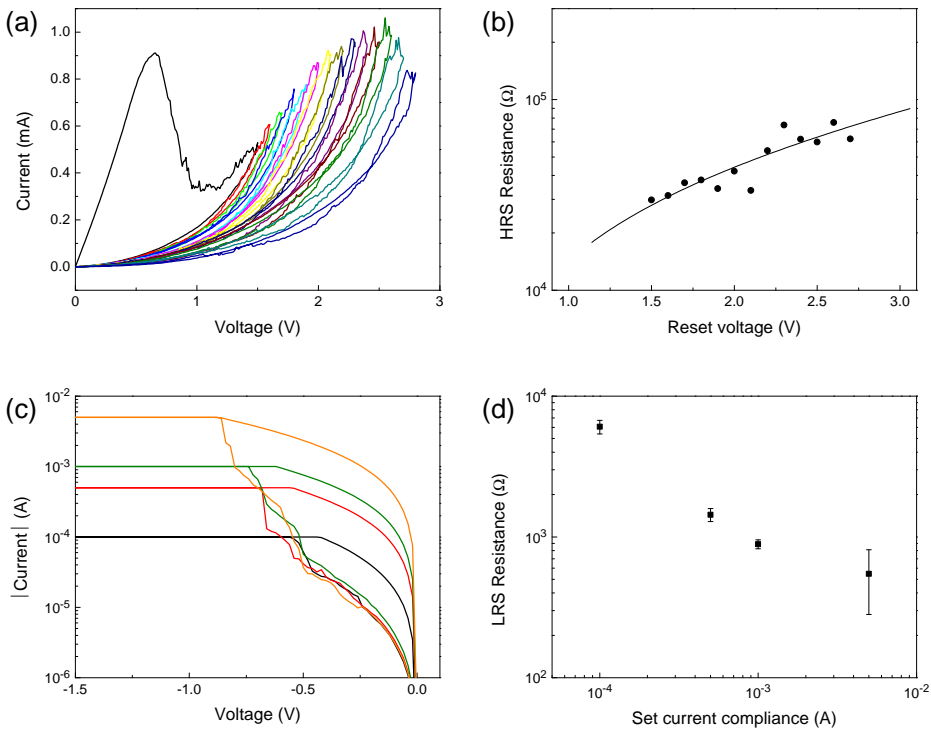


Figure 3.11: Adjustment of the HRS and LRS resistances obtained with a variation of the reset stop voltage and of the current compliance imposed during set, respectively. (a) Incremental reset processes. Each curve corresponds to a voltage sweep with stop voltage increased by 0.1 V. (b) HRS resistance variation as a function of the reset stop voltage. (c) Set processes executed with different current compliance, and (d) corresponding variation of the LRS resistance.

exploit the current limitation of a series transistor. By adjusting the gate voltage, a fine variation of the LRS resistance can be obtained.

The main difference between the initial forming step and the subsequent set transitions is that during set the filament is already formed and only a small portion of the oxide is subject to filament regrowth. This implies that, as visible in Figure 3.9, the resistance prior to the set transition is much lower than in the pristine state, and the electric field necessary to induce the set transition is also lower than in the forming step, which translates in set voltage lower than the forming voltage.

3.3.2 Device area dependence

The lithographic mask used to define the device top electrodes allows to pattern areas from $1.6 \times 10^{-5} \text{ cm}^2$ to $1.6 \times 10^{-3} \text{ cm}^2$. The corresponding HRS and LRS resistances are visualized in Figure 3.12. No major resistance variation can be observed for the corresponding two decades of area variation, strongly supporting the filamentary mechanism.

Watching closely to the HRS trend, a larger resistance spread is obtained for larger

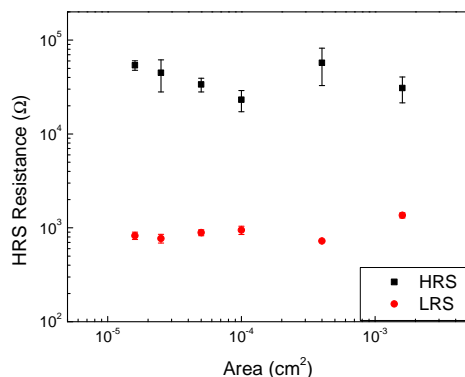


Figure 3.12: HRS and LRS resistance values for different device areas.

device areas. Considering this uncertainty, a slight increase of the HRS resistance for decreasing area seems visible starting from 10^{-4} cm² downward, while the LRS remains unchanged. This could be consistent with the fact that while the LRS mainly depends on the conduction through the filament, in the HRS a not negligible contribution comes from the leakage current through the whole device area, a trend recently confirmed in ultra-scaled devices [13].

The device areas tested at this stage are quite big when compared to the filament size (~ 10 nm of lateral scale [14]) and to standard microelectronic memory devices and where built with the only purpose to test the material properties. A careful investigation of the device scaling should imply lateral dimensions down to a few nm and a different patterning technique, which will be the focus of chapters 4 and 5.

3.3.3 Role of the metal–oxide interface on the switching behavior

Multiple resistance switching operation regimes are possible in the same Pt/HfO₂/TiO_x-N_y/TiN device. As previously discussed, the usual switching operation reported for the considered device stack requires an initial forming step followed by bipolar voltage operations with a clockwise direction of the current–voltage curves. This behavior is reported in Figure 3.9. The same CW switching is also shown in Figure 3.13 for the curves comprised in the restricted window range between -2 V and $+2$ V. However, also counterclockwise and complementary switching operations were obtained in the same device. These multiple regimes can be explained by considering a competing dynamics between the conductive filament formation and dissolution at the two opposite Pt/HfO₂ and HfO₂/TiN interfaces and highlight the role of the metal/oxide interface region.

The first reset after the initial forming displays an unusual current jump above the current value imposed by the current compliance during the previous forming operation, followed by a steep current decrease. This behavior is typical only of the first reset and is not reproduced in the subsequent reset cycles and is thus called *anomalous reset peak*.

Increasing the applied reset voltage, it is possible to increase the high resistance of the device, up to a point at which the same initial resistance of the pristine state is reached. For the tested devices, this full reset can be accomplished around 3.5 V. As reported in Figure 3.13(a), after the full reset, a following set operation carried out until -3.5

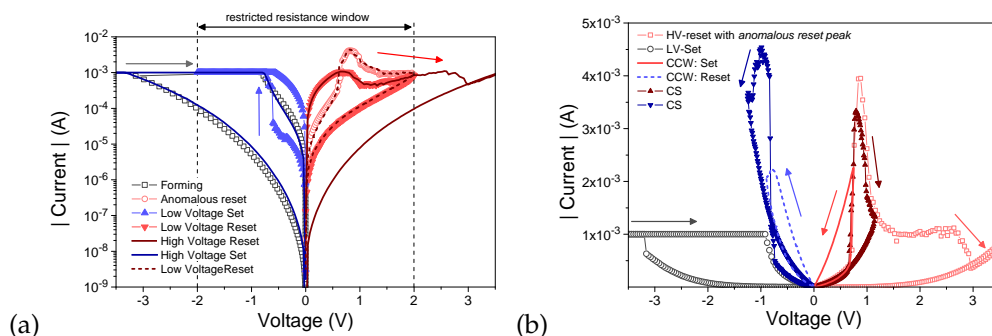


Figure 3.13: Multiple resistive switching operations performed in the same Pt/HfO₂/TiO_xN_y/TiN device. (a) Forming and low voltage bipolar clockwise switching between -2 V and $+2$ V. A high voltage reset up to 3.5 V is followed by a set process similar to the initial forming. (b) Varying the stop voltage during set and reset, counterclockwise and complementary switching regimes can be achieved (without any current compliance). Reprinted from [15].

V results in an overlapping with the initial forming operation, indicating that a nearly complete dissolution of the conductive filament occurred during the full reset. It is interesting to note that the subsequent reset results in a reappearance of the *anomalous reset peak*.

The extended resistive switching operation in the $-3.5 - 3.5$ voltage range occurs in the usual clockwise direction. However, reproducing the anomalous reset peak allows to exploit the rising shoulder for different switching operations if the voltage range is carefully adjusted. In Figure 3.13(b), both counterclockwise switching and a complementary switching regime are highlighted. After the negative high-voltage set, the rising shoulder of the *anomalous reset peak* provides an additional set transition for the opposite voltage polarity, reversing the direction of the switching curves. Afterward, reversing again the applied polarity, a reset process for negative voltage can be achieved. In a similar way, if after the high-voltage set the positive voltage sweep is protracted slightly over the anomalous peak shoulder, a set and a reset process take place one right after the other. Reversing the voltage polarity, the same set and reset features in succession can be obtained with the opposite polarity, resulting in a complementary switching regime.

The counterclockwise and complementary switching operations only happen in a restricted voltage range and lead to a narrow memory window. However, these interesting behaviors highlight that the rising shoulder of the *anomalous reset peak* can be interpreted as a set process occurring right before the reset process. The explanation of these particular behaviors can be found in the double-layer oxide stack that forms due to TiN upper surface oxidation and that was illustrated in section 3.2.1 following the XPS analysis of the HfO₂/TiN interface.

The drawing of Figure 3.14 summarizes with a pictorial single-filament model the conductive filament formation and dissolution in the device stack for the different set and reset processes. Starting from the cell pristine state, the forming step leads to the formation of a conductive filament throughout the film thickness. However, the overshoot due to discharge of parasitic capacitances or to inefficient current limitation in combination with the high applied voltage provokes a further evolution of the filament arrangement: the ion migration continues, depleting the bottom interface of oxygen vacancies and accumulating them at the top interface. On the other hand, the oxygen

species move in the opposite direction towards the bottom interface contributing in oxidizing the filament in the TiO_xN_y layer. Finally, the opening of a small gap is produced. This filament evolution is supported by the experimental evidence that after forming at negative voltage, the application of a positive voltage is able to further decrease the resistance, which in essence corresponds to the rising shoulder of the *anomalous reset peak*. While the typical clockwise operation implies the partial dissolution of the filament at the Pt/ HfO_2 interface, the exploitation of the filament dissolution at the opposite bottom interface enables a counterclockwise switching regime. Finally, the competitive switching of the opposite metal/oxide interfaces can explain the complementary switching regime, in which the filament formation and dissolution occurs at both interfaces. The TiO_xN_y layer is determinant because it preferentially switches with an opposite polarity with respect to the HfO_2 layer and, for this reason, it provides the competition that prevents an extreme filament growth and finally allows the restoration of a resistance close to the pre-forming level during the high-voltage reset.

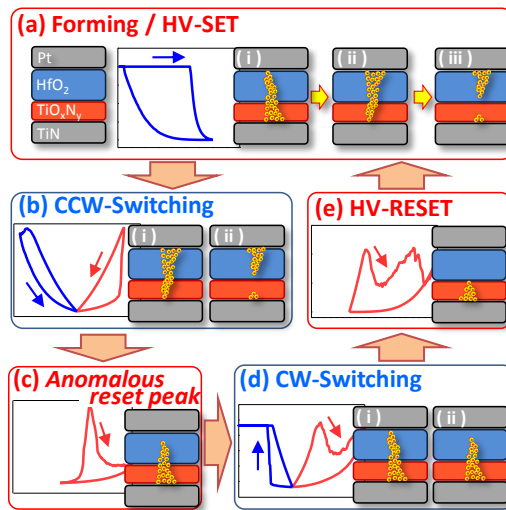


Figure 3.14: Pictorial model of the switching in Pt/ HfO_2 / TiO_xN_y /TiN devices. Blue panels correspond to switching modes and red panels to transient operations from one mode to another. (a) Forming or HV-set processes described in three steps: formation of a conic CF (i), that is reversed (ii) and dissolved at the bottom interface (iii). (b) Picture CCW switching and (c) the anomalous reset peak. (d) CW switching at low voltage. (e) The HV-reset allows restarting from panels (a–i) to (a–iii). Reprinted from [15].

3.4 Effect of Al doping on the DC switching behavior

DC measurements were carried out in Al-doped devices with different Al concentrations to characterize the switching behavior and the memory performance as a function of the Al doping concentration. In addition to the un-doped HfO_2 -based devices just reported, Al: HfO_2 devices with an Al concentration of $(4.0 \pm 0.5) \%$ and $(7 \pm 1) \%$, as estimated by XPS analysis, were fabricated.

In the pristine state before forming, the measured leakage current strongly depends on both the oxide thickness and the dielectric properties. However, since all the oxide

films showed a similar amorphous structure, any difference in the initial-state conduction and in the forming voltage should be mainly ascribed to fluctuations of the oxide film thickness (Figure 3.15(a)). After forming, the LRS conduction mainly depends on the characteristics of the conductive filament, while the HRS depends on the extent to which the filament has been constricted or ruptured during reset (Figure 3.15(b)).

In the 4 %-doped devices, the DC switching cycles closely resemble the ones of the un-doped cells, with also similar LRS and HRS average values. Conversely, in the highly doped devices with 7% Al, for the same reset stop voltage, the HRS resistance is more than halved. This effect is typical of highly doped HfO₂ films and was already reported in several papers, while no detailed analysis as a function of the doping concentration can be found in the literature and is thus the scope of this investigation [16–18].

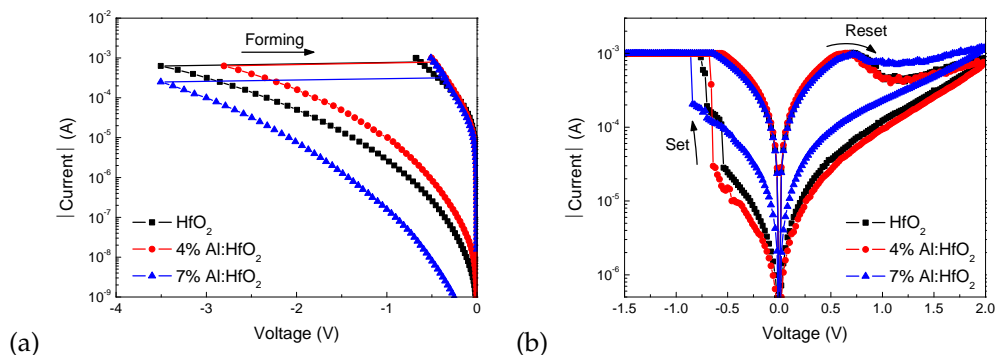


Figure 3.15: Forming (a) and (b) bipolar switching cycles obtained in an un-doped Pt/HfO₂/TiN device and in Al-doped devices with a similar stack and different Al doping concentrations.

3.4.1 Variability and endurance properties

One of the main concerns for the employment of RRAM in memory applications is the reproducibility of both the switching parameters (forming, set and reset voltages) and of the resistance states in repeated switching cycles and among different cells. The stochastic processes that underly the filament formation and dissolution inherent to the localized nature of the conductive filament cause a virtually zero probability of having exactly the same filament at each cycles and in each memory cell [19]. Even if the switching variability is somehow intrinsic to the switching mechanism, doping the HfO₂ layer with Al atoms was identified as a possible way to mitigate the switching fluctuations and improve the overall performance. Here, in order to understand the effect of the Al introduction, cumulative probability plots were constructed to display the variability distributions referred to either different devices or repeat cycles.

Variability among devices The variability among different devices is reported in Figure 3.16 for switching operations carried out with a current compliance of -1 mA and a reset stop voltage of 2 V. The switching voltage distribution extracted from at least 20 different memory cells is reported in Figure 3.16(a). In this plot, the forming voltage variation between the three type of devices is similar to the one reported in Figure 3.15(a). This is probably due to a slightly different oxide thickness variation among samples. Regarding the set and reset switching voltages, almost equivalent distributions are

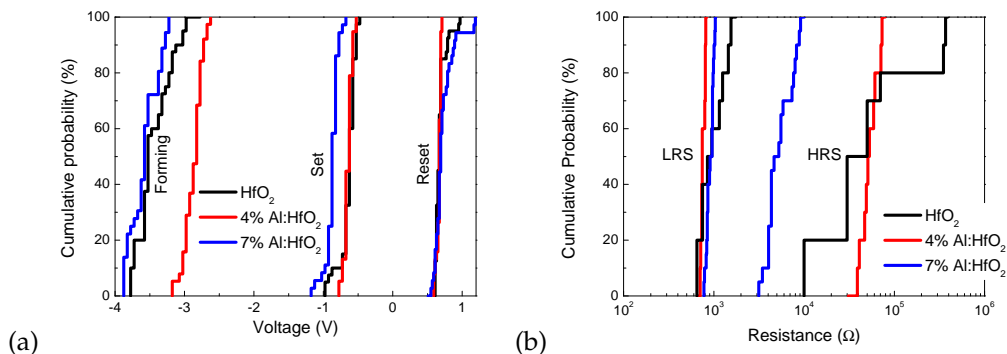


Figure 3.16: Cumulative plots of the device-to-device variability distributions of the switching voltages (a) and of the LRS and HRS resistances (b) for un-doped and Al-doped devices.

obtained for HfO₂-based and 4%-doped devices, with only a slight improvement of the distribution tail upon Al doping. On the other hand, higher Al concentration causes a worsening of the distribution tail and higher set voltages. Combining this latter increase of V_{set} with the lower HRS resistance and thus to the higher current prior to the set process (Figure 3.15(b)), an increase of the set switching power is determined for the highest Al doping concentration tested.

Considering now the resistance distribution, it is worth to mention that the LRS is mainly determined by the current compliance applied during set, which is an extrinsic factor with respect to the memory cell, and mainly depends on the reactivity of the current limitation. However, in Figure 3.16(b) an improvement of the device-to-device variability can be found in particular for the 4% doped devices. On the contrary, during the reset process no external current limitation is applied and the HRS distribution is a good benchmark of the intrinsic device variability. A clear improvement is again obtained for the 4% Al-doped devices, but for a quantitative comparison more statistics would be required for the un-doped devices, given their highly spread and thus staircase-shaped distribution. For the highly doped 7% Al-doped devices, an improved HRS distribution is also observed. However, it is accompanied to a marked closure of the memory window, as previously reported.

In conclusion, an improvement of the switching variability can be obtained for a 4% Al doping concentration, while for a higher 7% Al concentration this improvement is less evident and several drawbacks were identified.

Variability for repeated cycles Another key point to be considered when evaluating the cells variability is the degree of reproducibility for many switching cycles. Using the usual current compliance of -1 mA and 2 V of reset stop voltage, the obtained cumulative distribution for the switching voltages is reported in Figure 3.17(a). The distributions of the HfO₂ and 4% Al:HfO₂ devices are almost overlapped, while the cells based on the 7% Al:HfO₂ film again show higher set voltages and a slight worsening of the V_{reset} distribution.

The distributions of the switching voltages, and in particular of V_{reset} , also depend on the switching parameters. As an example, in Figure 3.17(b) the distribution of V_{set} is reported for three different reset stop voltages. Increasing the stop voltage from 2 V

to 2.5 V allows to increase the HRS without any noticeable worsening of the set voltage distribution, while for a higher reset at 3 V a broad range of effective V_{set} values is found.

Concerning the resistance variability among cycles (Figure 3.17(c)), the general picture is consistent with what is observed with the device-to-device distribution: a slight improvement of the HRS distribution is observed upon 4% Al doping, while for higher doping the variability improvement comes at the cost of a reduced memory window.

For the case of the 4% doped devices, a more visible improvement is found by increasing the reset stop voltage to 3 V (Figure 3.17(d)), which brings the HRS resistance up to 1 M Ω . Even if the drawback is the worsening of the LRS distribution, the memory window increases from 26 X at 2 V to 3000 X at 3 V.

In conclusion, doping with 4% Al allows to mitigate the effect of HRS distribution broadening for high reset stop voltages (>2.5 V), while for lower reset values the cycling variability improvement is less marked. On the other hand, increasing the Al content to 7% comes at the cost of a reduced memory window.

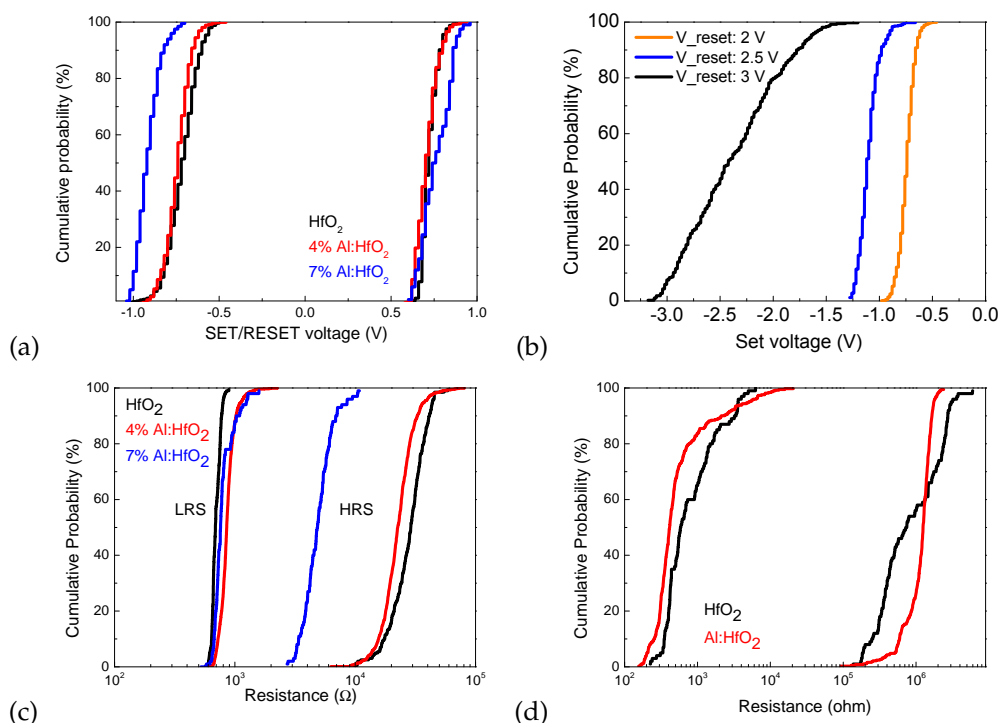


Figure 3.17: Cumulative plots of the variability distributions for at least 200 switching cycles. (a) Set and reset voltage distributions for operation carried out with 2 V reset stop voltage and -1 mA current compliance during set. (b) Distributions of the set voltage after reset processes at different maximum voltages. (c) LRS and HRS resistance distributions for operations at 2 V reset/ -1 mA current compliance during set. (d) Same resistance distributions for a reset stop voltage of 3 V.

Endurance The cumulative plots presented in the previous section are representative of 1000 DC cycles, and information about an eventual resistance deterioration for repeated cycling is embedded in the distribution. However, to better evaluate the en-

duration properties of the LRS and HRS states, a useful display of data is in the form presented in Figure 3.18.

For the first ~ 200 cycles, the HRS resistance of both the doped and un-doped cells gradually lowers and then settles. While the 4% Al-doped device shows a slightly more pronounced HRS resistance lowering, the resistance values are much less spread. No endurance failure was observed up to 2000 DC cycles for the tested devices using the standard 2 V reset and -1 mA current compliance during set. However, the endurance property strongly depends on the programming conditions. In Figure 3.18(b), the cycling variation for different reset stop voltages is reported. Interestingly, with a reset at 3 V the cell not only presents higher spreading of the resistances, as already reported, but a retention failure occurred after 380 cycles. In this case, an oxide breakdown led the cell to an unrecoverable LRS of a few Ω .

Various mechanisms could lead to endurance failure. In the literature, the most common failure event reported for the HRS is the impossibility to reset the cell after a certain number of cycles, while for the LRS a common issue is an irreversible oxide breakdown [20, 21]. However, the prevailing mechanism for endurance failure strongly depends on the programming conditions [22].

The long DC measurements prevent a statistically relevant analysis of the phenomenon associated with endurance failure. Moreover, it is worth to mention that DC programming causes an electrical stress much more severe than with switching pulses, which is the programming method commonly applied in memory applications. For this reason, DC cycles can only give a lower boundary for the number of possible repeated switching cycles before any degradation mechanism occurs in the tested device.

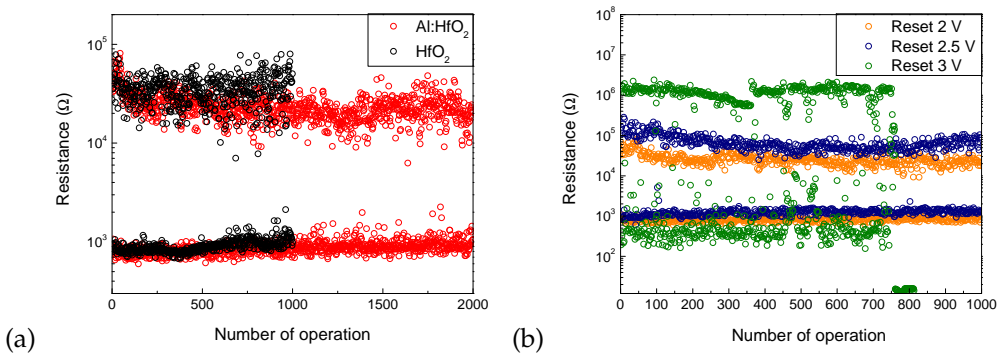


Figure 3.18: (a) Repeated switching cycles for the HfO₂ and the 4% Al:HfO₂ devices. (b) Comparison between the first 1000 DC cycles for the 4% Al:HfO₂ sample obtained for different reset stop voltages. The test operated with a 3 V reset shows retention failure after the 760th reset.

3.4.2 Retention measurements

In this work, a particular focus was devoted to the determination of the mechanisms that lead to a loss of the memory state through time. The retention measurements were carried out for all the three types of devices with Pt/HfO₂/TiN memory stack and Al-doped HfO₂ films. The resistance state of the cells was monitored for times up to 10^6 s and the storage temperature between consecutive measurements was varied between room temperature (23 °C) and 180 °C.

The experimental procedure consisted in an initial current-controlled forming step up to -1 mA and 10 consecutive reset/set DC cycles to check for cycling repeatability and ensure cell functionality. For the LRS, the current compliance was set to -1 mA, while the HRS was obtained by ramping the voltage up to 2 V. Given the lower ON/OFF ratio achieved with the highly doped 7% Al:HfO₂ devices, an additional resistance state was tested with an HRS resistance similar to the one obtained with the un-doped and 4% Al-doped devices, which was obtained by progressively increasing the reset stop voltage until the target resistance state was met. After cycling, the memory cells were programmed to either the LRS or the HRS and at least 20 cells were baked at the temperatures of choice. At time intervals arranged logarithmically, the memory state was monitored at room temperature by reading DC voltage sweeps. A low reading voltage of 10 mV was chosen in order to minimize the voltage-induced stress on the devices.

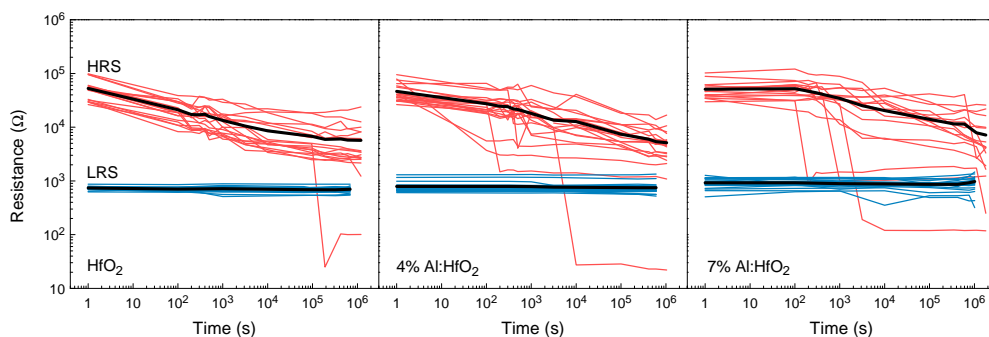


Figure 3.19: Comparison between the retention characteristics at 150 °C of the un-doped and Al-doped samples. The black line depicts the average value of the cells. For the 7%-doped devices, the reset stop voltage was increased in order to obtain the same initial HRS as of the un-doped and 4%-doped cells.

The retention characteristics acquired at 150 °C are reported in Figure 3.19, in which the HRS for 7% doped devices has been increased to a level comparable to the other devices. Considering the LRS, no significant variation can be identified as a function of time for all the inspected samples. This consideration holds true for the whole range of tested temperatures. Hence, for the particular choice of the switching parameters, the conductive filament exhibits a high stability even at high temperature. On the contrary, two main mechanisms can be identified for the HRS retention degradation in these cells. The main HRS trend is a gradual lowering of the resistance as a function of time, while a number of cells exhibit a complete loss of the HRS between two consecutive measures. This latter population was named *failure bits*, since the sudden resistance drop leads to a complete loss of the HRS.

The retention failure phenomenon associated with sharp resistance transitions was already reported in the literature for cells based on hafnium dioxide [23]. In this work, we were able to identify also the effect of oxide doping with aluminum. As visible in Figure 3.19, this effect strongly depends on the doping concentration and is particularly relevant for the 7% Al-doped devices, for which $\sim 50\%$ of the memory cells exhibit sudden transitions within 10^6 s and it constitutes the predominant retention loss mechanism. Given the high relative amount of failure bits, in the following statistical analysis

the highly doped devices will be treated separately.

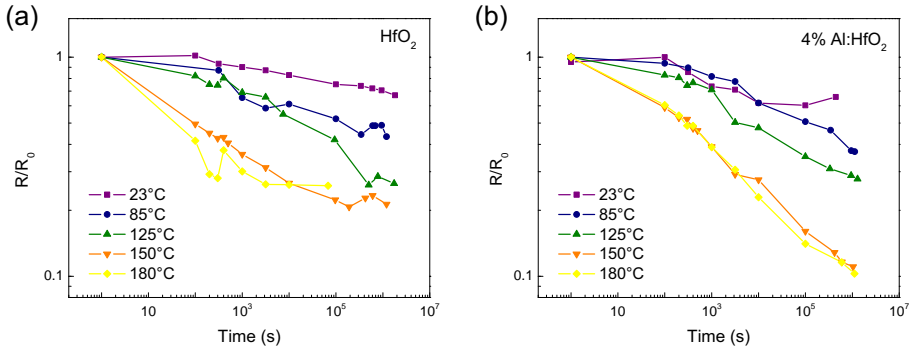


Figure 3.20: Normalized average HRS values as a function of time at various temperatures for the HfO_2 (a) and 4% Al:HfO₂ samples (b).

Gradual resistance lowering Thanks to the relatively long measurement time and to the temperature range tested, we were able to identify a gradual lowering of the average resistance in the retention characteristics. This phenomenon strongly depends on temperature, as shown in Figure 3.20. The average HRS decay rate normalized to the initial resistance of the un-doped and 4% Al-doped devices shows an almost linear behavior in a double logarithmic scale and increases with baking temperature. For a quantitative analysis, the time in which the cells lose half of their initial resistance value ($\tau_{1/2}$) was extracted. This definition was chosen since, excluding room temperature, $\tau_{1/2}$ lies inside the measurement range for the whole 85°C – 185°C temperature range, and no extrapolation is required. However, it is worth noting that half of the resistance value corresponds to a small variation of the memory window and does not prevent to reliably distinguish the HRS from the LRS; thus it is not a proper definition for the failure time.

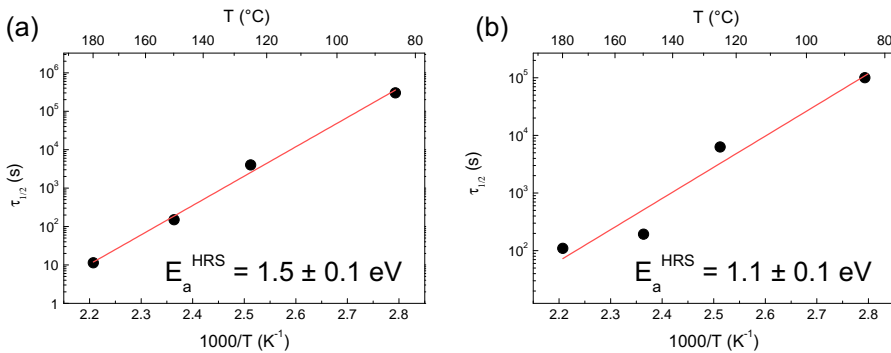


Figure 3.21: Arrhenius plot of the extracted decay time for the HfO_2 (a) and 4% Al:HfO₂ samples (b). $\tau_{1/2}$ represents the time in which the cells lose half of their initial resistance value.

Plotting $\tau_{1/2}$ as a function of $1/T$, the obtained Arrhenius plots reported in Figure

3.21 are typical of a temperature-activated process. Fitting the two plots with the law

$$\tau_{1/2} = Ae^{-E_a^{HRS}/kT}$$

allows to determine the activation energy (E_a^{HRS}) for the process of gradual filament recovery after reset for the HfO₂ and the 4% Al:HfO₂ devices. For the un-doped cells, an activation energy of (1.5 ± 0.1) eV can be derived from the slope of the fitting line of Figure 3.21(a), while for the 4% Al-doped samples a lower E_a^{HRS} of (1.1 ± 0.1) eV is extracted from Figure 3.21(b). These values are effective activation energies and were obtained at equilibrium, with only a negligible field applied during reading.

Repeating the same process for the 7% Al:HfO₂ devices results in an even lower value of (0.7 ± 0.5) eV, which is however affected by high uncertainty due the presence of the failure bits.

In order to understand the process responsible for the gradual HRS lowering, it is worth to compare the extracted activation energies with data reported in the literature from *ab initio* simulation and experimental approaches. In particular, the magnitude of E_a^{HRS} is compatible with the energy barrier for oxygen self-diffusion in HfO₂ films [24–26]. Moreover, Zhang et al. reported similar E_a reduction from ~ 2 eV to ~ 1 eV upon introduction of substitutional Al atoms in the HfO₂ lattice [27]. This lower E_a^{HRS} and thus the faster retention loss associated with the Al atoms introduction in the film can be understood in terms of an enhanced oxygen self-diffusion in the film, which brings a faster filament recovery. Indeed, the local stoichiometry of the film, together with its structure and defect density, are important factors in determining the effective energy barrier for the diffusion of oxygen species [28].

From *ab initio* simulation of monocrystalline or amorphous films, in general higher energy barriers of about 2 eV are derived. The slight discrepancy with the experimental data can be explained by the presence of defects in the film, which should be particularly relevant in the neighborhood of the conductive filament. Indeed, calculations considering oxygen vacancies in the film found E_a down to values comparable to the one found for the HfO₂ film [29], while for highly under-stoichiometric films values down to ~ 0.6 eV were calculated. Moreover, in amorphous films, an increase in density due to atoms rearrangement was also found to lead to E_a around ~ 1.6 eV [25].

In this framework, the retention loss can be depicted as follow: during reset, a small gap is created in the conductive filament, partially rupturing the filament [8]. After baking, the retention loss can be explained by oxygen vacancies diffusing back in the gap region, driven mainly by the concentration gradient, gradually restoring the broken filament.

In order to evaluate the long-term retention properties, a commonly employed criterion for comparison is the 10 years retention goal, defined as the temperature at which, after 10 years, the average HRS resistance reaches a value compatible with the LRS (complete closure of the ON/OFF window). With this definition, the time to failure requires a significant extrapolation from the average resistance trend of Figure 3.20 using a fitting procedure similar to the one adopted in Figure 3.21 in which the time to failure is plotted instead of $\tau_{1/2}$. For the un-doped devices, the 10 years retention goal occurs at ~ 170 °C, while despite the reduced activation energy, for the 4% Al-doped devices this goal is only slightly reduced to ~ 164 °C. Repeating the same procedure for the 7% Al-doped devices and excluding the failure bits, the 10 years retention goal is projected for a storage temperature of ~ 160 °C, only slightly lower than for the 4%-doped samples. However, this

data is affected by the strong requirement of excluding half of the memory cells.

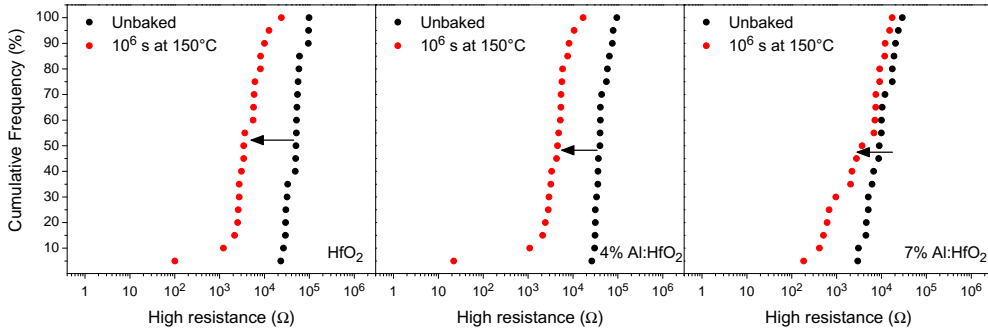


Figure 3.22: Comparison between the cumulative distribution of the initial stage and after baking at 150 °C for 10^6 s. For all the devices, including the 7%Al:HfO₂, the initial HRS distribution was obtained by a reset sweep at 2 V.

Sharp resistance transitions An equivalent picture of the retention degradation can be visualized by the evolution of the cumulative distribution of the cells after baking. In Figure 3.22, this distribution evolution is reported for all the device at 150 °C. With this representation, the gradual HRS lowering corresponds to a rigid shift of the distribution, while the failure bits are part of the distribution tail (higher slope), which deviates from the main log-normal trend.

The number of failure bits is strongly dependent on the doping concentration, while no major correlation was found with the baking temperature. In the un-doped devices, about 10% of the memory cells exhibit rapid failure, while in the 4% Al-doped devices this number increases to 15 – 20%. This allows to clearly distinguish between two different HRS decay regimes. Conversely, the highly doped devices with 7% concentration constitute a particular case, since about 50% of the cells lies in the distribution tail.

The bits in the tail of the device distribution exhibit a resistance decrease that often leads to a complete failure of the cell. For this reason, they constitute a much more severe issue in terms of data retention and deserve a separate investigation.

The time to failure can be evaluated for all the cells exhibiting rapid failure, resulting in the Weibull plot reported in Figure 3.23(a). Fitting the Weibull distribution results in the determination of a failure probability not constant in time. On the contrary, a rather low shape parameter $k = 0.19 \pm 0.01$ was found, comparatively lower than values reported for un-doped systems [30]. From the shape parameter, it can be derived a failure rate variable in time which follows the power law

$$\text{Failure rate} \propto t^{k-1} \approx t^{-0.8}$$

Since the failure probability rapidly decreases over time, this provides some direct evidence of the early decay of the analyzed cells. Additionally, from the extrapolation of the Weibull plot, after 10 years $\sim 84\%$ of the memory cells is expected to have completely lost its state by sudden transitions, proving that sudden resistance transitions constitute the main failure mechanism in highly Al-doped samples.

In section 3.4 it was shown that a high Al doping concentration brings a reduction of the HRS resistance. In order to build a comparison for the same initial state, the reset

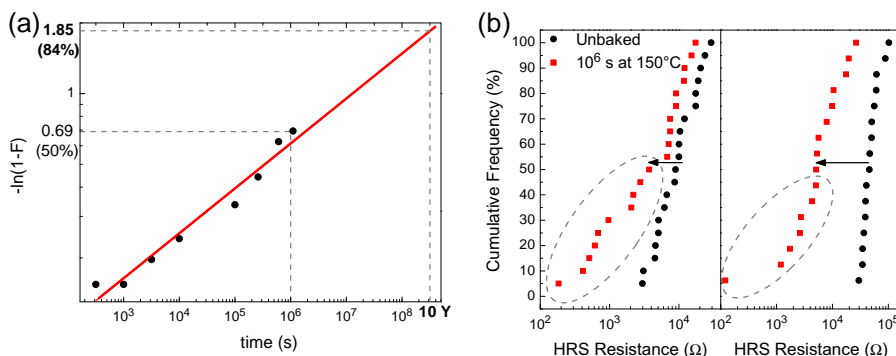


Figure 3.23: (a) Weibull distribution of the time to failure for the failure bits in 7% Al-doped HfO₂ memory cells. (b) Distribution of the HRS for the 7% Al:HfO₂ devices before and after baking at 150 °C for 10⁶ s. On the left, HRS obtained with a reset stop voltage of 2 V. On the right, same initial HRS of the HfO₂ and 4% Al-doped devices.

stop voltage was progressively increased until the same initial HRS of the HfO₂ and 4% Al-doped devices was met. The result is reported in Figure 3.23(b). Even if the initial HRS distribution exhibits a flat trend, the final HRS distribution obtained after baking at 150 °C for 10⁶ s shows the same resistance broadening over two decades and the same pronounced distribution tail of the retention analysis started from the lower HRS. Hence, the long distribution tail mostly depends on the doping concentration and is less dependent on the particular initial HRS.

A tentative explanation for the increase of the number of failure bits as a function of doping can be found in the clustering effect of oxygen vacancies around the Al impurities due to the preferential formation of the oxygen vacancies around the doping sites and of the positive vacancies attraction noticed in a few *ab initio* calculations [31, 32]. In case of high Al content, the clustering effect would cause a different filament structure and, after reset, a disconnection of the cluster of vacancies constituting the filament rather than the opening of a gap. Given the near proximity of the clusters, a near diffusion of a few vacancies would cause the restoration of the conduction path. Additionally, this effect would also explain the lower HRS obtained in 7% Al:HfO₂ devices.

Another possible explanation for the onset of the failure bits could be related to the formation of multiple conductive filaments during the forming procedure. During forming, once that one filament establishes connecting the two electrodes through the dielectric film, most off the current will pas through it and the other uncompleted branches will stop their evolution. Due to this mechanism, a single filament is likely to dominate the conduction. However, the high mobility of the oxygen vacancies induced by doping could facilitate the completion of the truncated filaments and the establishment of multiple conduction paths in parallel. This would account for the resistance level lower than the LRS that is sometimes reached by failure bits in Figure 3.19. Nonetheless, a full explanation of the phenomenon would require additional investigation.

A final remark should be devoted to the possibility of obtaining a complete reset of the memory cell, up to a resistance value similar to the pristine state. This possibility was anticipated in section 3.3.3 in association with peculiar switching characteristics.

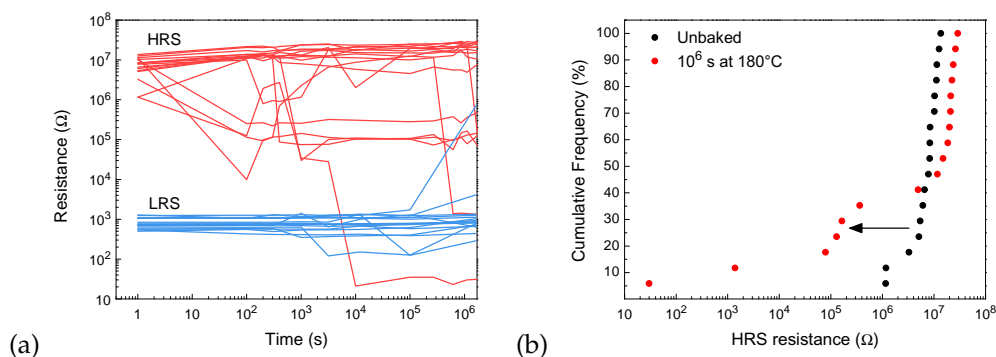


Figure 3.24: (a) HRS retention after a full reset at 3.5 V and relative LRS retention. (b) Cumulative probability of the initial state and after baking at 180 °C for 10^6 s of the HRS displayed in (a).

Figure 3.24 displays the retention characteristics for the HRS and LRS after full reset (stop voltage of 3.5 V) for un-doped HfO_2 devices for a baking temperature of 180 °C in order to accelerate the retention process. Interestingly, for this higher HRS even the un-doped cells exhibit a significant portion of failure bits: while the average trend surprisingly increases over time, nearly half of the cell population after 10^6 s lies in the distribution tail. This retention behavior could be an indication that a structural change occurred in the oxide, even if the resistance value is similar to the pristine state.

Another peculiar aspect is that the LRS is not anymore completely stable, with one cell that shows a resistance increase up to a value compatible with the HRS. The extreme reset condition presumably causes a complete deletion of the conduction path in a way that the subsequent set operation is also influenced, leading to a less stable filament.

In conclusion, doping HfO_2 -based resistive switching memory cells with aluminum allows the formation of more stable filaments and an improved reproducibility among different cells and between cycles. However, in particular for high Al concentration this comes at the cost of an enhanced diffusion of the oxygen species constituting the conductive filament, causing a faster loss of the state retention over time. For a 4% Al doping, this degradation is however limited and an optimum balance can be identified, while for the higher 7% concentration the not negligible fraction of failure bits causes a complete loss of the memory state. Finally, the choice of the switching parameters was also found to play a role in the retention loss process and should be taken into account when considering the retention performance.

3.5 Current fluctuations and random telegraph noise

When a small read voltage is applied to the RRAM devices, it is possible to notice a current fluctuation over time between two (or more) current levels. As an example, Figure 3.25(a) reports an I–V curve acquired after setting the cell to the HRS with a reset operation at 2 V. A fluctuation between two different current levels can be distinguished superimposed to the main trend, while the fluctuation amplitude ΔI clearly increases with the applied bias voltage. This current fluctuation is often referred to as random telegraph noise (RTN). However, RTN refers to a purely electronic phenomenon, while

in resistive switching memory cells also ionic phenomena can be identified and a distinction should be made [33–36].

In order to analyze this phenomenon, a constant bias of 500 mV was applied in Figures 3.25(b) and (c), while monitoring the current. Different sampling times and total measurement times were used in the two cases, but a similar current jump between current levels can be detected in both measurements. Moreover, in Figure 3.25(b) slow and fast events are clearly superposed in the same measurement. It is worth to notice that slower switching events cause larger current fluctuation, up to 20% in Figure 3.25(c), and their analysis is of great interest for a reliable reading of the memory state.

Repeating the same measurement after different cycles and in different cells, a similar multi-level behavior can be identified. However, the number of levels and their $\Delta I/I$ changes at each measurement. For a detailed statistical analysis of the phenomenon and a determination of the number of current states, in the literature analysis based on discrete hidden Markov chains as been applied [37]. However, when the complexity of the signal pattern is limited to a few states, a direct visual determination of the number of states can be achieved with time-lag plots like the one reported in Figure 3.25(d). In this plot, the $n + 1^{th}$ point is plotted as a function of the preceding n^{th} point, allowing to identify autocorrelated variables accumulating on the diagonal of the quadrant. In this representation, discrete current levels appear as separated accumulation spots on the diagonal.

Along with time-lag plots, useful information can be identified in the power spectral density (PSD) of the acquired time series (Figure 3.25(e)). Two main trends can be distinguished in the analyzed frequency range. At lower frequency, the $1/f$ trend prevails, while at higher frequency the main PSD follows the $1/f^2$ slope. In the classical RTN theory [38], the $1/f^2$ slope indicates a dominating trap, while the $1/f$ slope is the fingerprint of a large number of superposing traps [39]. The PSD plot is thus able to identify different regimes occurring at low and high frequency.

Aside from the general RTN trend of Figure 3.25, in some occasions also abrupt jumps can be detected with a $\Delta I/I$ over 70% even at 100 mV bias voltage (Figure 3.26(a)). These jumps are followed by large oscillations and by a different RTN signal after a new equilibrium has been reached. In the time-lag plot, these oscillations are outside of the diagonal and uncorrelated to the RTN points (Figure 3.26(b)). While it is possible that these transitions originate from non-equilibrium electric phenomena [36], ionic motion is also a likely candidate. Ionic reconfiguration could also be the responsible of a marked current drift sometimes observed for prolonged measurements and consistent with the resistance increase expected for positive polarities (Figure 3.26(c)). For long measurement times, even a low bias could perturb the memory cell and gradually change the memory state. The new signal configuration can be clearly distinguished in the time-lag plot as a well separated series of accumulation points with a lower current value along the normal (Figure 3.26(d)).

RTN in different high resistance states Increasing the reset stop voltage, the HRS resistance increases, while looking at the noise traces, a corresponding change from the $1/f$ to the $1/f^2$ regime can be observed. Comparing the noise spectra corresponding to the different states in Figure 3.27, only $1/f$ contributions are visible in the noise spectrum after reset at 1 V maximum voltage, indicating that a large number and continuous distribution of active traps is contributing to the noise spectrum. Increasing the reset voltage at 1.5 V, one single trap becomes predominant and a correspondent $1/f^2$ trend

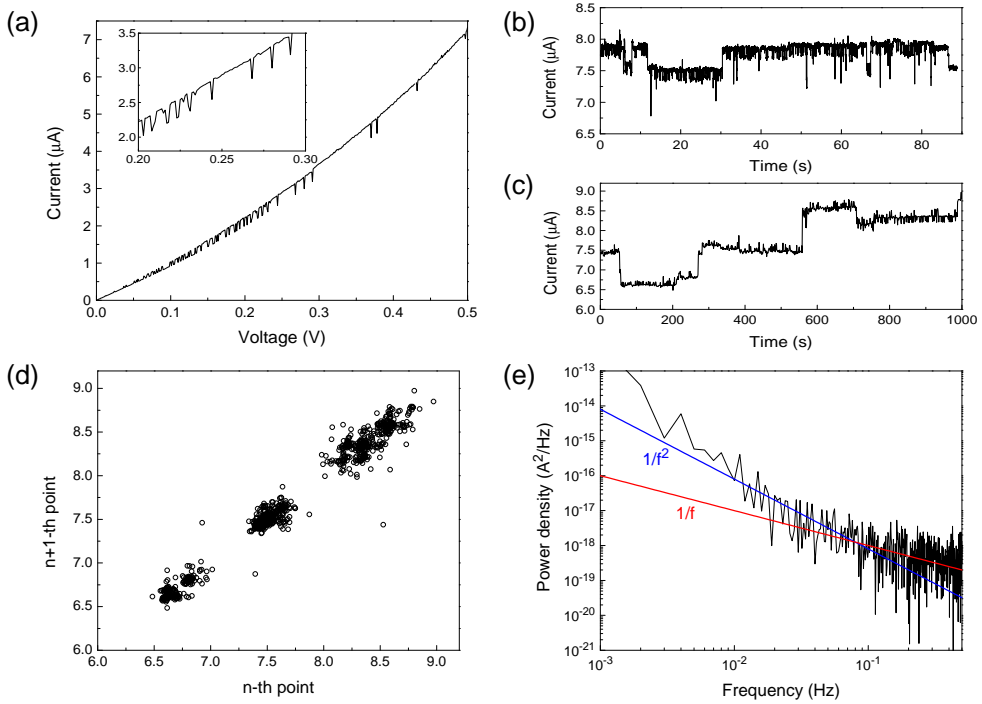


Figure 3.25: (a) Current–Voltage curve acquired after a reset at 2 V maximum voltage. In the inset, a magnification of the curve showing the two distinct current levels. (b) Current–Time series obtained with 500 mV bias and 10 ms sampling time. (c) Current–Time series obtained with 500 mV bias and 1 s sampling time. (d) Time–lag plot corresponding to time series (c). Power spectral density extracted from time series (c).

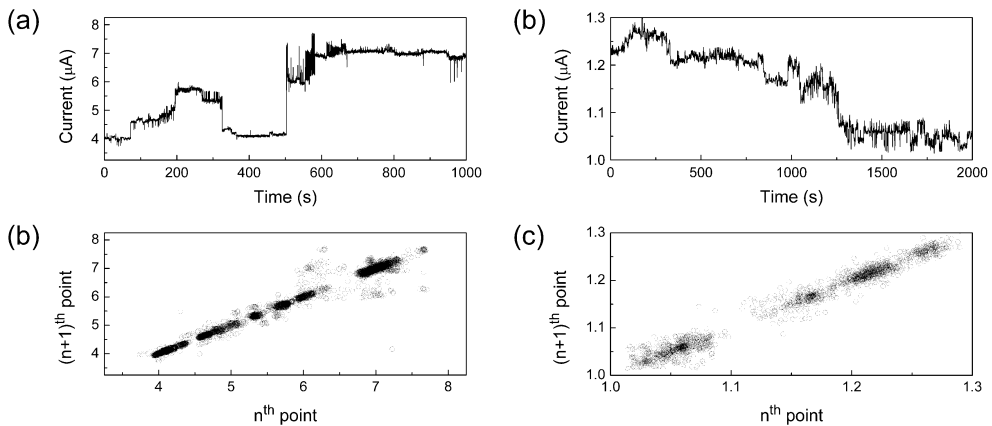


Figure 3.26: Anomalous noise traces and relative time–lag plots (bias 100 mV; sampling time 1 s). (a,b) time series displaying a current jump with $\Delta I/I$ over 70%; (c,d) Time series displaying a current drift.

emerges. This change in PSD trend could be related to an incomplete filament dissolution with a 1 V reset, while the reestablishment of a dielectric gap is expected for higher reset voltages, where a limited number of traps exists. Indeed, the noise trace observed upon 1 V is qualitatively similar to the LRS noise traces [40].

After the high voltage 3 V reset, also a clear $1/f$ contribution can be distinguished starting from 0.1 Hz, which was not clearly detectable with a lower reset voltage. This reappearance of a $1/f$ contribution with high voltage reset was previously explained by the increased number of active traps in the thicker dielectric barrier obtained with higher reset voltages [37, 41, 42].

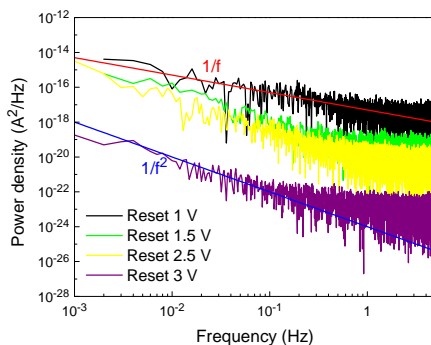


Figure 3.27: Current power spectral densities of noise measurements performed after reset at different voltages in a HfO₂-based device.

RTN in the low resistance state Considering the LRS, for short observation times (< 100 s), the noise trace does not display any relevant RTN feature and the noise spectrum closely follows the $1/f$ trend, while the time-lag plot does not indicate any relevant correlation between adjacent data (Figure 3.28(a–c)). The reported data suggest that a continuum of active traps is active in the region of the conductive filament, while no active trap is dominating at this time scale. Nonetheless, the fact that a white noise spectrum appears only at frequencies above 10 Hz means that capture/emission processes are actually taking place in the cells [39].

Prolonging the measurement time up to 1000 s, an RTN-like noise trace was detected in some occasions (Figure 3.28(d–f)). The PSD correspondent to this trace clearly displays a $1/f^2$ slope up to 1 Hz, while the three distinct current levels are also distinguishable as three main spots along the diagonal in the time-lag plot. The explanation of this RTN signal with $\Delta I/I$ limited to less than 1 % could be explained by charging and discharging of electron traps located in the near vicinity of the conductive filament, as reported in ref. [43, 44].

RTN in Al-doped devices During the reset process, the conductive filament is partially oxidized and a dielectric barrier is created along the conduction path, highly enhancing the device resistance. While the effective barrier length depends on the maximum reset voltage, the characteristics of the barrier layer and the amount of traps available for trap-assisted-tunneling conduction through this barrier can also determine the HRS. In sections 3.3.1 and 3.4.2 the effect of doping the HfO₂ films with Al was discussed, and a

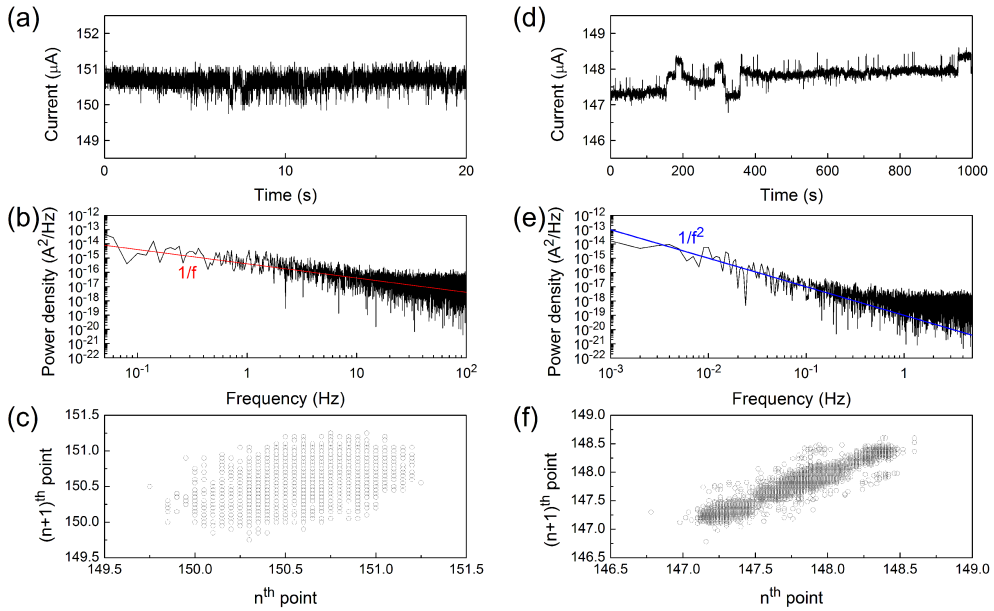


Figure 3.28: Noise traces and relative PSD and time-lag plots for the LRS. In (a–c), a bias voltage of 100 mV and a sampling time of 2 ms was used. In (d–f) a bias voltage of 100 mV and a sampling time of 1 s was applied.

reduced HRS was reported for high Al concentration. By means of RTN measurements, it is possible to determine the amount of effective active traps in the oxidized part of the filament as a function of Al doping, extracting information about the residual defects in this layer.

In Figure 3.29, the noise traces for the 4% Al:HfO₂ (a–c) and 7% Al:HfO₂ (d–f) doped devices highlight an increased number of current levels and thus of active charge traps contextually to increase of the doping concentration. The noise traces for short measurement times evidence the same trend, but a high level of $1/f$ and white noise prevents to reliably distinguish the distinct current levels. For longer time scales, the presence of a high number of different current levels becomes apparent, and in time-lag plots the current points are distributed over the diagonal evidencing high correlation, however the signal appears as a superimposition of RTN due to the activity of a high number of different traps, which becomes a continuum of spots along the diagonal for the highly doped 7% Al:HfO₂ device.

Because of the high number of superimposed RTN signals, the best way to compare the different samples is by the PSD plots of Figure 3.30. In the un-doped HfO₂ device a clear transition from the $1/f$ to the $1/f^2$ regime can be detected around ~ 0.1 Hz. For 4% Al doping, the higher number of active traps enhances the $1/f$ contribution to the spectrum and shifts this transition to lower frequency. In this sample, a $1/f^2$ trend can be distinguished below ~ 0.05 Hz. In the highly doped sample, the $1/f^2$ slope is barely detectable, since the $1/f$ regime prevails down to ~ 0.01 Hz and measurements longer than 1000 s would be required to clearly go beyond the $1/f$ noise.

In conclusion, doping the HfO₂ film with Al atoms highly enhances the number of

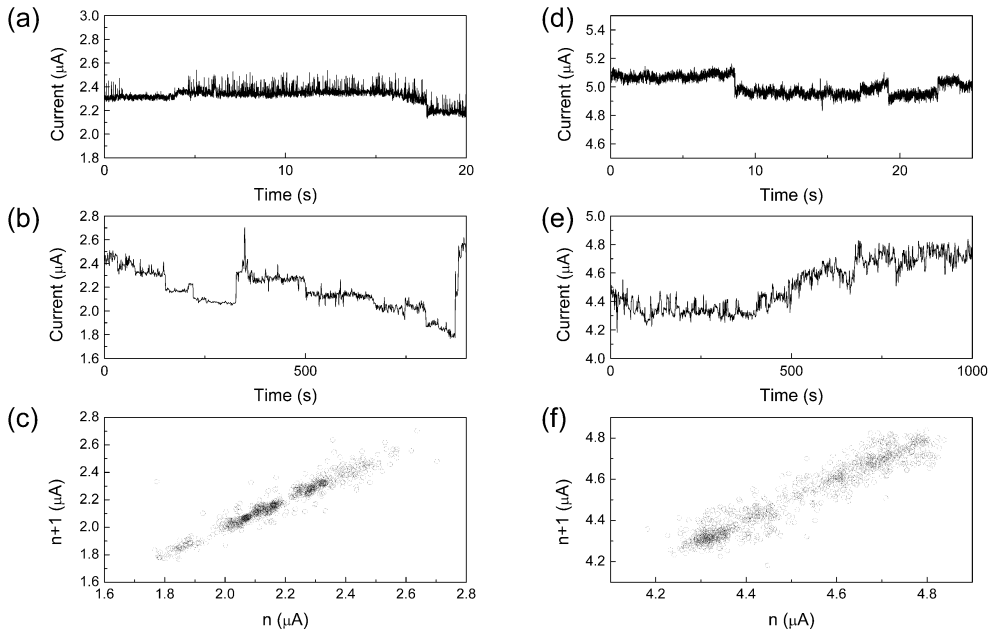


Figure 3.29: Noise traces and relative time-lag plots after reset at 2 V for a 4% Al:HfO₂ device (a–c) and for a 7% Al:HfO₂ device (d–f). In both cases, a bias voltage of 100 mV and a sampling time of 1 s were applied.

active traps in the barrier dielectric region created along the conduction path upon reset in the memory cell. In this respect, oxygen vacancies are considered main candidates for electron trapping processes in HfO₂ and it is worth noting that their formation energy highly reduces along the Al doping sites. The reported increase of superposed RTN traces in the HRS could be explained by a higher number of residual oxygen vacancies in the gap region in the doped samples.

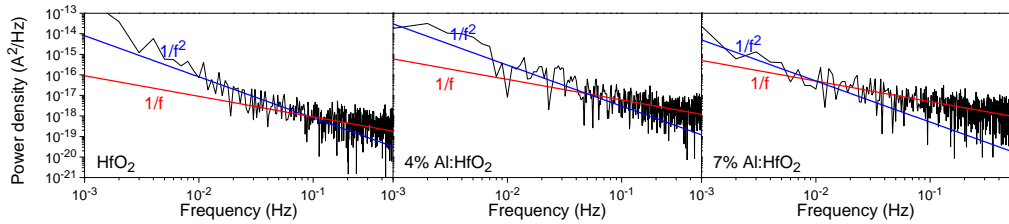


Figure 3.30: Current power spectral densities for the three analyzed samples derived from noise traces with 100 mV bias voltage of and 1 s sampling time.

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Block copolymer self-assembly for lithographic applications

4.1 Introduction

Over the past decades, the sustained development of microelectronics was made possible by a continued scaling of the device dimension. A sustained innovation pushed the limit of standard photolithography technologies to its edge. However, below 40 nm half pitch the now commonly employed 193 nm immersion lithography finds a resolution limit due to diffraction [1]. Smaller features can be printed using additional process steps to halve the pitch (pattern doubling) or by doing more than one exposure per level to enhance the pattern resolution (multiple patterns). However, these additional steps dramatically increase the process complexity and rise lithography costs [2].

Alternative techniques were proposed to continue the device scaling. Viable ways are a further reduction of the light wavelength down to the extreme UV or even X-ray regime or to use e-beam lithography to directly pattern the resist with an electron beam. The development of these approaches could guarantee a resolution below 10 nm, however they are affected by high complexity, elevated cost, or low throughput [1].

The promise of self-organizing materials is to allow a relatively simple and cost-effective construction of regular patterns without relying on sophisticated tooling to control the dimensions of the smallest features in a device, but rather directly controlling the properties of the applied molecules. Block copolymers offer a rich variety of periodic nanoscale patterns with long-range order up to the μ scale, which can constitute the building blocks for more complex patterns. Moreover, BCP lithography is now considered the only readily available technology able to reach 8 nm critical dimension (CD, equal to half pitch) for the long-term lithographic challenge, and BCP assembling in domains of only 5 nm was recently reported [3, 4].

BCP-defined features can be self-assembled on top of pre-defined guiding substrates for pattern orientation and registration with nm-size accuracy in what is commonly called *templated self-assembly* (TSA) [5]. The combination of standard lithographic techniques with BCP lithography allows to reach very low features size and pitch still maintaining compatibility with current processing tools.

Before BCP self-assembly can be adopted as a standard patterning technology, the stringent requirements imposed by the microelectronic processes should be met. One of the challenges is to reach the target level of less than 1 defect/cm² necessary for the introduction of the technology into production. This imposes a stringent requirement on the molecular weight distribution of polymers (a polydispersity index as close to

unity as possible is required), on the guiding pattern, and on the annealing process [6]. Another requisite for practical application of BCP lithography is the development of design routines to apply the simple periodic self-assembled patterns in arbitrary chip designs [7, 8].

Besides these issues, other technological problems need to be solved in practical applications. PS-*b*-PMMA was subject of intense research in the past few years and is currently the diblock copolymer with the most demonstrated applicability for semiconductor patterning. However, the pattern transfer of this all-organic polymer typically shows low etch selectivity. Therefore, additional strategies are necessary for transferring the pattern into deep features, such as the intermediate transfer into robust hard masks or the selective incorporation of chemical precursors into one of the polymer blocks [9, 10]. The low driving force parameter for self-assembly typical of this polymer additionally prevents features size below 12 nm, and new polymers are actively investigated [11].

While significant questions remain about the optimum material and the best process, as resolution is pushed to the absolute limits, the lithographic paradigm is increasingly shifting from a "top-down" to a "bottom-up" approach.

4.2 Block copolymer self-assembly

Block copolymers are macromolecules composed of two or more chemically distinct block units covalently bonded together to form a single polymer chain. Each single block is formed by the repetition of a particular monomer, forming a homopolymer chain. Different architectures can be fabricated by living linear polymerization techniques, adding the different block units in $(A - B)_n$ type architectures forming diblock ($n = 1$), triblock ($n = 2$) or even starblock copolymer architectures ($n > 3$), while more complicated and ramified block copolymers are also possible.

The peculiarity of block copolymers is that under particular conditions, when the constituent blocks are chemically immiscible, they can autonomously segregate in spatially separated phases with dimension determined by the size of the polymer blocks. While a mixture of the same type of homopolymer chains would lead to a macroscopic phase separation, the covalent bond between the blocks allows the separation in phases of only deca-nm size. After phase separation, the polymer chains remain amorphous and are characterized by fluid-like disorder on the molecular scale, while at longer length scales the regular repetition of the nm-scale phases assures a high degree of order [12, 13].

The phase separation is promoted when enough kinetic energy is given to the polymer chains to move and reorganize, which happens above the glass transition temperature. However, the phase separation is thermodynamically and entropically favored only when the chemical force repulsing the distinct blocks is high enough. In this situation, the minimum free energy configuration is reached by minimizing the interaction energy, which favors the phase segregation in order to minimize the monomers contact. The nanophase separation happens at the expense of translation and configurational entropy for the polymer chains by local compositional ordering.

The experimentally relevant parameters that dictate the phase separation in bulk block copolymers are:

N overall degree of polymerization, which corresponds to the number of monomers in the polymer chain;

f_A fraction of the A component given by N_A/N , where N_A is the number of monomers A in the polymer chain;

χ_{AB} Flory–Huggins interaction parameter between the A and B blocks.

The first two parameters are compositional constraints that can be experimentally controlled during polymerization and are essentially entropic factors that determine the translational and configurational energy of the polymer chains.

On the contrary, the χ_{AB} parameter is largely an enthalpic contribution and represent the cost in free energy for the contact between the A and B monomers and is thus principally dependent on the selection of the two polymer blocks. For the particular case of diblock copolymer ($n = 1$) used in the present work, the interaction parameter has the following dependence [13]

$$\chi_{AB} = \frac{Z}{k_B T} \left[\varepsilon_{AB} - \frac{1}{2} (\varepsilon_{AA} + \varepsilon_{BB}) \right]$$

with Z the number of nearest neighbor monomers, k_B the Boltzman constant, and ε indicates the interaction energy per monomer between the AA , BB , and AB couples. Note that $Z/k_B > 0$ and the sign of χ_{AB} is entirely determined by the specific interaction energies per monomer. When $\chi_{AB} > 0$ the overall interaction between the A and B monomers is repulsive, while when $\chi_{AB} < 0$ the attractive interaction favors a mixing between the A and B monomers. Note in addition that χ_{AB} is proportional to T^{-1} . At typical operating temperatures with dissimilar A and B blocks with no specific interaction, χ_{AB} is positive but small compared with unity [14].

At first order, the entropic contributions to the to the free energy per chain deriving from the stretching of the different domains covalently bonded together (elastic free energy) can be approximated by the Hook law [15]

$$F_{domain}/k_B T \propto \frac{L_0^2}{N a^2}$$

where L_0 is the domain period and a is the characteristic segment length which depends on the local structure of the polymer chain.

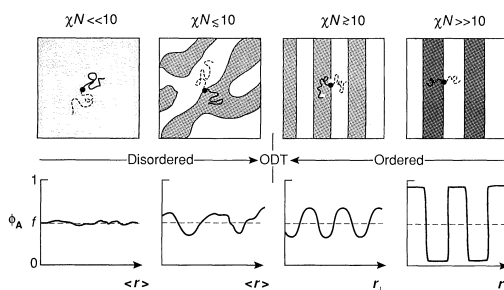


Figure 4.1: Disordered and ordered BCP phases for the different values of χN [13].

Since the entropic contributions to the free energy density scale as N^{-1} while the enthalpic factors are mainly represented by χ , at equilibrium the minimum free energy configuration is determined by the product χN .

Figure 4.1 displays a schematic representation of the disordered and ordered BCP phases for the different values of χN . When $\chi N \ll 10$ the entropic factors dominate and a spacial homogeneity is obtained, without any phase separation (Figure 4.1). In this phase the block copolymer is disordered and $A - B$ segments interaction is sufficiently weak to leave the polymer chains unperturbed. The phase transition between ordered and disordered states (ODT) occurs for $\chi N \sim 10$, when entropic factors are balanced by energetic factors. In the proximity of the ODT transition, the $A - B$ interaction is still weak enough to leave the polymer chains unperturbed in a melt-like fashion, and the composition profile is characterized by a sinusoidal distribution with period scaling as $N^{1/2}$. This regime is called *weak segregation limit* (WSL). The complete phase separation occurs when $\chi N \gg 10$, in a regime called *strong segregation limit* (SSL). In the SSL the contact between the A and B blocks is minimized and the chain stretching is increased, leaving well separated nanodomains. Minimization of the energetic factors gives narrow and localized interfacial regions with width scaling as $a\chi^{-1/2}$, while the domain period scales as $aN^{2/3}\chi^{1/6}$ due to the competition between $A - B$ contact area minimization and entropic penalty for extended chain stretching [15–17].

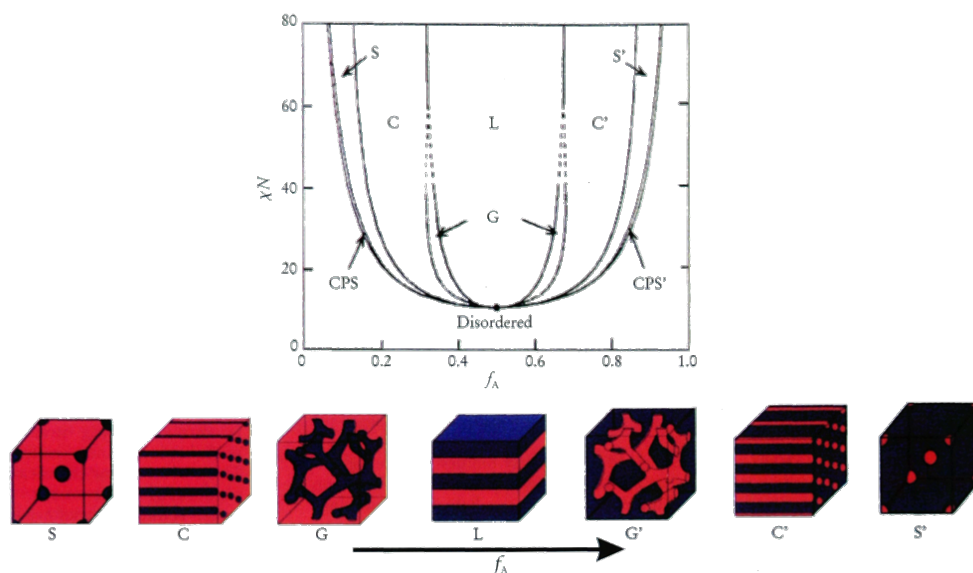


Figure 4.2: Equilibrium phase diagram calculated by self-consistent mean field theory and relative morphologies for di-block copolymers [18].

Phase diagram The equilibrium phase diagram for diblock copolymers can be calculated by self-consistent mean field theories [17, 19] and experimentally verified by TEM, SEM, and small angle X-Ray scattering techniques. The morphologies available with di-block copolymers in the SSL regime are fully determined by the relative fraction of the monomer units (f_A). As shown in Figure 4.2, increasing progressively f_A sphere-type domains of block A inside the B matrix are first encountered; then cylinders of A in B , gyroid structure (also called ordered continuous double diamond) and lamellar morphology can be achieved. Increasing f_A over 0.5 results in the inversed morphologies,

i.e. gyroid, cylinders and spheres of block B inside the A matrix [20].

Thin films The above discussion about BCP thermodynamics and phase separation is based on bulk BCP. In these systems, the nucleation of the ordered phase originates from random positions in the bulk and gives rise to grains of ordered domains oriented randomly with respect to each other. Conversely, in thin BCP films, when the film thickness t is at least comparable to L_0 in size, the effects of confinement and surface or interfacial energetics on microphase separation should be considered, as well as the interplay between the copolymer's characteristic length scale L_0 and the film thickness t . As a result of surface and interfacial energy minimization, BCP thin films are often characterized by highly oriented domains throughout the film plane [21].

The evolution of the BCP morphology in thin films develops from the polymer/substrate and upper surface/polymer boundary conditions and is dictated by the most energetically compatible block with respect to each interface. If the same block preferentially wets each interface, boundary energetics is symmetric. On the contrary, if a different block is present at each surface, the BCP wetting is termed anti-symmetric. For symmetric wetting the BCP film exhibits a stable morphology throughout the surface when $t = nL_0$, with n an integer and positive number, while for anti-symmetric BCP a stable morphology is found for $t = (n + 1/2)L_0$. If there is no commensurability between the film thickness and the BCP characteristic length scale, the film will not uniformly cover the entire substrate and islands or holes will be formed [22].

While the domain orientation in thin films is dominated by the preferential wetting of the given BCP blocks with respect to the boundary surfaces, the most energetically compatible block depends upon the energetic and chemical nature of the surface, which is determined by the magnitude and type of interaction (attraction or repulsion) these boundaries have with each of the block species. The picture is further complicated by the interplay with the film thickness parameter t and by the specific evolution of each BCP morphology, with primarily depends on the f_A parameter as previously discussed.

For the study of the morphological shifts as a function of film thickness, theoretical approaches are based on surface energetics and geometrical considerations [23] or on computational calculations [24], while experimental investigations based on mass spectrometry (tof-SIMS) and neutron reflectivity profiles were reported [25, 26].

In order to obtain a domain orientation perpendicular to the surface in diblock copolymer films, neutral boundary conditions are necessary [27]. To remove any preferential wetting of one of the two polymer blocks with respect to the substrate, for the PS-*b*-PMMA BCP a random copolymer (RCP) functional layer was demonstrated as a viable solution [28]. The RCP contains styrene and methyl methacrylate monomers randomly arranged along the polymer chain and it can be end-grafted to the substrate by a proper end-chain functional group, avoiding an RCP intermixing with the above BCP film. By tailoring the styrene and methyl methacrylate composition, it is possible to balance the interactions between the BCP segments and the interface, obtaining highly perpendicularly oriented cylinders and lamellae [29–31].

Templated self-assembly Templated self-assembly (TSA) is also referred as directed self-assembly, since it is a method to externally direct the self separation so that instead of a random nucleation, a pattern registration and alignment of the BCP features is obtained. As previously discussed, the energy minimization of the BCP blocks with respect

to surfaces and interfaces can drive the BCP self-assembly process by adding boundary conditions to the phase separation process. Indeed, aligned lamellar patterns have been obtained on topologically-defined substrates, as well as hexagonally packed cylinders and square sphere arrays aligned along the desired direction. For more complicated designs, lamellar arrays were bended at defined angles and bended nanowires were obtained [5, 32].

Templating methods can be divided in two broad categories, graphoepitaxy and chemoepitaxy. The former is based on the definition of a physical topography to guide the BCP phase separation as a topological constraint, while the latter consists in chemically distinct regions of the surface with different affinities for the polymer blocks. The physical dimension of the guiding pattern should be comparable or larger than the BCP periodicity, while for very wide templates the guiding forces are overcome by entropic factors and the ordering is lost. Considering that practically feasible BCP M_w lie between 20 and 2000 Kg mol⁻¹ and have domains with periodicity between 10 and 200 nm, suitable techniques should be adopted to pre-pattern the substrate at comparable or larger length scales. Typical patterning techniques are direct writing by electron beam lithography, nanoimprint lithography or advanced optical lithography. However, TSA makes practically feasible patterning and positioning small features below 10 nm starting from templates up to a few μm wide, highly relaxing the requests on the lithography technology even when small features are needed. In addition, TSA can extend the natural length scale at which the BCP periodicity is conserved (correlation length) [11, 33].

In wide templates, commensurability with the BCP periodicity is not necessary since the BCP period can be slightly stretched to fit the template. However, when the template dimension approaches the BCP periodicity, for defect-free arrays, laws similar to the one expressed for thin films should be applied, with template widths corresponding to nL_0 or $(n + 1/2)L_0$ depending on the specific boundary conditions.

Templating patterns can have different 1D, 2D, or even 3D morphologies. For the alignment of periodic lamellae, usually long trenches allow the alignment along or perpendicularly to the boundary edges, depending on the specific affinity. Circular cavities can result in concentric lamellae, while pits disposed with periodicity equal to the BCP can be used to align and bend the lamellae. For cylindrical and square BCP arrays, all the aforementioned guiding patterns have been applied. With trench width equal to L_0 , BCP confine to a single line of cylinders or spheres. With wider templates, BCP self-organizes in ordered arrays with high periodicity (cit. needed).

One of the challenges of TSA is reducing the placing error down to a value compatible with microelectronic processes. The main sources of loss of accuracy come from the edge roughness of the template and from fluctuations of the BCP periodicity. The fabrication of BCP molecules with polydispersity close to unity can reduce the domain size fluctuation. However, thermodynamic considerations also come into play and the BCP annealing conditions should be carefully adjusted to maximize the placement accuracy.

The combination of pre-patterned substrates by top-down lithography with the bottom-up BCP self-assembly is a typical example of synergistic integration discussed in chapter 2, and can potentially add the benefit of custom definition and accurate positioning of the defined features typical of top-down technologies with the extremely high density, scalability, and low cost of bottom-up BCP self-assembly.

PS-*b*-PMMA diblock copolymer The BCP adopted in the present work is PS-*b*-PMMA. This all-organic diblock copolymer is one of the mostly employed BCP and presents

some optimal properties. In particular, PMMA nanodomains can be easily removed using ultraviolet exposure and acetic acid etch, leaving a nanoporous PS film that can be used as soft mask for lithographic processes [34]. Moreover, PS-*b*-PMMA can be self-assembled by means of an annealing step, avoiding the use of more delicate processes like solvent annealing. Self-assembly by rapid thermal annealing process was demonstrated [35], which reduces the processing time to a few minutes. More recently, also laser induced millisecond thermal annealing was used to induce the BCP phase separation, further decreasing the processing time [36]. However, it should be noted that for laser annealing the overall processing time depends on the dimension of both wafer and laser beam, since the laser spot should be scanned in a raster-type pattern over the entire wafer surface.

Lamellar morphology is achieved with the usual 0.5 PS/PMMA ratio, while the cylindrical morphology can be obtained with a PS volume fraction of ~ 0.7 . The variation of the chain length (or, in an equivalent way, of the BCP molecular weight) allows to finely tune domains size and spacing. For the cylindrical morphology, the minimum molecular weight with a χN parameter above 15, which allows the BCP self-assembling, is 39 Kg mol⁻¹, and diameters down to 12 nm with a lattice spacing of 24 nm can be obtained [37, 38].

For PS-*b*-PMMA on SiO₂ substrates and more generally on hydrophilic oxide surfaces, the PMMA block exhibits a preferential surface affinity, while the non-polar PS segment preferentially assembles at the polymer/air interface. However, for phase separation performed under vacuum or in inert ambient, above 225 °C the interfacial interactions at the free surface are balanced and the addition of a RCP layer to neutralize the surface permits the self-assembly of cylindrical and lamellar morphology with domains perpendicular to the substrate.

The analysis of the SiO₂ surface neutralization by RCP with low molecular weights (down to 1.7 Kg mol⁻¹) unveiled that the perpendicular morphology and thus an effective surface neutralization can be always achieved for an RCP thickness above 5 nm, for which the RCP completely screens the substrate surface. However, the study evidences the possibility to promote the perpendicular orientation of PMMA cylinder also for ultrathin RCP films of only 2 nm if a sufficiently low molecular weight is used [39].

In thin films, a balanced interfacial interactions can promote perpendicular domains only to a limited extent, and an additional constraint comes from the BCP film thickness. An investigation of the proper window as a function of the composition of P(*S-r*-MMA) films anchored to the substrate revealed the BCP thickness window within which a domain orientation normal to the film surface persists. The optimal RCP compositions were found to be around 0.64 and 0.55 PS mole fraction for cylindrical and lamellar domains, respectively [40]. In the study, the maximum achievable BCP thickness was 42 nm for lamellae and 39 nm for cylinders. A recent study however extends this range to a thicknesses of 200 nm for cylinders. This unexpected enhancement was motivated by the adoption of high temperatures and short processing times, possible with the adoption of the RTP technique to promote the phase separation [41].

4.2.1 Applications

The possible applications of self-assembled block copolymers can be manifold in different fields of nanotechnology. For lithographic applications in electronics, the BCP self-assembly can be used in combination with traditional photolithography to overcome the limits that arise below 40 nm, decreasing features size and pitch [1, 42]. Indeed,

BCP can allow the multiplication and rectification of an existing pattern, also healing resist defects and reducing feature size variation of ill-defined resist patterns [43, 44]. TSA of High- χ BCP thin films can generate regular arrays of sub-10 nm scale features with good positional and orientational accuracy. Grating and holes/pits patterns were demonstrated, which can constitute the building blocks for more complex structures. Moreover, the adoption of Si-containing BCP allowed to simplify the pattern transfer process and reach high aspect ratio structures [33, 45–47].

From the practical viewpoint, BCP found prototypical applications for the aggressive scaling of line–space patterns for FinFET and circuit fabrication with critical dimensions defined by self-assembly [48, 49] and for contact hole patterning in integrated circuits for technology nodes beyond 14 nm [50]. Besides logic circuit implementations, BCP were exploited in electronics for the patterning of capacitors with high accumulation capacitance for on-chip power supply decoupling [51, 52].

Numerous recent works also focus on the employment of the BCP technology in memory applications. Arrays of metal nanodots formed by BCP templates were proposed for charge-trap memories with ultrawide memory window in order to expand the number of distinct levels in a single cell and reduce the variability [53, 54]. The possibility to build ordered arrays of metal nanoparticles with densities hardly achievable with other techniques can be also exploited for the fabrication of bit-patterned magnetic recording media [55]. The nm-scale dimension of the magnetic dots and their close vicinity allows to overcome the superparamagnetic limit that arises for small recording bits in continuous magnetic films, permitting very high recording densities [56–58].

In the contest of phase change memory (PCM) devices, the reduction of the contact area between the heater electrode and the phase change material achieved by BCP-formed SiO_x nanostructures allowed a 20-fold reduction of the switching power [59]. Alternatively, a host–guest approach with two different diblock copolymers was applied for the positioning of spherical domains at the center of cylindrical ones, resulting in a template of regularly arranged ring-shaped nanostructures. The pattern transfer of the nanorings to the phase change material allowed to build prototypes of highly scaled PCM devices with highly reduced switching volume. The individual devices were tested through contact atomic force microscopy, demonstrating a low switching current in the μA range [60].

Various approaches were used for the application of BCP-formed patterns to resistive switching memories. Yeon Sik Jung and co-workers applied the same methodology previously described for contact area reduction in PCM memories for the nanostructuring of the contact between the top electrode and the switching layer in unipolar NiO resistive switching devices. A Si-containing block copolymer was self-assembled to produce insulating SiO_x nanodots above the NiO layer, localizing the top electrode contact at specific locations. This allowed to confine the electric field and to achieve a more reliable and reproducible control of the conductive filament growth and dissolution. The result was a substantial reduction of the operating voltages fluctuation as well as of the HRS/LRS ratio variation [61].

Another approach for RRAM device fabricated using diblock copolymer self-assembly lithography consists in scaling down a pre-patterned region by placing inside of it a single self-assembled cylindrical domain. In a work by Wu et al, this methodology allowed holes of 20 nm to be patterned. The ALD conformal deposition method was afterward used to deposit the switching oxide and the top electrode inside the patterned holes, obtaining memory devices less than 12 nm in lateral size [62].

Finally, a Si-containing diblock copolymer was used to directly form ordered arrays of SiO_x -based resistive switching devices on metal and graphene electrodes, avoiding a pattern transfer process. The self-assembled SiO_x nanostructures were contacted by atomic force microscopy and showed unipolar-type switching of the resistance. This method allowed a very high device density (~ 0.5 Tbit inch $^{-2}$) without using high-cost lithography techniques or pattern-transfer methods [63].

Besides applications in electronics, the dimension of the BCP self-assembled templates at the molecular length scale finds practical employments for the creation of membranes for molecular sorting, sensing, drug delivery, and filtration. Highly porous free-standing silicon membranes were constructed by transfer of the self-assembled pattern to the Si layer followed by backside etching of a SOI wafer [64]. The fabrication of a membrane with an asymmetric film geometry provided both high selectivity and high flux for virus separation. It was composed of a thin film prepared from a block copolymer template with cylindrical pores of 15 nm diameter with a narrow pore size distribution on top of a conventional support membrane that provided the necessary mechanical strength [65]. The advantage given by BCP templates is that the narrow pore size distribution permits an efficient filtering of viruses, at the same time allowing smaller proteins to overcome the selective barrier. The implementation of these innovative membranes could pave the way to new types of more efficient blood filtering systems, highly reducing the risk of viral infections.

4.3 Periodic array of metal nanoparticles on the HfO_2 surface

The purpose of the experimental work presented in this chapter is to find an experimental procedure for the fabrication of periodic arrays of metal nanoparticles with high control over the particles size and density. As previously discussed, BCP can self-assemble in regular nanoscale domains upon phase separation. Polymeric templates based on BCP self-assembly are an optimal tool for the formation of ordered arrays of metal nanoparticles (NPs) by means of pattern transfer processes. This lithographic technology can enable a broad range of applications. As an example, by reducing the NPs size, the surface to volume ratio is increased, highly enhancing the catalytic activity of noble metal NPs [66, 67]. Another example can be found in the plasmon-enhanced luminescence encountered in nanoscale arrays of metal NPs, which offer the possibility to concentrate and manipulate light [68–70]. Consequent applications range from light emitting devices and photovoltaics [71] to advanced sensing. In the latter case, the plasmonic properties of metallic NPs enable the surface-enhanced Raman scattering technique [72], which finds notable applications in the characterization of small molecules. Localized surface plasmon resonance sensing and second harmonic generation techniques are other possibilities enabled by metal NPs [73].

Aside to plasmon-activated techniques, noble metal NPs can also offer an enhanced corrosion resistance to the etching processes and can be exploited for the pattern transfer of high aspect ratio features by reactive ion etching [74, 75].

In this work, the creation of periodic arrays of metal NPs by block copolymer self-assembled templates was used for the definition of nm-sized electrodes in resistive switching memory devices. In addition to a device size down to 12 nm, the applied method allows to highly reduce the distance between the devices beyond the limits imposed by other lithographic technologies, allowing to reach an unprecedented density of 1.5×10^{11} cm $^{-2}$. In this way, it was possible to explore the extreme high density scalability limit

for resistive switching memory cells, as will be discussed in detail in the next chapter.

The main requirement that should be satisfied by a lithographic technology is a reproducible size and a controlled particles dispersion. Indeed, for the particular choice of the block copolymer used (PS-*b*-PMMA), the size dispersion for the metal NPs achieved was demonstrated to be well reproducible and around 2.5 nm, while the particles diameters could be easily controlled down to 12 nm by the choice of the molecular weight. Probably the main advantage of this technology is however the very high density achieved combined with the relatively low fabrication cost.

Another notable property is that the produced NPs are not placed disorderly over the surface. In perspective, defect-free polymeric templates can be obtained by combining block copolymer self-assembly with pre-patterned substrates, allowing a very long-range order.

Finally, the broadest range of applications can be achieved only if the technology can be extended to virtually any substrate of choice [76]. While the great majority of BCP applications reported involves Si and SiO₂ substrates, in this work the applicability was extended to HfO₂-based substrates, proving its feasibility.

4.3.1 HfO₂ Surface neutralization

The creation of polymeric templates suitable for pattern transfer requires the formation of domains with perpendicular orientation. In thin films, the orientation of the domains is governed by energy minimization at the interfaces with the bottom surface and with the air at the top. In the case of the PS-*b*-PMMA BCP, at temperatures higher than ~225 °C the free surface at the top becomes neutral [77]. However, the removal of any preferential wetting of one of the two polymeric blocks with respect to the bottom surface is required in order to achieve a perpendicular domains orientation (Figure 4.3). On Si-based substrates, a neutralization layer formed by a random copolymer (RCP) with random styrene and methyl methacrylate positions in the polymeric chain is a viable method to achieve surface neutralization [28]. In the present work, we investigated the surface neutralization of ALD-deposited HfO₂ and Al:HfO₂ films by a P(S-*r*-MMA) RCP.

A brush layer of hydroxyl-terminated P(S-*r*-MMA) RCP with 0.62 styrene fraction, 14.5 kg mol⁻¹ molecular weight (M_w) and polydispersity index (PDI) 1.25 was deposited on the HfO₂ surface by spinning a solution of 18 mg in 2 mL of toluene at 3000 rpm for 30 s. The samples were then thermally treated in an RTP machine for 10 min at different temperatures from 230 to 310 °C in N₂ atmosphere to promote the “grafting to” surface reaction between the hydroxyl groups at the end of the chain of the functional copolymer with the -OH groups present on the HfO₂ substrate. In this way, a self-assembled monolayer chemically grafted at the substrate can be obtained. The non-grafted polymer chains were afterward removed by washing in toluene for 5 min, and the grafted substrate was dried under N₂ flow.

The grafted RCP thickness evolution as a function of the annealing temperature is illustrated in Figure 4.4. At temperatures lower than 300 °C, the thickness monotonously increases with temperature, meaning that a higher kinetic energy is required for the RCP chains to find available -OH sites on the surface. At 310 °C, the saturation thickness is reached, indicating that all the available -OH sites are grafted to RCP end-chains.

A straightforward method to ascertain the HfO₂ effective surface neutralization is to self-assemble a layer of the required BCP on the functionalized surface, investigating

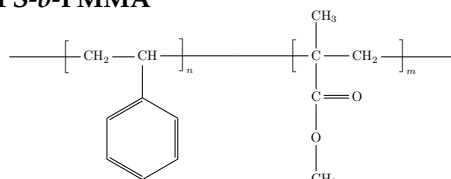
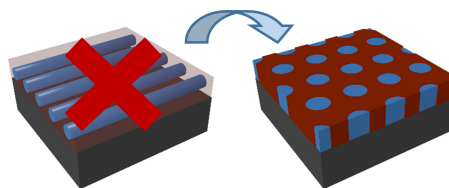
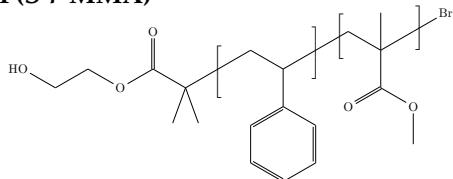
PS-*b*-PMMA**P(S-*r*-MMA)**

Figure 4.3: Chemical representation of the PS-*b*-PMMA block copolymer forming the self-assembled template and of the P(S-*r*-MMA) random copolymer adopted as neutralization layer. On the right, three dimensional schematic of the BCP cylindrical morphologies with a parallel and perpendicular orientation with respect to the sample surface. For pattern transfer, a perpendicular orientation is required.

the orientation evolution as a function of the RCP grafted thickness. In Figure 4.4), for an RCP thickness < 4 nm the cylinders are completely parallel to the surface throughout the sample after nanophase separation. Increasing the RCP thickness, the perpendicular orientation starts to nucleate and above 5 nm areas with perpendicular orientation appear. The relative coverage of the areas with perpendicular orientation increases with increasing RCP thickness and for a thickness > 6 nm the cylinders are perfectly oriented perpendicularly to the surface.

The maximum RCP thickness achievable and the value above which a perfect neutralization is obtained are highly dependent on the specific RCP M_w . For the RCP M_w value of 14.5 kg mol^{-1} adopted, on HfO_2 substrates the saturation thickness is slightly lower than what is obtained on SiO_2 [37, 78], suggesting that a lower density of available hydroxyl groups is present on the hafnia surface. These results however demonstrate the possibility to obtain a complete surface neutralization and thus a perpendicular BCP nanodomains orientation on HfO_2 substrates.

The same RCP grafted thickness and an effective surface neutralization above 6 nm was obtained on both amorphous (as deposited) and crystalline (annealed) HfO_2 films and on Al-doped films, indicating that the hydroxyl groups type and content do not vary significantly among these substrates and that it is not substantially influenced by a post-deposition annealing treatment.

Surface cleaning Prior to polymer spinning, the substrate surface needs to be cleaned. This step is particularly important not only because it helps removing the possible contaminants and impurities, but it also can have an impact on the wettability of the surface and occasionally affects the substrate properties

Piranha solution is widely applied on SiO_2 substrates prior to RCP and BCP spinning to remove carbon contaminants. In addition, the effect of the piranha surface treatment in producing a highly hydrophilic surface was reported for silica and borofloat glass, providing an improved grafting of the RCP chains to the Piranha-treated surface [79–81]. However, this wet process has a poor compatibility with transition metal oxides [82].

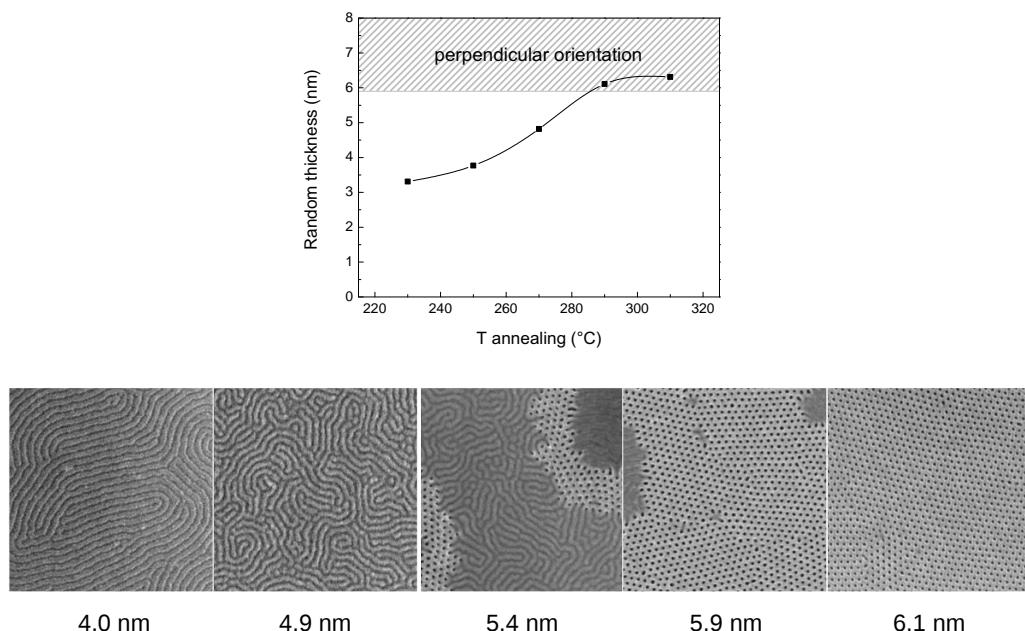


Figure 4.4: Thickness of the grafted RCP layer on the HfO_2 substrate as a function of annealing temperature. In uncleaned samples, the RCP thickness shows a monotonous increase as a function of temperature. Highlighted with gray stripes, the region where a full surface neutralization can be achieved. At the bottom, SEM plane views of the BCP cylinders orientation for the different RCP thicknesses (the edge of the SEM pictures corresponds to $1\ \mu\text{m}$).

In fact, the as-deposited amorphous HfO_2 film is completely removed by a treatment lasting only a few minutes. The HfO_2 film annealed at $500\ ^\circ\text{C}$ for 60 s to induce the oxide crystallization shows an enhanced corrosion resistance. However, in Figure 4.5 AFM and SEM film surface analysis are reported before and after Piranha cleaning, clearly showing the appearance of surface damage after the Piranha cleaning process.

In order to avoid any damage of the HfO_2 film, an alternative route for the surface cleaning from carbon contaminants was explored [83]. An oxygen plasma (O_2 plasma) treatment of 120 s at 40 W was applied, resulting in no detectable HfO_2 film thickness variation by spectroscopic ellipsometry, while from SEM and AFM analysis the appearance of major surface topography modifications was excluded for both crystalline and amorphous films.

In Figure 4.6 the RCP grafted thickness as a function of temperature is compared for the different cleaning processes. In the O_2 plasma-treated samples, the RCP grafting is highly enhanced already at $230\ ^\circ\text{C}$, resulting in a flat trend as a function of temperature, while the saturation thickness is compatible for all the inspected samples. This is an indication that the different dependence on temperature is to be related to more reactive hydroxyl groups formed after exposure to O_2 plasma, rather than to an increase of the number of hydroxyl groups on the hafnia surface. This behavior is unique of the hafnia substrate and is probably to be related to the inherent high density of $-\text{OH}$ sites present on ALD-grown transition metal oxides, while on thermally grown SiO_2 substrates the

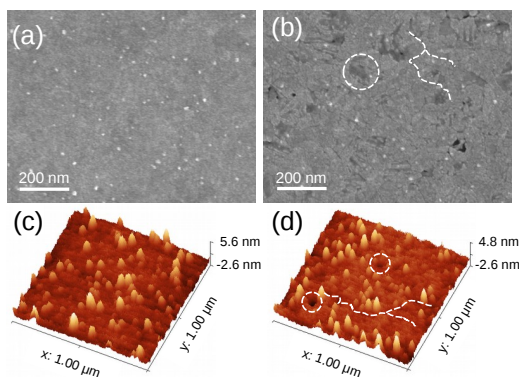


Figure 4.5: SEM plane views of the annealed HfO_2 surface before (a) and after (b) cleaning in piranha solution. Some holes and cracks appear on the surface. AFM surface topography before (c) and after (d) cleaning also reveals the appearance of surface damages.

effect of O_2 plasma cleaning is not as effective in providing an enhanced RCP grafting.

The RCP grafted thickness after Piranha cleaning is inserted for comparison (in this case, a crystallized film was used). As opposed to SiO_2 substrates, in HfO_2 films the RCP thickness after Piranha lies between the thicknesses obtained on the un-cleaned and the O_2 plasma-cleaned samples, while upon saturation the thickness is again comparable (at temperatures $> 290^\circ\text{C}$). In this respect, it is worth noting that the thickness variation among repeated experiments lies within 0.5 nm.

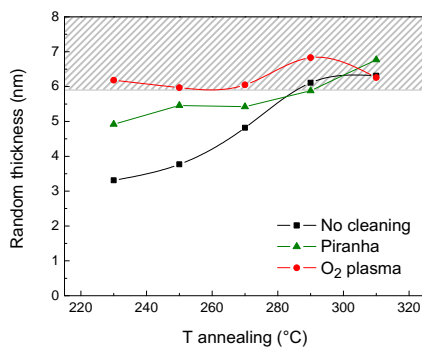


Figure 4.6: Thickness of the grafted RCP layer as a function of annealing temperature. While the uncleaned samples show a monotonous increase of the grafted polymer thickness for increasing temperatures, the samples treated with oxygen plasma have a nearly flat trend and lie in the full neutralization region (highlighted with gray stripes) for all the inspected temperatures.

4.3.2 Block copolymer template formation

After effective surface neutralization by RCP grafting to the HfO_2 surface, cylinders-forming BCP were spun on the neutralized surface. The BCPs contained a styrene fraction of ~ 0.7 (Polymer Source Inc.), were diluted in toluene solution (18 mg in 2 mL) and spun at 3000 rpm for 30 s, forming a film with uniform thickness of 30 nm.

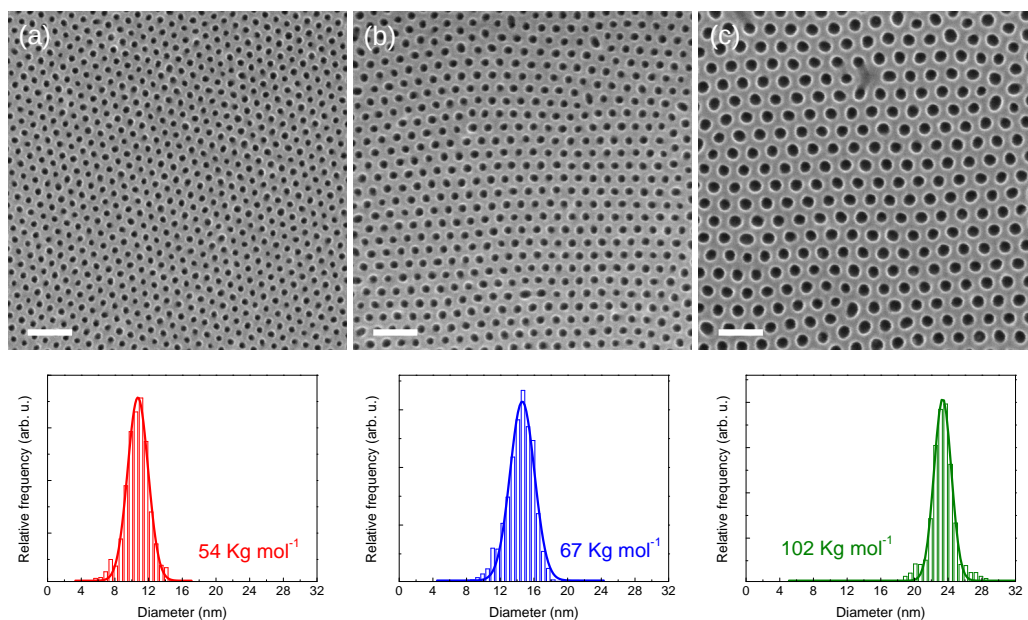


Figure 4.7: SEM plane views of the PS templates with periodically ordered nanopores obtained after 30 s of O_2 plasma exposure from self-assembled BCPs with M_w of a) 54 Kg mol^{-1} , b) 67 Kg mol^{-1} , and c) 102 Kg mol^{-1} (scale bars: 100 nm). At the bottom, relative distributions of the pore diameters.

In order to create templates with different diameter and density of the pores [37], various M_w were adopted: 54 Kg mol^{-1} (PDI 1.07), 67 Kg mol^{-1} (PDI 1.09), and 102 Kg mol^{-1} (PDI 1.08). The nanoscale phase separation was promoted by thermal annealing in an RTP machine at 250°C in N_2 atmosphere, with processing time varying from 5 to 15 min. An annealing time of 5 min was sufficient to obtain a well ordered periodic structure for all the considered BCPs, while the correlation length, defined as the mean distance over which the periodic distribution is conserved, greatly varies for the different M_w and also depends on the annealing time and temperature [41].

After annealing, a regular array of hexagonally packed PMMA cylinders perpendicular to the surface embedded in a PS matrix was obtained. The final PS nanoporous template to be used as soft mask for the BCP-based lithography was obtained by selectively removing the PMMA cylinders by degrading the polymer chains under UV light exposure ($\lambda=253.7 \text{ nm}$, 5 mW cm^{-2}), followed by soaking in acetic acid for 8 min, rinsing in deionized water and drying under N_2 flow. The pores were finally opened and the RCP on the bottom was removed by exposure to O_2 plasma (40 W).

An SEM plane view of the three nanoporous templates is reported in Figure 4.7 together with the distribution of the pore diameters, while the density of the pores attainable with the different M_w adopted is reported in Table 4.1. The determination of the pore size and density was carried out by software analysis applying a threshold mask to the SEM images, then the equivalent radius was extracted using the Grain Distribution function of *Gwyddion* software. The reported mean values and standard deviations of Table 4.1 were extracted from pore counts and Gaussian fits to data similar to the one reported in Figure 4.7. At least 4 SEM images of $1.125 \times 0.774 \mu\text{m}^2$ were used for statistical

data analysis for each sample.

Table 4.1: Density and diameter of the pores (after 30 s of O₂ plasma) obtained from self-assembly of the three different BCPs adopted. The uncertainties correspond to the standard deviations extracted from analysis of SEM images.

M_w (g mol ⁻¹)	54 K	67 K	102 K
Density of the pores ($\times 10^{11}$ cm ⁻²)	1.520 \pm 0.014	1.015 \pm 0.015	0.520 \pm 0.010
Diameter of the pores (nm)	12.4 \pm 1.0	14.6 \pm 1.1	23.4 \pm 1.0

While the density of the pores is fixed for a particular M_w , the mean pore diameter strongly depends on the O₂ plasma time that is necessary to completely open the pores and remove the RCP from the bottom, uncovering the oxide surface. Indeed, after the PMMA component has been degraded and removed, an exposure to O₂ plasma isotropically erodes the remaining PS matrix, enlarging the pores in a mostly linear fashion as a function of time (Figure 4.8). The error bars in the figure depict the standard deviation of

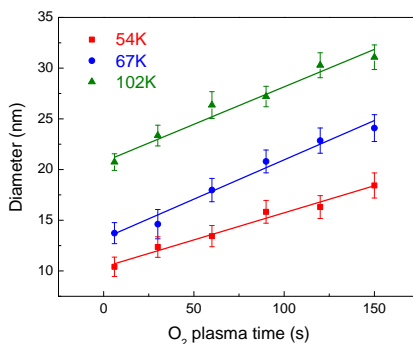


Figure 4.8: Diameter of the pores in the BCP-formed PS template for increasing oxygen plasma time (from 6 to 150 s) for the three different BCP molecular weights.

the diameters as derived from multiple SEM images. Even if the pores are enlarged by nearly 10 nm after 150 s, the diameter dispersion only slightly increases and σ remains below ± 1.3 nm, meaning that the control over the pore size distribution is not worsened by exposure to O₂ plasma.

Figure 4.8 also reports a substantial diameter overlap for different M_w obtained by adjusting the O₂ plasma time. This property potentially allows a decoupling between the defined features density and their dimension. However, for an RCP thickness of ~ 6 nm a minimum plasma time of 150 s is required to remove the bottom-lying RCP and completely open the pores in order to perform a pattern transfer using a lift-off process.

4.3.3 Pattern transfer process

The patterning of ordered metal NPs was accomplished through lift-off process. First, a metal film was deposited over the self-assembled polymeric template, then the template together with the excess metal on top were removed by wet process [53, 56, 73, 84].

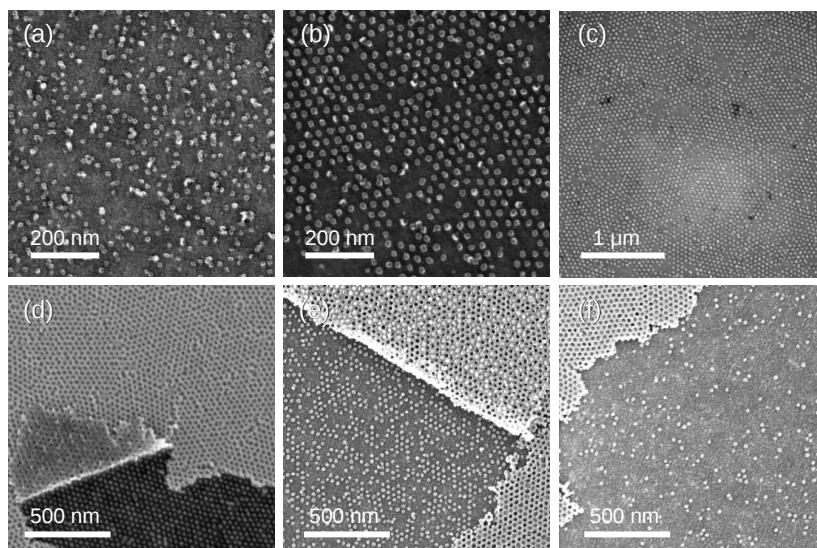


Figure 4.9: Lift-off processes for 5 nm Pt performed in piranha solution from a 67 Kg mol^{-1} BCP. (a) An insufficient O_2 plasma time (120 s) leads to an incomplete opening of the pores, resulting in a poor pattern transfer. (b) and (c) regular arrays of Pt dots obtained after 150 s of O_2 plasma, with a wet piranha etch of 10 min. Even if large areas can be developed in a short time, some flaws are clearly visible in the periodic distribution. (d) Early stage of the lift-off process, when the polymeric mask starts to lift up exposing the regular array of metal dots. After 5 min (e) and 25 min (f), an increasing deterioration of the transferred pattern can be observed with time.

For the deposition of the top metal, different techniques can be used, as described in chapter 3. Nevertheless, for the template to be efficiently removed, a good separation between the metal covering the template and the metal within the pores is required. While highly conformal depositions like ALD should be avoided, also the physical sputter deposition brings poor results since it leads to a partial coverage of the template walls. On the contrary, electron beam evaporation method offers the advantage of a low chamber pressure ($\sim 10^{-6}$ mbar) and a less energetic deposition if compared with the sputtering method, allowing a better pattern transfer by lift-off of nm-sized features.

Another requirement necessary for the fulfillment of the lift-off process is that the deposited thickness respects the rule of thumb of $\leq 1/3$ of the polymer template thickness. With a PS template ~ 30 nm thick, NPs of about ~ 10 nm can be obtained. If a higher metal thickness is required, thicker template masks can be deposited by either lowering the spinning velocity or depositing a denser polymer solution [41].

Two wet methods (acid or solvent) were alternatively applied to dissolve the template mask. The immersion of the sample in piranha solution rapidly removes the polymeric component, resulting in big areas developed in a short time. However, the etch rate is so high that the process can be difficultly controlled. Additionally, only a few materials have a sufficiently high etch selectivity to be patterned with this etchant [82]. Another concern is the surface damage that can be produced even on a crystallized HfO_2 substrate, as mentioned previously.

The patterning of a 5 nm Pt film with the piranha wet etch is shown in Figure 4.9.

Platinum is among the few metals compatible with piranha. However, several flaws manifested with increasing processing time. The same sample analyzed after 5 and 25 min of piranha soak shows a clear loss of the patterned particles and a deterioration of the periodic distribution for increasing processing time. The type of the generated flaws, including repositioning of the metallic dots and tilting, indicates a poor Pt surface adhesion.

For application purposes, platinum is known to have a poor surface adhesion on many materials, including transition metal oxides. The addition of an interlayer of titanium greatly improves the pattern adhesion [85, 86]. However, Ti is etched away very fast by piranha solution.

An alternative route to the piranha etch can be a selective solvent for the PS template, an approach that brings a clear advantage in terms of material compatibility. Toluene is a PS selective solvent, however during the O₂ plasma treatment a partial cross-linking of the polymer chains was found to occur, decreasing the PS solubility starting from 30 s of plasma. The consequence is that long baths in warm toluene are required, while a low power sonication should be added to break the metallic film in order to aid its removal. With this method, areas of the sample with lateral dimension of the order of hundreds of μm can be effectively patterned, but a whole template removal is difficult to achieve unless very long times are applied.

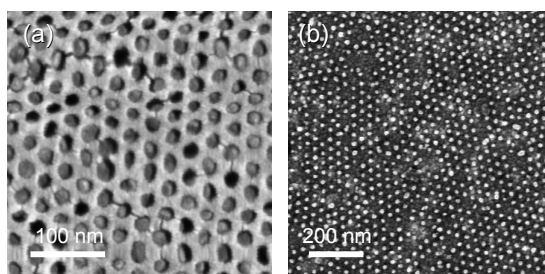


Figure 4.10: Patterning of a 5 nm Pt film by lift-off in a warm toluene bath. (a) Detail of the residual metal covering the PS template showing some cracks after prolonged sonication. (b) The template obtained from the 67 Kg mol⁻¹ BCP is well reproduced, but some patterned features are missing.

The lift-off performed in toluene allows a better pattern transfer, with the disappearing of flaws caused by repositioning of the metal dots (Figure 4.10). Nevertheless, the long wet process and the addition of sonication, even at low power, causes the loss of some of the patterned features in the periodic matrix.

The addition of a Ti layer of 4 nm prior to the Pt deposition allows to overcome the Pt adhesion issue [85]. Comparing the PS nanoporous template with the obtained Pt/Ti metal NPs (Figure 4.11), a perfect pattern transfer can be found for the 67 and 102 Kg mol⁻¹ BCPs, with flaws only coming from the original template, mainly in correspondence with grain boundaries.

The 54 Kg mol⁻¹ BCP constitutes a particular case. The small dimension of the pores and their close vicinity establishes a nearly continuous metallic film after deposition. This adds a difficulty in the template removal, requiring longer processing times and a higher sonication power, leading to a complete loss of the patterned features. In order to degrade the polymer in a faster time, we adopted a short dip in piranha solution (5

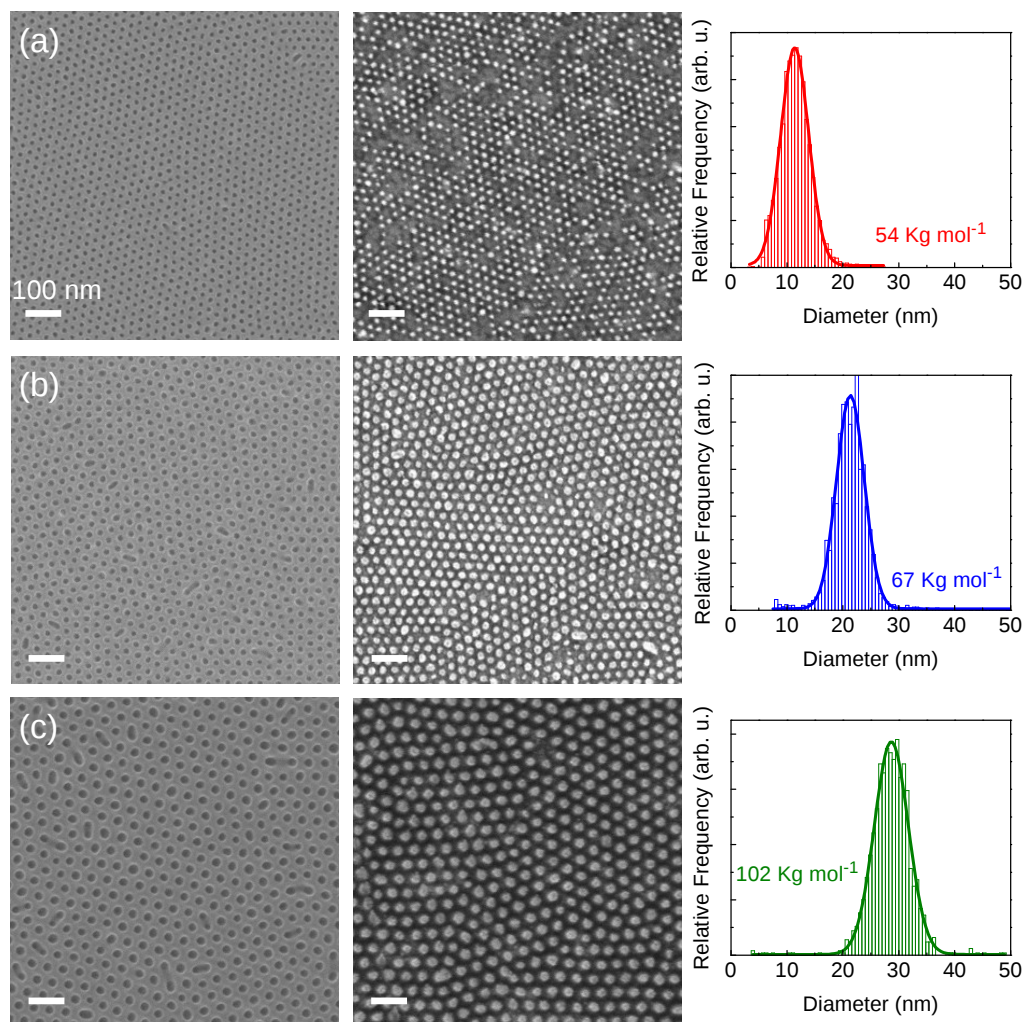


Figure 4.11: BCP-based templates originated from polymers with M_w of 54 Kg mol^{-1} (a), 67 Kg mol^{-1} (b) and 102 Kg mol^{-1} (c) and the relative Pt/Ti dots (6 nm Pt, 4 nm Ti) obtained by lift-off process. On the right, statistical distributions of the dots diameters. (Scale bars: 100 nm).

s) before soaking in toluene. It is worth to note that this very short dip does not impact significantly on the underlying HfO_2 surface. The NPs deficiencies that can still be identified in the periodical matrix can be related to either a not complete opening of the pores or to the fast piranha dip required in this case.

The diameter of the pores completely opened by 150 s of O_2 plasma and the relative diameter of the Pt/Ti NPs fabricated by pattern transfer for the three adopted templates are summarized in Table 4.2. For the 67 Kg mol^{-1} and 102 Kg mol^{-1} BCPs, the resulting metal NPs are about 2 nm smaller than the original template holes, a value still compatible within the uncertainties. The slightly smaller dimension can be related to a partial covering of the template walls.

Table 4.2: Diameter of the pores after 150 s oxygen plasma treatment and relative diameter of the Pt/Ti NPs after pattern transfer. The uncertainties correspond to the standard deviations extracted from Gaussian fits.

M_w (g mol ⁻¹)	54 K	67 K	102 K
Diameter of the pores (nm)	18.4±1.2	22.9±1.2	31.1±1.2
Diameter of the NPs (nm)	12.0±2.5	21.4±2.5	28.8±2.7

For the 54 Kg mol⁻¹ BCP template the discrepancy is higher, about 6 nm. Metal NPs with a diameter of only 12 nm were obtained in this case even if the original pore diameter is around 18 nm. It is interesting to note that the width of the Gaussian distribution is similar to that obtained with the wider templates.

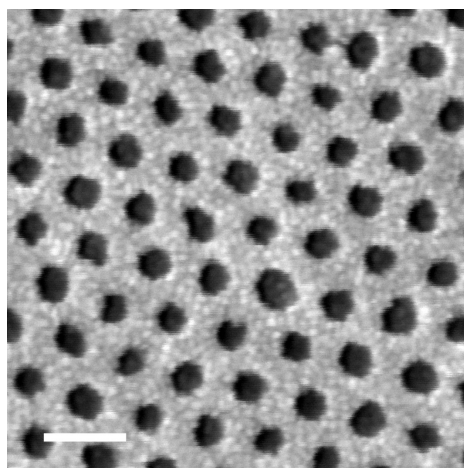


Figure 4.12: Pt/Ti film deposited over the PS nanoporous template. Grains of about 6–7 nm are distinguishable in the metal film. (Scale bar: 50 nm).

The experimental results suggest that the process of pattern transfer operated with the smallest template reaches a limit beyond which the final result changes significantly. A plausible explanation is that when the dimension of the pores is approaching the dimension of the grains composing the Pt film, the deposited film can no longer be seen as continuous. At this size, the granularity of the patterned film could influence the result of the pattern transfer technique [87]. Indeed, SEM images of the deposited Pt/Ti film evidence the presence of grains with an average dimension of 6–7 nm (Figure 4.12). This peculiar behavior allows to pattern ultras-small NPs of only 12 nm without losing control over the particles size distribution.

The proposed fabrication method can be easily extended to the patterning of other materials with the same control over the defined features size and density, which are mainly determined by the self-assembled polymeric templates adopted. The final dimension of the NPs obtained with the smaller templates is however likely to depend also on the nanostructure characteristics of the deposited film, which can result in a par-

ticle size smaller than the original template as in the present case.

4.3.4 Highly scaled, high density array of patterned top electrodes for resistive switching memories

The proposed fabrication method allows a relatively easy and cost-effective way to produce a very large number of ordered arrays of metal NPs in parallel all over the sample substrate. This tool can be exploited at the laboratory level for the patterning of nanoscale electrodes in M–I–M systems. The possibility to apply BCP templates on HfO_2 films allows to eventually build up resistive switching nanodevices.

The strengths of BCP lithography in the framework of RRAM devices are manifold. First, it allows the definition of electrodes with diameter down to 12 nm with controlled dispersion. The size of the electrodes can be tuned by the choice of the BCP M_w , and sub-10 nm features can be achieved by using Si-containing BCPs [33, 45], opening up the possibility to study the resistive switching phenomenon at the ultimate scalability limit, when the dimension of the device approaches the size of the filamentary conduction path. An important characteristic is also the compatibility of BCP-based templates with the standard fabrication processes of the microelectronic industry [42, 88]. Nonetheless, probably the main advantage of the BCP lithography is the extremely high density of the patterned features (up to $1.5 \times 10^{11} \text{ cm}^{-2}$ in this work), which goes beyond the limits of alternative patterning technologies. This enables the study of the effect of aggressively reducing the pitch between the distinct devices, which will be the topic of the next chapter. A schematic diagram of the workflow of the process used to pattern nanoscale top electrodes of RS devices is visualized in Figure 4.13.

In principle, different fabrication methods can be applied in order to obtain noble metal NPs with controlled size and density. Examples are solid-state dewetting [89–91], metal deposition assisted by colloidal PS particles [75], and block copolymer micelle lithography [92]. However, the presented method allows ordered arrays of NPs to be produced in a periodic fashion maintaining a uniform control over the NPs size distribution for the different dimension and with full CMOS-processes compatibility, avoiding for example aqueous solutions which would limit the fields of application.

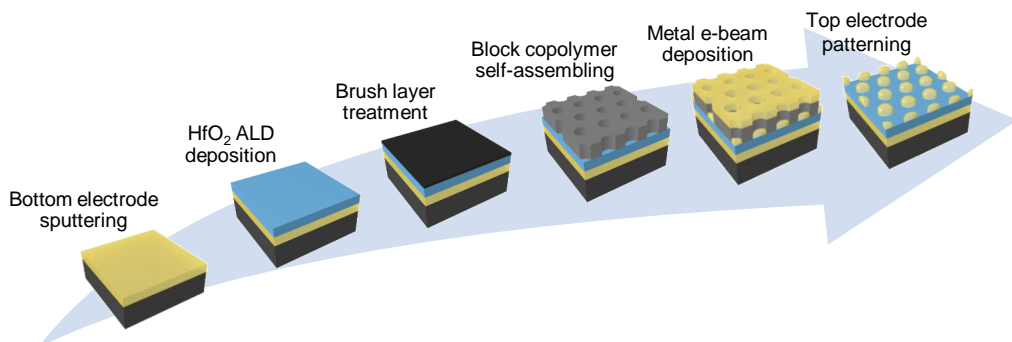


Figure 4.13: Procedure for the top electrode patterning. A BCP self-assembled template was adopted for pattern transfer with a lift-off process.

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Characterization of high density arrays of resistive switching devices

5.1 Introduction

This chapter presents an investigation of the conduction variability and resistive switching behavior at the nanoscale. First, bare HfO_2/TiN films were inspected by conductive atomic force microscopy (C-AFM). The conductive tip was scanned above these amorphous oxide films in order to evaluate the inherent nanoscale conduction variability, which characterizes the initial state of HfO_2 -based RRAM devices.

The system composed by C-AFM tip/oxide/bottom electrode has itself all the constituting elements of RRAM devices. Nanoscale resistance switching (RS) operations were in fact reported in the literature using a direct tip contact over the oxide [1]. However, several limitations arise in this configuration which can hinder the characterization of the RS phenomenon. In particular, very high voltages are required for the initial forming operation due to several issues located at the tip/oxide interface.

To overcome the limitations imposed by the direct tip contact, a fabrication procedure was developed to produce a high density array of top electrodes with controllable size and selectable electrode material. The top electrodes were patterned using a bottom-up fabrication approach based on block copolymer (BCP) self-assembling. A detailed description of the fabrication procedure can be found in Chapter 4. Ordered array of Pt/Ti/ HfO_2 /TiN RRAM devices with a well-controlled diameter of 28 nm and a density of 5×10^{10} devices/ cm^2 were produced in this way. A measurement methodology was developed using C-AFM to selectively address individual memory cells in the highly scaled and high density layout of Pt/Ti top metal electrodes. The memory characterization concerned in the first place the device initial state prior to switching. The initial device-to-device variability was correlated with the inherent presence of the leakage current paths randomly spread in the HfO_2/TiN stack. Proceeding with the device characterization, bipolar RS operations were confirmed in the nanoscale devices with a forming voltage lower than what is in general observed with the direct adoption of the C-AFM tip as top electrode.

A crosstalk between not continuous memory cells at a distance of 75 nm was discovered upon set and reset switching. The memory structure will be examined and a model will be proposed to elucidate the crosstalk arising at high density based on the formation of filamentary conduction paths leading to sneak connections among different devices. The experimental data suggest the occurrence of an important scalability issue for ultra-high density memory arrays based on continuous HfO_2/TiN thin films. RS device structures of this type were suggested in particular as a possible solution for

3D integration. Consequently, alternative integration schemes need to be envisioned in order to decouple the electrical switching phenomena of each single cell when the distance between the devices approaches a critical limit.

5.2 Nanoscale conduction variability in HfO_2 thin films

Figure 5.1 shows the C–AFM analysis carried out on the surface of HfO_2/TiN films. The HfO_2 thickness is alternatively 3 nm or 6 nm. Along with morphology maps of the surface reported in Figures 5.1(a) and (c), this method allows to obtain current maps of the local conductivity and consequently to reveal the oxide non-homogeneity at the nanoscale (Figures 5.1(b) and (d–f)). During the electrical analysis, the voltage is applied at the bottom of the sample through the AFM chuck, while the conductive tip is grounded. The conductive C–AFM tip acts as top electrode and a resolution down to the nm level can be achieved thanks to the reduced tip–surface contact area.

When a small voltage of 0.5 V is applied at samples with 3 nm HfO_2 film on top of the TiN electrode, the majority of the surface presents very low leakage current, while isolated current spots indicate the presence of randomly spread leaky sites (Figures 5.1(b,d)). No clear correlation can be found between the surface topography and the leaky sites, while the electrical conduction greatly differs between the different sites.

Response as a function of applied voltage The number of visible conductive spots mostly depends on the applied voltage, since for very low bias most of the spots remain hidden below the detection limit. The current threshold can be set around 1.5 pA considering the average noise in the not conductive areas. When a bias of 0.5 V is applied to the sample, ~ 50 spots/ μm^2 are visible in Figures 5.1(b,d), while about 100 spots/ μ^2 are revealed above the detection limit in Figure 5.1(e) when the applied potential difference is increased to 1.5 V. This higher bias allows to better highlight the variability of the current level measured in the conductive areas. Indeed, it changes considerably among conductive spots and ranges between a few pA up to the saturation of the current amplifier (set to 100 pA in this case) for a few conductive spots, with an average value of ~ 10 pA at 0.5 V and ~ 25 pA at 1.5 V.

The C–AFM electrical characterization of the bare oxide is in agreement with what is in general observed for amorphous HfO_2 films of 3 nm deposited on TiN, with no evident correlation between the surface morphology and the location of the leaky sites [2, 3]. It is worth to note that the same general behavior is also observed in HfO_2 films grown on different substrates such as SiO_2 irrespective of the specific substrate composition and morphology, suggesting that the conductance inhomogeneity is rather an intrinsic property of the HfO_2 film [4] and it is not induced by the chemical or morphological properties of the TiN bottom electrode.

Comparing different C–AFM tips Different conductive tips were used in Figures 5.1(a,b) and 5.1(c,d). In the first case it was applied a highly doped diamond-coated tips (CDT-CONTR from nanosensor, with 100 – 200 nm curvature radius), while in the second case a sharp Si tip with a 25 nm thick Pt/Ir coating (PPP-CONTPt from nanosensor, with a guaranteed curvature radius below 10 nm) was used. The diamond-coated is best suited to withstand repeated scans thanks to its higher mechanical strength, but has larger nominal curvature radius. Nevertheless, the contact area is highly reduced due to

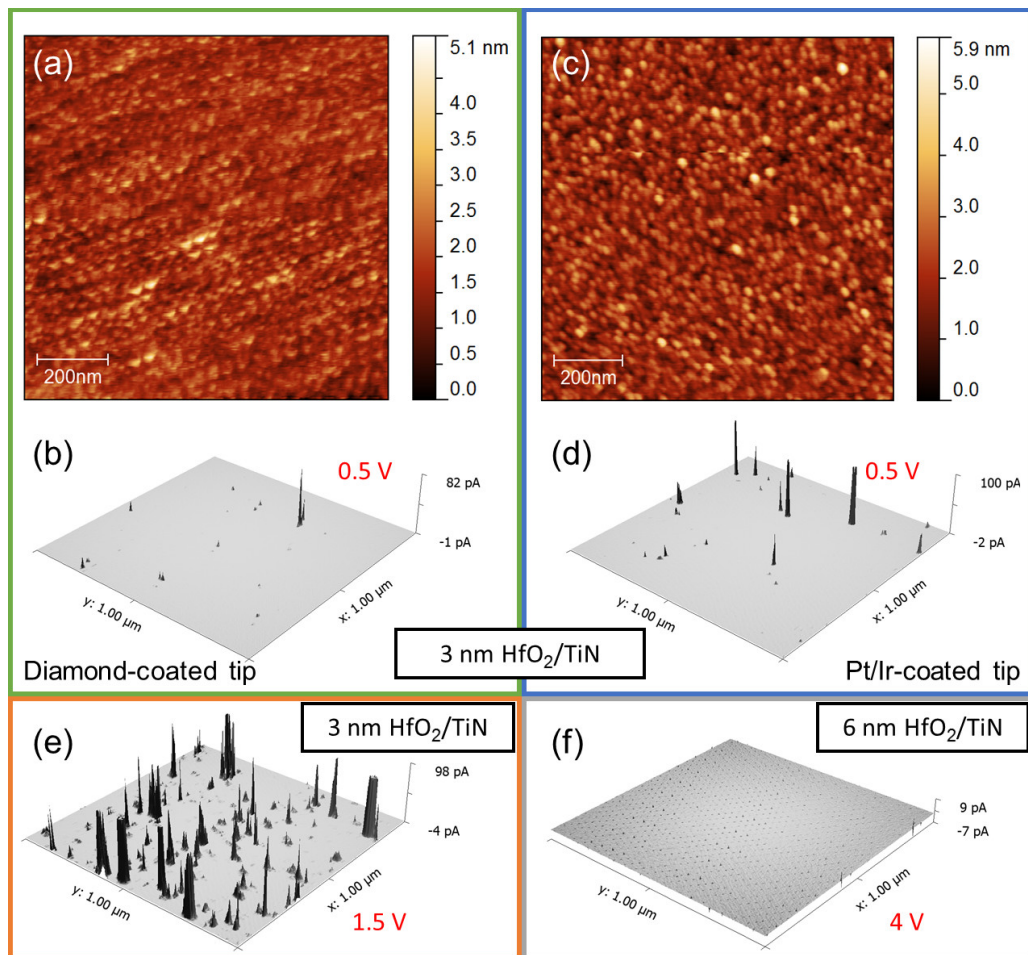


Figure 5.1: AFM surface morphology (a) and relative 3D current map (b) of a 3 nm HfO₂/TiN film inspected using a diamond-coated tip at 0.5 V bias. (c,d) Morphology and relative current map acquired with a Pt/Ir-coated tip at 0.5 V. (e) Current map of the same film with an applied bias of 1.5 V using a Pt/Ir-coated tip. (f) A thicker 6 nm HfO₂/TiN film shows no conductive spots even at 4 V (Pt/Ir-coated tip).

the roughness of the coating grains around 10 nm, which provides a low effective contact area on flat films.

In spite of the different tips adopted, a similar result was obtained in terms of density of current spots. Comparing Figures 5.1(b) and (d), ~ 50 spots/ μm^2 are visible with both Pt/Ir and diamond-coated tips at 0.5 V. The difference between the adopted tips lies in the measured area of the conductive spots. With the Pt/Ir-coated tip, the current spots have an average area of 76 nm^2 , resulting in a coverage of 0.4% of the sample area. With the diamond-coated tip, the spots average area reduces to 23 nm^2 , corresponding to a coverage of 0.13% of the inspected area. The difference in the measured average spot area points toward a lower effective contact area when a diamond-coated tip is used, probably because of the nm-scale granularity of the coating. An upper limit of about 5 nm can be determined for the average lateral dimension of the conductive spots based on this current analysis. This value is on average smaller than the 28 nm diameter of the top electrodes that will be defined by BCP lithography on top of the HfO_2 surface.

Comparing different HfO_2 film thicknesses When a HfO_2 film of 6 nm is considered, no relevant leaky sites can be detected up to 4 V (Figure 5.1(f)). This result highlights the highly insulating nature of the thicker dielectric film even when the same electric field is applied. However, this lack of nanoscale conduction in the as deposited film prevents the achievement of a reproducible RS in the voltage range of the C–AFM instrumentation.

RS operations with a direct tip contact The above discussion is based on C–AFM scans performed at a low voltage in order to avoid any perturbation induced by the electric field. This was verified by repeating consecutive C–AFM maps of the same area. Conversely, a non-volatile change of the resistance requires higher voltages. A test of the voltage required to induce an oxide breakdown in the film can be performed by placing the tip in various positions and acquiring current–voltage characteristics in a way similar to what was previously discussed for μ -size devices in chapter 3. This procedure was carried out on thin HfO_2 film of 3 nm in order to reduce the required voltage.

After the initial C–AFM scan at low voltage shown in Figure 5.2(a), 25 different locations were chosen for an I–V characterization with fixed tip position using a Pt/Ir-coated tip as top electrode. The array of 5×5 I–V curves in the 0–10 V range (Figure 5.2(b)) was performed with a series resistance of 10 M Ω to avoid an irreversible oxide breakdown. However, no forming transition was obtained in the 0–10 V range allowed by the instrument, locating the tip in either insulating sites or in correspondence of leakage current paths. This is consistent with previous works on 3 nm HfO_2 amorphous films, since quite a high voltage (>16 V) was in fact necessary to induce the oxide breakdown with a direct tip–oxide contact [2, 3].

After the measurements in the 5×5 array, the next AFM surface topography showed an array of protrusions in correspondence of the tip sites (Figure 5.2(c,d)). This effect could be related to anodic oxidation induced by the water meniscus present around the AFM tip due to air humidity. It is worth to mention that no noticeable variation in local conductivity was observed in correspondence of the I–V sites.

This effect, together with an instable and not always reproducible tip–surface contact, can prevent a reliable investigation of the RS properties using the AFM tip as top electrode. It should also be added that the AFM tip and its coating are subjected to wear during scanning, thus the effective contact area and the conductive property of the tip can change during operation. All these reasons could be responsible for the impossibil-

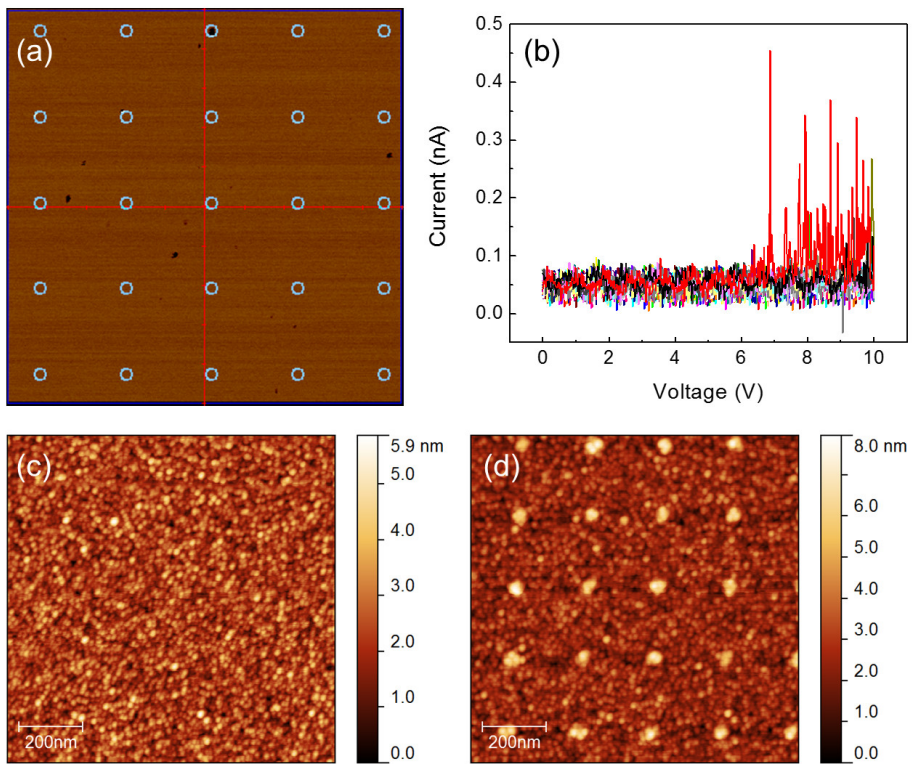


Figure 5.2: (a) Matrix of 5×5 points for fixed-tip current–voltage characteristics carried out at 1 V/s (b). (c, d) AFM surface morphologies acquired before and after fixed-tip I–V characterization with a series resistance of $10 \text{ M}\Omega$.

ity to achieve a resistance variation in a reasonable voltage range by simple tip–surface punctual contact.

The solution to this problem was found in the controlled fabrication of monodispersed top electrodes by BCP-assisted lithography. In this way real M–I–M devices were inspected with a defined and constant area and a more easily selectable top electrode material. The proposed system appears as an interesting option for the investigation of RS properties at the nanoscale.

5.3 Characterization of nanoscale RRAM arrays fabricated by block copolymer templates

On top of the 3 nm HfO_2/TiN film, ordered arrays of top electrodes with diameter of 28 nm were patterned starting from a PS nanoporous template formed by BCP self-assembly and a lift-off process in toluene, as described in chapter 4. For the formation of the nanoporous template, a BCP with M_w of 102 Kg/mol was chosen so that the produced regular features have a dimension and spacing compatible with the dimension of the C–AFM tip. With smaller M_w , the metal nanodots can not be easily distinguished during the AFM scans, since the tip can not plunge completely between neighboring dots.

In Figure 5.3 the regular PS nanoporous template, together with the Pt/Ti nanoelectrodes organized in regular arrays with HCP symmetry are reported. Figure 5.3(d) shows a 3D representation of the surface morphology and a line scan extracted from the same image. The data clearly indicates that the C–AFM tip could distinguish the different nanodevices, which is an essential requirement for a selective addressing of the nanoscale memory cells.

5.3.1 Initial state characterization of a large number of nanoscale devices

Combined topographic and current maps acquired by C–AFM on top of the patterned metal electrodes allow the electrical characterization of a large number of devices in the same scan. This method can be used to probe the leakage conductance of the nanoscale devices in the initial state, before any RS operation. A potential difference of 1.5 V was chosen to highlight the device variability, yet low enough to avoid electric field-induced perturbations, as verified with repeated scans.

In Figure 5.4(a,b) a close correlation can be found between the hexagonally packed Pt/Ti metal electrodes and the uniform conductive spots in the current map, confirming the equipotential behavior of the metal electrodes. This is the first requirement for their correct operation, since the voltage applied through the AFM tip is distributed to the whole device area.

The leakage current level of the different spots in Figure 5.4(b) highly varies among different devices. By plotting the cumulative distribution of the resistance measured on each individual device in the initial state, two different conditions can be identified in Figure 5.4(c). High resistance devices, which cover nearly 80% of the total population, show a low dispersion of the resistance, while the remaining low resistance devices have a resistance value spread over almost 2 decades. Repeating the initial state analysis in a different area of the sample and with a different voltage (1 V), the same general trend is obtained, as shown in Figure 5.4(d). This confirms that the 80% – 20% subdivision of the

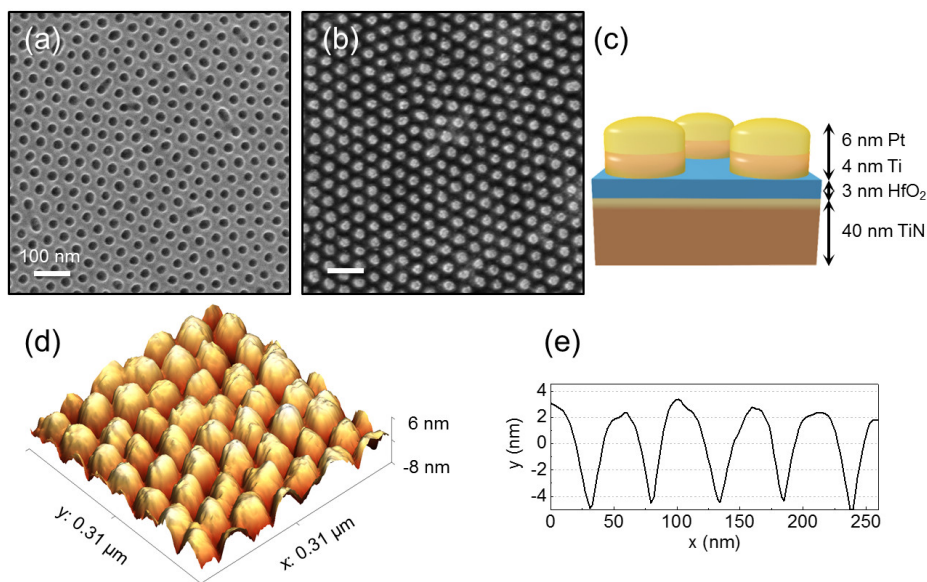


Figure 5.3: SEM plane views of (a) nanoporous PS template obtained by BCP self-assembling in periodic perpendicular cylinders and (b) arrays of Pt/Ti top electrodes on top of the HfO₂ surface obtained from the self-assembled polymeric template depicted in (a). (c) Device stack representation. (d) AFM surface morphology acquired with a Pt/Ir-coated tip showing the top electrodes with hexagonal distribution and relative line scan (e) displaying the electrodes height. Reprinted from [5].

device resistance status in the initial state is a general behavior and can be reproduced in different area of the sample.

The resistance distribution can be explained by comparing the cumulative device distribution with the analysis previously reported on the bare HfO₂ surface. We observed an average number of ~ 100 current spots/ μ^2 at 1.5 V, a value in agreement with previous observations [2]. Comparing this value with the patterned density of 500 devices/ μ^2 , we can clearly correlate the 20% of highly conductive devices with the inherent presence of leakage current paths in the HfO₂/TiN stack. Given their wide current dispersion, they are probably responsible for the resistance variability over 2 decades for the 20% of the most conductive devices. On the other hand, the 80% of highly resistive devices can be correlated with the insulating background found outside of the current spots in the bare HfO₂/TiN film.

When a thicker HfO₂ film of 6 nm is inspected, most of the surface is highly insulating with a registered current level below the instrument sensitivity, due to the low density of the leakage sites. The same occurs with patterned Pt/Ti electrodes on top. However, in Figure 5.4(f) a spot appears at the site of one of the metal electrodes for the higher potential difference of -4.5 V. This implies that a small but non-zero density of leakage paths also exists in the 6 nm oxide.

In Figures 5.4(e,f) the C-AFM investigation was carried out on metal electrodes fabricated starting from a BCP with molecular weight (M_w) of 67 Kg/mol, resulting in electrodes of 21 nm in diameter. The shape of these smaller metal electrodes is clearly con-

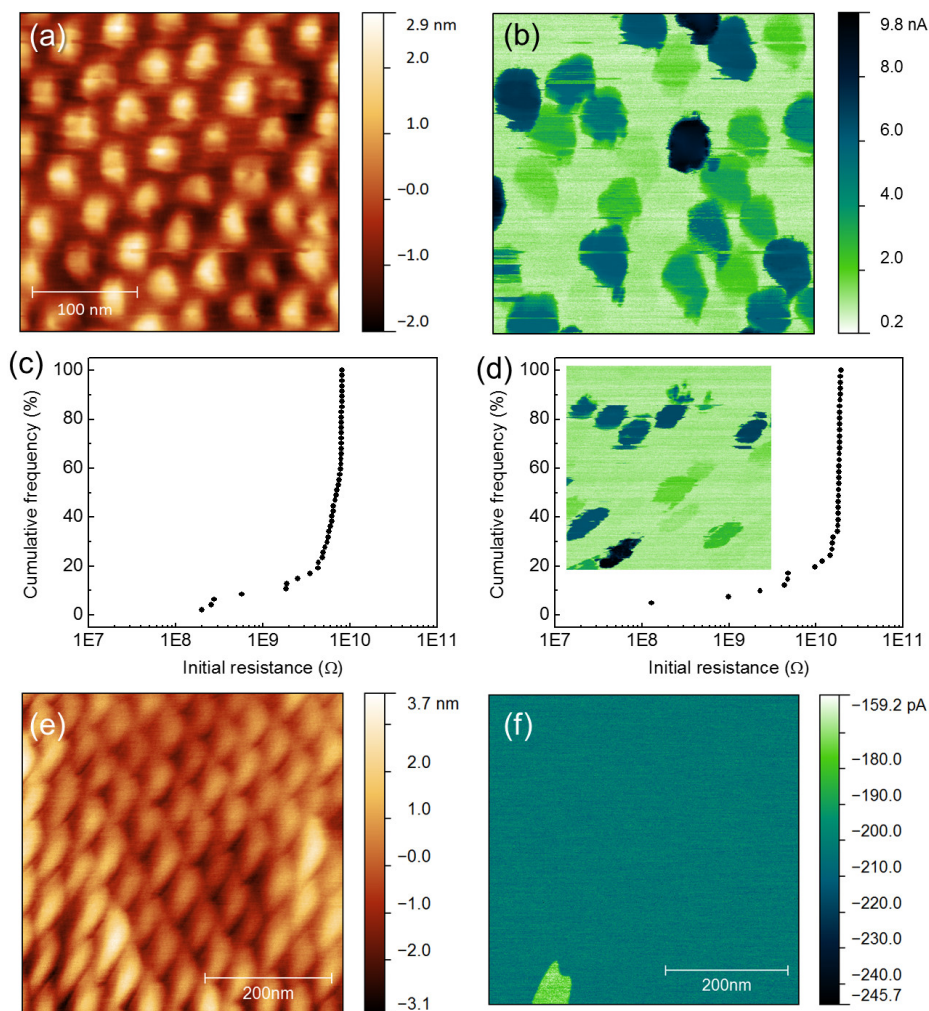


Figure 5.4: AFM morphology (a) and corresponding current map (b) of top Pt/Ti metal electrodes (diameter of 28 nm) defined by BCP lithography on top of a 3 nm HfO_2/TiN film, acquired with an applied bias of 1.5 V. (c) Initial state resistance distribution of the devices in figure (b). (d) Current map and resistance distribution of the devices in the initial state acquired in another area of the sample with a bias of 1 V. The same general trend of (c) can be identified also in this case. (e) C-AFM morphology and relative current map (f) of a sample containing Pt/Ti metal electrodes (diameter of 21 nm) on a 6 nm HfO_2/film with an applied bias of -4.5 V. Reprinted from [5].

volved with the triangular shape of the diamond AFM tip, and neighboring electrodes appear connected due to the small lattice spacing of 35 nm [6]. This happens since all the aforementioned analysis were carried out with diamond-coated tips. This type of hard coating is best suited for repeated C–AFM scans with an applied bias, while other metal-coated tips would rapidly degrade. However, this comes at the cost of a larger radius of curvature. For this reason, all the electrical characterization on nanoscale electrodes was performed with metal electrodes fabricated from BCPs with a M_w of 102 Kg/mol, which gives rise to electrodes of 28 nm diameter and 47 nm lattice spacing.

5.3.2 Resistive switching at the nanoscale

Forming operation With the sharp conductive tip of the C–AFM, it is possible to selectively address individual memory cells. By placing the tip over a selected electrode and ramping the voltage, the forming transition can be obtained as in Figure 5.5(a). Repeating the operation in different randomly selected devices, the forming voltages are comprised in the 3.5 – 5.5 V range (Figure 5.5(b)). The forming transition was obtained in devices comprised in either the 20% of conductive devices or in the 80% share, meaning that the inherent presence of leakage conduction paths is not a prerequisite for the device forming. However, using C–AFM as the contacting method does not allow to acquire enough statistics to conclusively correlate the initial state with the forming voltage and the subsequent switching behavior.

The presence of a forming transition is in contrast with the absence of any resistance transition observed in the 0 – 10 V range with a fixed tip operation without any metal dot (Figure 5.2). In contrast with a direct C–AFM tip contact, the nanoscale electrical characterization through nanoelectrodes defined by BCP lithography brings the big advantage that real devices are investigated. As previously discussed, various artifacts located at the tip–oxide interface can be avoided (water meniscus, anodic oxidation, etc. [7]), while the device area can be carefully defined by the BCP template and the electrode material can be more easily selected. In this respect, the insertion of the Ti interlayer in the top electrode stack allowed to reproduce a memory stack widely adopted in the literature, which was also associated with a reduction of the forming voltage [8–10].

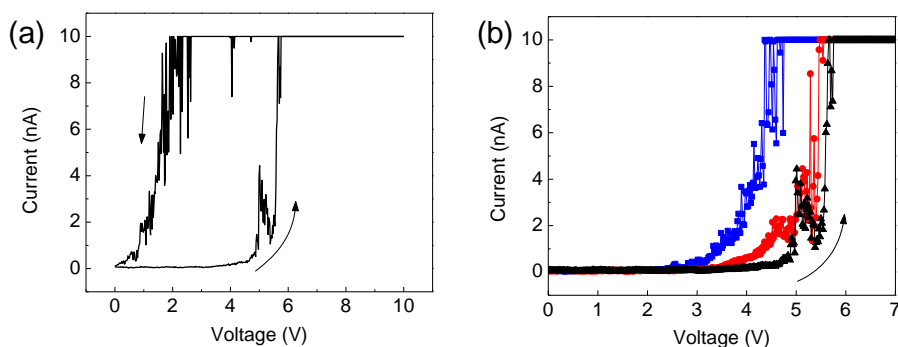


Figure 5.5: (a) High initial resistance device: Forming process in a Pt/Ti/HfO₂/TiN nanodevice. 10 nA is the maximum detectable current, not a current compliance. (b) Other forming transitions in different nanodevices. Reprinted from [5].

Resistive switching with a fixed tip position Resistive switching operations in nanoscale devices were first performed using fixed tip operations. The sample surface was first scanned to locate the top electrodes, then individual devices were addressed and I–V curves were acquired.

In Figure 5.6(a), a current map acquired at 0.5 V shows in the scanned area two devices with high initial conductance. Selecting the device indicated by an arrow (on the left) and performing a steady state negative voltage sweep (in inset), the device conductance is suppressed, as it is evident in the subsequent reading current map of the same area (Figure 5.6(b)). This can be interpreted as the reset of a device that was initially in a LRS, with a conductive channel already in place in the oxide without the requirement of an initial forming step. In other words, the initial conductance of devices located in correspondence of leaky sites can be manipulated with bipolar voltage operations without the need of an initial forming step.

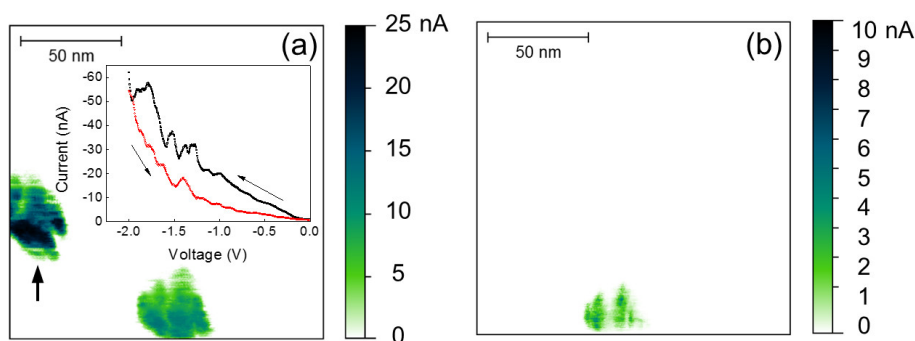


Figure 5.6: (a) Current map acquired at 0.5 V. A device with high initial leaky conduction is indicated by an arrow. A reset operation was performed in this device (the I–V curve is reported as inset). (b) After reset, the device conductivity is suppressed and it is not anymore visible in the reading current map. Reprinted from [5].

Reproducible resistive switching with a scanning tip Owing to the small electrode dimension, which is of the same order of magnitude of the tip contact area, a different C–AFM procedure was developed to gain better reproducibility during repeated set/reset processes. By scanning the tip over only one selected device with a constant applied bias, the tip–electrode contact was improved, while the applied bias was chosen high enough to induce the RS phenomenon. The conductance modification was then inspected with a following reading current map over a larger area at a low non perturbing voltage.

The result of this switching procedure is reported in the series of reading current maps of Figure 5.7. In Figure 5.7(a), a current map displays the initial resistance status of the devices. The C–AFM tip was then scanned with a constant bias of +4 V over the area enclosed by the black square (50 nm side), containing a single device which exhibits an initial current level below the ammeter sensitivity but was visible in the related topographic map. The subsequent current map of the whole area in Figure 5.7(b) shows a significant conductance increase of the device under test (forming process). The voltage required to induce the forming transition was in this case slightly lower than that required for punctual C–AFM tip operations as in Figure 5.6(a), thanks to the longer lasting voltage stress induced with scanning tip operations, along with a more stable

tip–electrode contact that helps reducing the contact series resistance. Scanning again over the same device with -3 V, the conductivity was substantially suppressed (reset), as visible in Figure 5.7(c). The application of $+4$ V was able to restore the low resistance state (Figure 5.7(d)). The reading current maps were acquired about 10 minutes after the switching occurred, indicating a non-volatile switching in resistance.

The same set/reset operations with the conductive tip scanning over a box of 50×50 nm² was also performed on a device that exhibited a not negligible initial state leakage current, as reported in the current maps series of Figure 5.8. After the application of $+4$ V to the area enclosed by the first black square, in Figure 5.8(b) the device conductivity reaches a level above the maximum of the current amplifier as in Figures 5.7(b,d) despite the different conductivity in the initial state. Moreover, by applying -4.5 V, it was possible to annihilate the conduction path and reach a resistance value lower than the initial state, with a final current value under the detection limit in Figure 5.8(c). The complete reset highlights the high control on the HRS that can be attained with nanoscale devices, which is at the basis of the ON/OFF window opening previously observed in nanoscale systems [11].

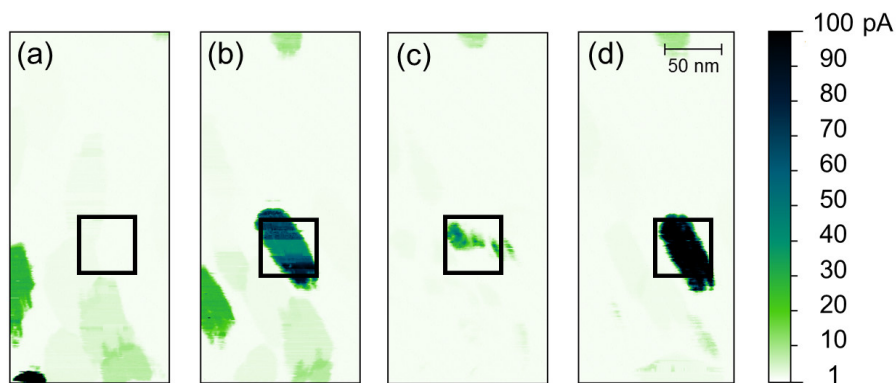


Figure 5.7: Current maps (0.5 V bias) acquired before the switching processes (a), after the set process with $+4$ V (b), after reset with -3 V (c), and after set with $+4$ V (d). The black square, containing a single nanodevice, encloses the area where the tip was scanned with $+4$ V/ -3 V to induce the set/reset transitions. The elongated shape of the metal electrodes is an artifact caused by a drift in the scanning system. Reprinted from [5].

5.3.3 Crosstalk observation between distinct nanodevices

In Figure 5.8, another interesting aspect is visualized. The two conductive devices on the left side of Figure 5.8(a), labeled A and B for convenience, share the same initial current value of 15 pA. After the application of a potential difference to the device enclosed by the black square (A), the not selected device at the bottom left (B) was also influenced (Figure 5.8(b)). This crosstalk effect between distinct devices at a distance of 75 nm happened again during the reset operation, when both devices reached a resistance value higher than the initial state. It is worth noting that devices A and B are not nearest neighbors, otherwise they would appear contiguous as in Figure 5.4(b). Additionally, the pitch is fully compatible with the presence of an additional electrode in-between the two nanodevices. Other nearest neighboring devices were unaffected during both set

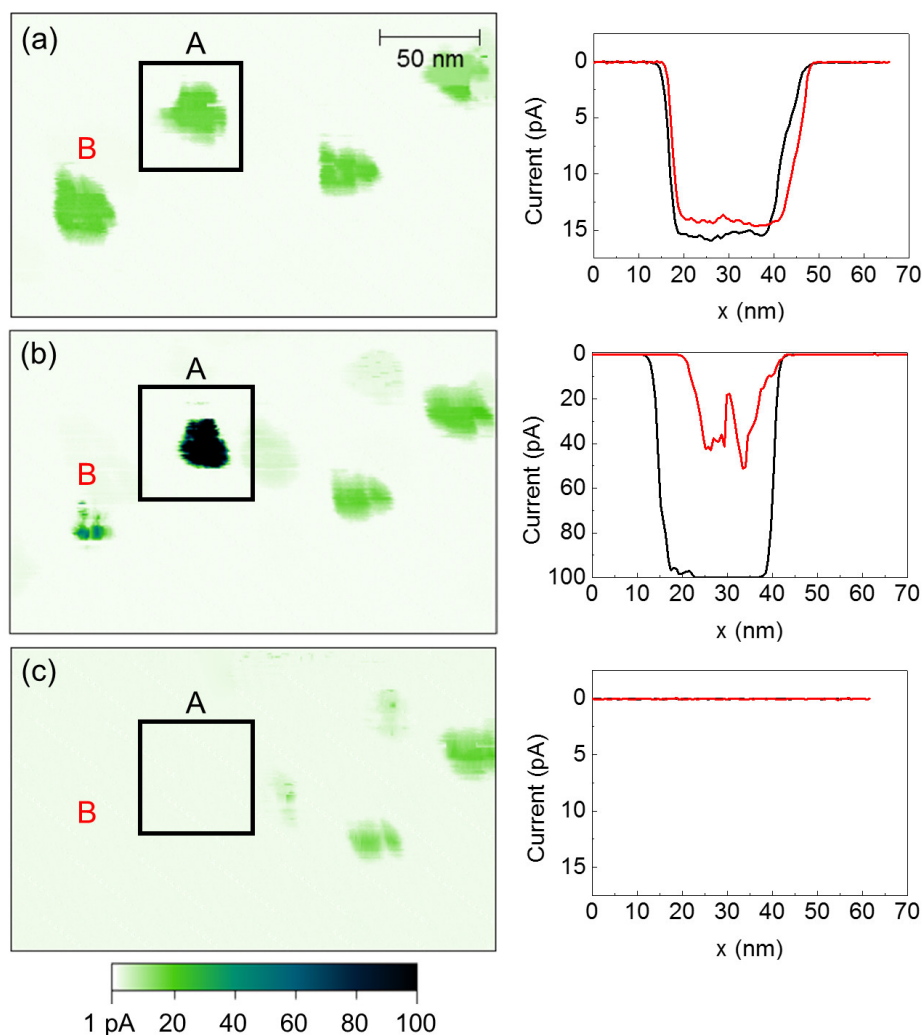


Figure 5.8: Current maps (0.1 V bias) acquired before the bipolar voltage operation (a), after set (b), and after complete reset (c). To induce the set and reset processes, the tip was scanned in the area enclosed by the black squares with a constant applied bias of +4 V (set) and -4.5 V (reset). On the right, line scans of the device to which the bias was applied (A, in black) and of the correlated device (B, in red). Reprinted from [5].

and reset operations, demonstrating that the observed crosstalk cannot be ascribed to the tip contacting many devices at the same time. Two other devices visible in Figure 5.7 at a distance of 80 nm and 130 nm were also unaffected, while a slight lowering in their conductance from Figure 5.7(a) to Figure 5.7(c) can be ascribed to the tip coating wearing out.

A similar crosstalk phenomenon was previously reported in the bare HfO_2/TiN stack using the conducting C-AFM tip as a mobile top electrode scanning the surface by Brivio et al.[12]. After forming, distinct conductive spots appeared in the scanned region, while

the following reset of one spot influenced the neighboring ones. The observed phenomenon was explained with the formation of bunches of connected conductive filaments during forming.

In the present case, we adopted an array of fixed devices instead of a mobile scanning electrode, with the C-AFM tip contacting only one device during forming. The presence of connected filaments should therefore be intrinsic of the HfO_2/TiN stack, as also indicated by the reinforcement of both devices after forming in Figure 5.8(b).

Basic model of crosstalk The mechanism behind the observed crosstalk effect deserves further considerations in order to achieve a plausible description of the physics of the system during the set/reset operations. Thermal profile simulations recently pointed out the thermal crosstalk, rather than the filament size itself, to be the ultimate limit for device scaling [13]. However, in our system, we can exclude thermal crosstalk to be the cause of the linked switching behavior. Indeed, a second neighboring device was affected, while no nearest neighbors were influenced. Additionally, the crosstalk phenomenon is observed even during the set transition, which is mostly electric field-induced and can not be effectively driven by a pure thermal process. Furthermore, in a homogeneous dielectric medium the stray electric field does not extend much beyond the contacted electrodes and consequently a mere effect of the stray electric field isotropically extending out of the device A volume is not reasonable. Moreover, in this hypothesis also the first neighboring cells would be affected by the stray electric field during switching operations.

The experimental evidence indicates that the cells A and B are characterized by a similar leaky conduction through the oxide in the initial state in Figure 5.8(a). Therefore, they are already connected to the underlying TiN electrode, *i.e.* an electrical circuit is already in place in the dielectric film. Furthermore, since the set and reset processes operated on device A lead to a conductance increase/decrease also of the unselected device B, the two devices are likely to share a common portion of the filamentary conduction paths, which is modified during set and reset operations and is responsible for the crosstalk effect.

The physical origin of the observed connection among distinct nanodevices, and the localization of the connected filamentary paths, should be sought in the structure and morphology of the insulating stack where the RS occurs. Brivio et al. [12] suggested that the origin of the localized conduction paths can be located at the highly defective HfO_2/TiN interface, in which the TiN morphology and its oxidation behavior are also likely to play a role. In this respect, it is worth discussing our system in more detail. The bottom TiN electrode is composed of columnar crystalline grains extending throughout the film thickness, as evidenced by the AFM surface morphology and corroborated by the SEM cross sectional image reported in Figure 5.9. The height–height correlation function (HHCF) extracted from the AFM maps, which gives an estimation of the average grain dimension, returns a value of 17.4 ± 0.7 nm. Yet, grains with lateral size up to 40 nm are clearly visible in both the AFM and SEM data. The surface root mean square roughness (RRMS) is equal to 1.57 ± 0.04 nm. This value is slightly lowered to 1.46 ± 0.08 nm upon exposure to 300 °C in air. These conditions are representative of the ambient experienced by the sample when it is introduced in the ALD chamber for the growth of the HfO_2 film. In particular, the smoothing of the TiN film upon air exposure is related to the oxidation of the TiN surface that results in the formation of a thin TiO_x layer. The oxidation behavior is reported to follow a logarithmic growth law which rapidly reaches the saturation

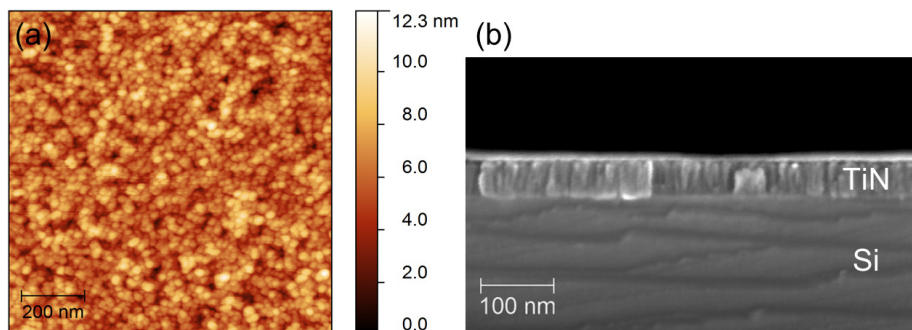


Figure 5.9: (a) Morphological characterization of the TiN surface performed upon oxidation in air by AFM operating in tapping mode. (b) SEM cross section of the $\text{HfO}_2/\text{TiN}/\text{Ti}/\text{Si}$ stack. The TiN grains extend throughout the film thickness. Reprinted from [5].

thickness, with the vertical columnar boundaries acting as fast diffusion paths for the oxygen species [14, 15]. According to XPS analysis reported in chapter 3, a TiO_2 oxide film of 2 – 3 nm is formed, and the presence of a TiO_xN_y component was evidenced as well. As a result of this oxidation process, an $\text{HfO}_2/\text{TiO}_x$ bilayer oxide is formed on top of the TiN electrode. It is interesting to note that the HfO_2 deposition performed by ALD forms an amorphous and uniform film conformal to the underlying surface. Conversely, the morphological and chemical structure of the TiO_x layer is strongly influenced by the TiN nanocrystalline structure.

To summarize, the dielectric stack where the resistance switching takes place is composed of a non-homogeneous dielectric with leaky paths that are already present in the initial state, and a defective TiO_xN_y layer at the interface between the HfO_2 layer and the TiN bottom electrode.

Regarding the HfO_2 /top electrode interface, it is worth to mention that the Ti layer inserted in the Pt/Ti top electrode is reported to lower the oxygen vacancies (V_O) formation energy in the HfO_2 film [16]. However, for the gettering layer thickness used in this work (4 nm), we can exclude the establishment of an asymmetric V_O profile or a V_O reservoir next to the top electrode in the HfO_2 film. Indeed, for thick (~ 10 nm) gettering layers, the switching polarity is opposite to the one observed in the present case. Apart from this, the Ti interlayer is expected also to act as an oxygen diffusion barrier, limiting oxygen outer diffusion through the Pt top electrode during the switching operation [17]. Furthermore, the Ti layer improves the Pt electrode adhesion, which is essential for repeated AFM tip scans. Finally, we can exclude a role of the top electrode and of its interface with the HfO_2 film in the crosstalk mechanism due to its limited lateral extension, since it is patterned by BCP-assisted lithography.

On the basis of this detailed structural/compositional analysis of the nanodevices reported above, Figure 5.10 provides a pictorial view illustrating the structure of the system and the corresponding electrical diagram to elucidate the physical model accounting for the observed phenomena.

Electrodes A and B, which exhibit a crosstalk phenomenon as shown in Fig 5.8, are placed in correspondence of low resistance paths (thin-line resistors), while electrode C exhibits a much higher resistance (thick-line resistor), due to the nanoscale non-homogeneity of the of the HfO_2 . Further, taking into account also the discussed non-

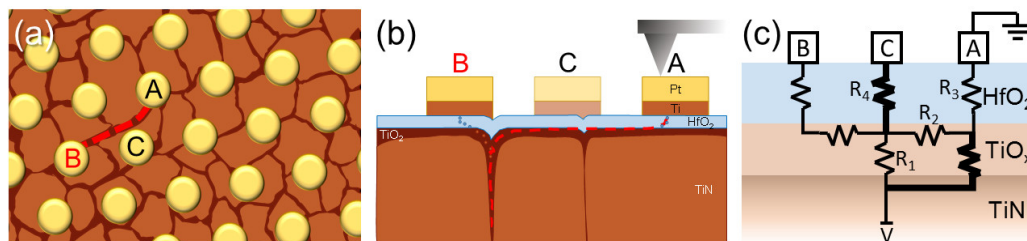


Figure 5.10: Pictorial view of the correlated switching for two different devices. (a) Plane view of the periodically patterned electrodes on top of the $\text{HfO}_2/\text{TiO}_x/\text{TiN}$ structure. (b) Cross section representing the current path along the grain boundaries. (c) Electrical schematic diagram illustrating the resistance network responsible for the crosstalk between devices A and B. The thin-line resistors correspond to low resistance paths, while the thick-line resistors are representative of a much higher resistance. Reprinted from [5].

homogeneity of the interfacial TiO_x dielectric layer, electrodes A and B are connected to the common TiN bottom electrode through a network of resistors that follow the lowest resistance paths and share a common portion of the path, depicted as R_1 .

During the set operation, when a positive potential difference is applied between the bottom electrode and the electrode A, a filament reinforcement takes place in the $\text{HfO}_2/\text{TiO}_x$ stack [18, 19]. At the beginning, most of the voltage is dropping across the highly insulating HfO_2 layer, where V_O^{q+} are formed preferentially along the already present leakage conduction path due to joule heating and to the high electric field [20, 21], while the oxygen species (O^{q-}) are drifted toward the bottom electrode, where they can easily diffuse along the TiN grain boundaries and can be stored. Once a filament is established in the HfO_2 layer, resulting in a significant variation of the layer resistance (R_3), most of the electric field will drop across the TiO_x , leading to a resistance change also in this layer. This finding is reported in literature for many bilayer structures [22], and a thin layer of 2.5 nm of oxidized TiN was also reported to exhibit resistive switching properties [23]. The location of this additional filament portion depends on the TiO_x chemical, electrical, and morphological profile [24] and will be favored in correspondence of defective sites. In particular, the TiO_x layer is expected to exhibit a higher conductivity in correspondence of the former grain boundaries of the underlying TiN electrode [25, 26], which can efficiently exchange oxygen species and promote the filament formation. Therefore, the locally non-homogeneous TiO_x interfacial layer provides preferential, non-trivial low resistance paths that allow lateral current flowing. Along the route of the maximum current, electrochemical processes are most likely to occur, leading to a switching in resistance for the series of resistors (R_2, R_1) connecting electrode A and the TiN bottom electrode.

After the set operation on device A, when the current is measured grounding electrode B (electrode A is floating), the reading current map of Figure 5.8(b) displays an increase in conductivity also for device B. This latter finding can be explained by the current path passing through the common resistor R_1 , whose resistance was changed during operation on device A. Conversely, other devices which did not show any relevant initial leaky current in the HfO_2 , including the nearest neighboring cells of device A, remain insulated by a locally sturdy HfO_2 layer and do not show any relevant change in resistivity since the resistance R_4 dominates all the other resistances in the connecting network.

Finally, during the reset operation on device A, with the application of an opposite voltage polarity, the O^{q-} ions stored along the TiN grain boundaries diffuse upwards and recombine with the V_O^{q+} , oxidizing the common lower portion of the filament and interrupting the conduction path for both the devices through an increase of resistance R1.

5.3.4 Concluding remarks

The results discussed above raise important questions about the real extension of the conductive filaments. Several direct experimental evidences in the HfO_2/TiN film highlighted a spatial extension in the deca-nanometers range [27, 28]. Our data indicate that the presence of large grain boundaries in the oxidized TiN can extend the filament region even more. This consideration calls into question all the system scales in ultra-high density arrays like the one we have been testing. Even if functional devices down to 10 nm have been demonstrated [3], at the current stage it is impossible to exclude that the conductive filaments could extend beyond the limits of the single cell or that lateral sneak paths due to memory stack non-homogeneities can cause a potential crosstalk issue in ultra-high density memory arrays.

In this experiment, the crosstalk was observed between two devices already showing a certain degree of conduction in the initial state. If however we envisage to form all the devices in the array, the presence of sneak paths in the underlying film can become a severe issue, with two or more devices being influenced by an adjacent one in case of a low resistance path is established between neighboring devices as depicted in Figure 5.10. This phenomenon can arise whenever the spacing of the device array becomes comparable to the intrinsic defectivity length of the materials in the memory stack.

In conclusion, the observed effect is the result of localized leaky paths in the HfO_2 film in combination with a switching layer located at HfO_2/TiN interface, where the intrinsic defective and non-homogeneous structure gives rise to lateral conduction along low resistance sneak paths.

The TiO_x which forms at the upper TiN interface is in general unavoidable, owing to the exposure to an oxygen-rich ambient and to the ALD deposition process. At the same time, the general features of the TiN film, including the polycrystalline morphology, are commonly encountered among different deposition techniques and are not limited to the sputter deposition method [29]. It is worth noting that the HfO_2/TiN stack is currently widely adopted among the best performing devices found in the literature, as both materials are very well integrated in the Si-based IC processes [30].

The observed crosstalk is expected to occur in memory architectures in which a lateral physical connection exists between different devices. The integration of a continuous oxide film or electrode is however of crucial importance in many recent prototype applications of highly scaled RS devices, based on both planar technology [31] or on a three-dimensional integration [32–34]. In the latter case in particular, the near proximity of the stacked cells make them particularly vulnerable to the crosstalk issue and it must be considered during the structure design. While the oxide/electrode patterning would provide a possible solution, it is responsible for a variety of additional issues related to the etching procedure and encapsulation [35], and is hardly applicable in case of stacked integration of vertical RRAM devices.

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Future outlook: oxide RRAM patterned by sequential infiltration synthesis

6.1 Introduction

Block copolymer (BCP) can self-assemble in nanoscale periodic patterns upon phase separation. However, for a useful implementation of the created patterns, the BCP features need to be transferred to the required material. In Chapter 4, this task was accomplished using nanoporous templates based on PS-*b*-PMMA BCP in which the PMMA domains were selectively removed and a lift-off process after metal deposition. With this process it was possible to produce ordered arrays of Pt/Ti metal nanoparticles with lateral dimension down to 12 nm and density up to 1.5×10^{11} particles per cm^2 on top of HfO_2/TiN films [1]. These regular arrays were used as nanosized metal electrodes and contacted by conductive atomic force microscopy (C-AFM) to probe the resistive switching phenomenon at the nanoscale [2]. The testing devices were based on a simple structure constituted by continuous switching oxide and bottom electrode films. Yet, the fabrication method allowed to produce functioning devices and the produced structure was representative of actual configurations such as three-dimensionally stacked devices [3]. Nonetheless, for practical nanoscale applications also the switching oxide needs to be patterned and a study of the resistance switching phenomenon as a function the oxide lateral dimension down to a few nanometers is required. Patterning of the switching material seems also a requisite necessary to avoid the crosstalk between two different devices which was evidenced in Chapter 5 during resistance switching in the very high density array fabricated by BCP templates on a continuous HfO_2/TiN film. In this respect, it would be particularly intriguing to exploit bottom-up approaches for the fabrication of patterned oxides in order to conceive novel integration approaches and study the switching phenomenon down to extreme scales.

Among the bottom-up techniques presented in Chapter 2, BCP-based patterning emerges as one of the most promising methods for technology nodes down to 5 nm when applied in combination with top-down techniques for a precise positioning of the patterned features. PS-*b*-PMMA is the most applied BCP due to its flexibility and easy of application. However, this all-organic BCP poses several challenges during pattern transfer processes. In the first place, pattern transfer by lift-off entails several limitations, not secondarily a limited aspect ratio of the defined structures. Moreover, during dry etch the PS and PMMA domains possesses a poor etch selectivity. A workaround would be to transfer the BCP mask to an intermediate hard mask. This solution however further complicates the patterning process. The best method would be to avoid the

pattern transfer process and directly transform one of the two domains in useful nanostructures of the required material.

Darling and coworkers [4, 5] first exploited chemically reactive sites present only in one of the BCP domains for a domain-selective reaction. This technique, called sequential infiltration synthesis (SIS), may use selected pairs of precursors developed for the atomic layer deposition (ALD) method. During SIS cycle, one precursor first interacts with only one of the self-assembled domains of the BCP template. Then, the second precursor completes the growth cycles and selectively modifies the BCP domain. SIS technique is able to convert self-assembled polymeric templates into inorganic material, which do not suffer from limitations connected with soft materials. Moreover, with SIS method selected materials can be directly patterned, thus avoiding the pattern transfer process [6–10]. As an example, this method was applied for enhancing the contrast of the BCP domains in transmission electron microscopy, making possible the observation of their three-dimensional structure [11].

In this work, we exploit the selective presence of reactive sites (carbonyl groups) only in PMMA domains for a SIS process based on trimethylaluminum (TMA) and H_2O precursors in an ALD reactor. This process leads to the formation of aligned alumina nanowires from a self-assembled BCP template. The results highlight the possibility to obtain aligned alumina nanowires with lateral width down to 7 nm and center-to-center distance of 26 nm. In addition, the dimension of the nanowires can be finely tuned by adjusting the number of the processing steps. Concerning the oxide properties, XPS analysis on the alumina nanostructures evidences the presence of mainly Al^{3+} valence bonds ascribable to Al_2O_3 stoichiometry.

The oxide nanostructures produced in this way can be used as hard mask for a subsequent pattern transfer process. However, the most advantageous way to exploit this innovative patterning method would be to directly make use of the oxide nanostructures in an appropriate device scheme. Indeed, the final aim of this project is to integrate the bottom-up parallel alumina nanowires with metal electrodes defined by top-down electron beam lithography (EBL). This allows to study the resistive switching phenomenon in devices in which the switching oxide has been patterned in both lateral and vertical directions down to extreme scales.

One of the advantages of SIS technique is that it can make use of reagents employed for ALD growths that are already widely tested and available on the market. However, an important aspect to be considered is the thermal compatibility of the process with the self-assembled BCP template. We chose to perform the first SIS tests using TMA+ H_2O precursors since this process allows to obtain Al_2O_3 nanostructures with good material properties at relatively low temperature (below 100°C) [12]. Even if SIS technique is still in its infancy, the applicability of other ALD precursors was demonstrated in the literature for the production of various materials like SiO_2 , TiO_2 , ZnO , and even tungsten metal [4–6]. Many of these materials are of potential interest for an application in RRAM devices. As future prospects of the ongoing project, other materials like HfO_2 , TiO_2 , and ZrO_2 will be tested along with their possible integration in nanoscale RRAM devices.

In conclusion, the development of SIS technique is of high interest for many future integration schemes combining bottom-up and top-down approaches. The direct patterning of functional materials as well as contacting metal electrodes can pave the way for high density integration of many electronic devices beyond current limits imposed by lithographic and patterning techniques.

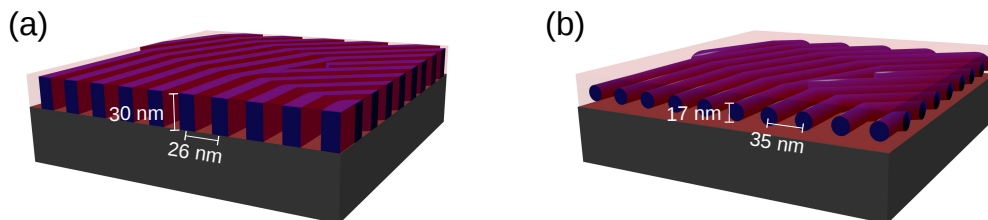


Figure 6.1: Schematic representation of perpendicular lamellae (a) and parallel cylinders (b) obtained by BCP self-assembly. Also indicated are the average spacing and height of the features produced with the two BCPs used in this study.

6.2 PS-*b*-PMMA block copolymer templates

Before SIS, block copolymer films were spin-coated on substrates containing native silicon oxide or thermal oxide and self-assembled by thermal treatment in a rapid thermal processing (RTP) machine. In order to remove any organic residual and increase the density of hydroxyl groups at the surface, the oxide substrates were treated in Piranha solution as previously described in Chapter 4. Two types of PS-*b*-PMMA BCP were selected in order to produce either lamellar or cylindrical domains.

Perpendicular lamellae A symmetric BCP with molecular weight (M_w) of 51 Kg/mol from Polymer Source Inc. was spin-coated from a solution of 8 mg in 1 mL of Toluene.

In order to induce the perpendicular orientation, a layer of random copolymer (RCP) of 8 nm was spin-coated and grafted at hydroxyl groups present on the substrate prior to BCP deposition, removing any preferential wetting of the SiO₂ surface by one of the two polymer blocks. Additional details about SiO₂ and HfO₂ surface neutralization by RCP can be found in Chapter 4.

The self-assembly was induced by thermal treatment at 290°C for times up to 1 min. Processing parameters were selected to maximize the correlation length (the average length over which the parallel orientation of the lamellae is conserved) yet avoiding a degradation of the polymer. A detailed analysis of the effects of temperature and processing time on the ordering process can be found in ref. [13].

A sketch of the self-assembled lamellae is reported in Figure 6.1(a). The average spacing measured from the first peak of the 2D Fourier transformation of SEM images is 26±0.1 nm, while the height of the lamellae is determined by the film thickness of about 30 nm. The symmetric content of PS and PMMA components determines a similar dimension of both domains corresponding to 13 nm (half the average spacing).

Parallel cylinders An asymmetric BCP with 0.7 Polystyrene volume fraction and M_w of 67 Kg/mol (Polymer Source Inc.) was spin-coated from a solution of 9 mg in 1 mL of Toluene.

Upon thermal treatment, PMMA cylinders self-assemble inside the PS matrix. For parallel cylinders, no surface neutralization is required since PS wets preferentially the SiO₂ surface, thus no RCP layer is needed in this case. Nevertheless, as previously noticed in chapter 4, the film thickness needs to be tuned in order to deposit a single layer of parallel cylinders (film thickness must be commensurate to the lattice spacing of the

adopted BCP domains). The BCP film thickness can be varied either by changing the density of the solution or the speed of rotation during spinning. In this case, a careful calibration of the density of the solution resulted in a single layer of parallel cylinders throughout the sample surface.

The thermal treatment was performed at 250°C for 5 min. In this case, no specific calibration of the annealing parameters was performed and the correlation length was quite limited. However, this does not hinder any further consideration about the SIS process since it does not depend on the value of the correlation length.

As shown in Figure 6.1(b), the average spacing obtained with the M_w of 67 Kg/mol is about 35 nm, while the diameter of the cylinders is about 17 nm. Both spacing and diameter depend on the BCP M_w . A detailed analysis of the produced dimensions as a function of the M_w for cylinders-forming BCP can be found in ref. [14].

Comparing perpendicular lamellar structures with parallel cylinders, both have their strengths and weaknesses. As shown in Figure 6.1, lamellar features have a higher aspect ratio. Even if the chosen M_w of the BCP for cylinders is higher than for lamellae, the height of the features is much smaller. On the other hand, cylinders benefit from the absence of any RCP wetting layer. Since also the RCP contains reactive sites, during SIS this layer is partially transformed in inorganic oxide and an etching process is required to remove this unwanted material between alumina nanowires. The effect of SIS on the RCP is discussed in section 6.3.5.

Apart from the aforementioned peculiarities, many of the results reported in this chapter for the SIS process can be applied to both structures. In the following section, a study of the SIS parameters is conducted using lamellar structures as testing ground because of their great relevance in many possible applications. In Figure 6.2 lamellar features are portrayed before and after SIS. After the initial process optimization with BCP perpendicular lamellae, the study is proceeding in parallel with BCP self-assembling in perpendicular cylinders. A first results on cylinders is reported at the end of the section.

For a rapid and simple testing of the SIS process, un-patterned substrates were used. In these substrates, self-assembly proceeds in a random fashion and the parallel cylinders or lamellae have random orientation. In case that a specific placing and orientation of the produced features is required, the BCP self-assembly can be externally driven by a pre-patterned substrate in a procedure called templated (or directed) self-assembly (TSA). This method was introduced in Chapter 2 and discussed in detail in Chapter 4. It is worth noting that the SIS results reported in this chapter for BCP on un-patterned substrates can be easily extended to TSA samples.

6.3 Sequential infiltration synthesis in PS-*b*-PMMA block copolymer

Sequential infiltration synthesis (SIS) was performed in a Savannah 200 reactor (Cambridge NanoTech.) using a semi-static mode. In this particular operation mode, the outlet valve was closed during exposure to precursors in order to maintain a constant environment and give time to the alternating precursors to diffuse inside the polymer film. First, samples containing self-assembled PS-*b*-PMMA BCP films were inserted in the ALD reactor and the chamber was evacuated down to a base pressure of 20 mTorr. The samples were then thermalized and excess moisture was removed under N₂ flow (100 sccm) for 30 min at the same temperature set for the following SIS process. During exposures to TMA and H₂O precursors, the chamber was sealed and a sufficient time

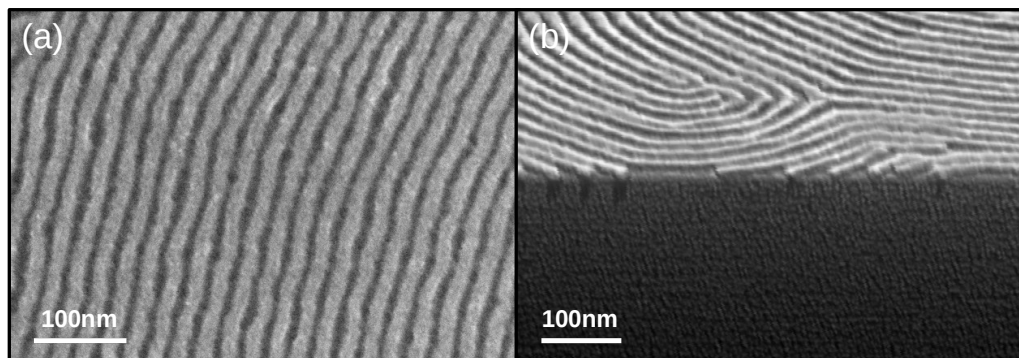


Figure 6.2: (a) SEM plane view of BCP perpendicular lamellae after self-assembly. (b) SEM tilted view of alumina nanowires formed after 5 SIS cycles from perpendicular lamellar structures.

was awaited to allow for precursor diffusion and incorporation inside the polymer matrix. Each cycle was composed of a first exposure to TMA for 60 s, a purge step of 60 s in N_2 flow (100 sccm), an exposure to H_2O vapor for 60 s to complete the alumina reaction, and a final longer purge step of 300 s in N_2 flow (100 sccm). Finally, an oxygen plasma process at 50 W was performed in order to remove organic components remained after SIS.

The main parameters that can be easily controlled during the SIS process in the ALD reaction chamber are the vapor pressures of the two precursors, the exposure times, and the duration of the purge steps. In addition, the process temperature has a deep influence on the kinetic of the reaction between TMA and water molecules and can affect the polymer morphology [15]. Finally, keeping constant all the other parameters, the number of SIS cycles has a mayor impact on the final morphology of the alumina nanowires obtained after polymer removal [4].

6.3.1 Effect of temperature

Temperature is fundamental parameter affecting ALD growth. A temperature between $85^\circ C$ and $90^\circ C$ is usually applied for SIS processes in order to avoid any perturbation of the self-assembled polymeric template [4–6]. Despite $90^\circ C$ is still within the ALD growth window for the highly reactive TMA precursor [12], higher temperatures would be beneficial for the quality of the produced Al_2O_3 material. Unfortunately, PS-*b*-PMMA can not withstand temperatures higher than the degradation temperature, while a temperature higher than the melting point T_m (about $130^\circ C$ for the PMMA alone [16]) would likely lead to a disappearance of the regular pattern.

For what concerns the SIS process, temperature plays a significant role in determining the diffusion and desorption of the precursors inside the polymer and the speed of the reaction between TMA and reactive sites. In particular, TMA and H_2O diffusion should accelerate above the glass transition temperature T_g (about $103^\circ C$ in lamellar forming BCP with M_w of 50 Kg mol^{-1}) [15].

Figure 6.3 shows the evolution of the produced alumina nanowires after one SIS cycle (TMA pressure 6 Torr after pulse; H_2 pressure 2 Torr) as a function of the processing temperature. For these TMA and water pressures, at $90^\circ C$, after one SIS cycle alumina

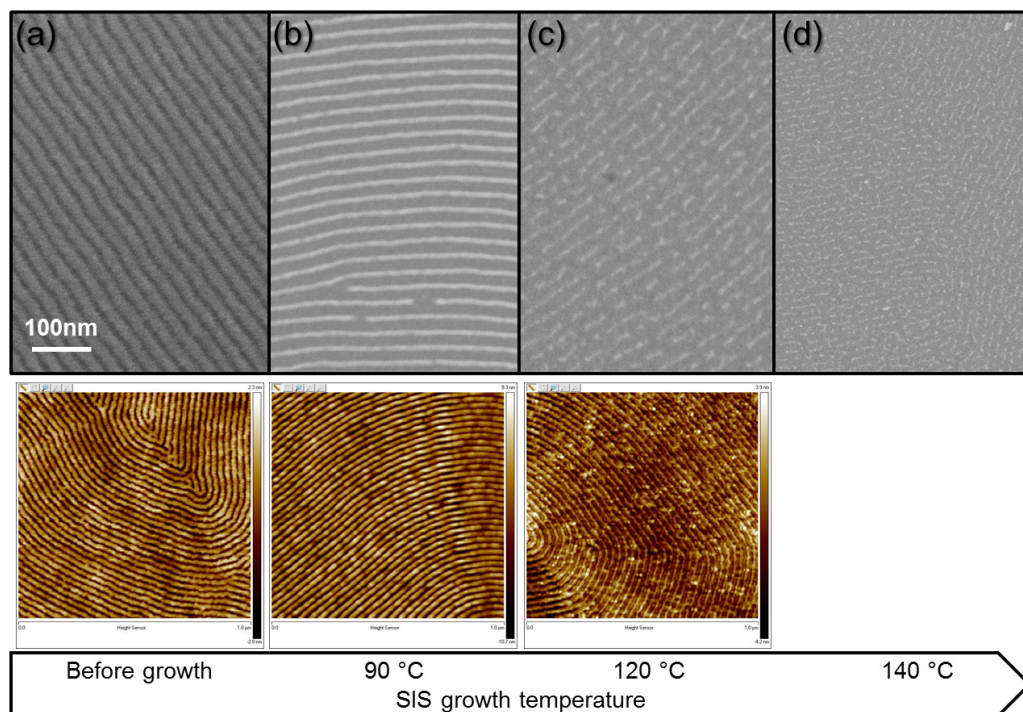


Figure 6.3: Evolution of the lamellar domains before (a) and after ALD sequential infiltration synthesis at increasing temperatures (b–d). Above, SEM images. Below, AFM images (frame edge 1 μm). AFM analysis for the growth at 140 $^{\circ}\text{C}$ was not performed since lamellae were visibly degraded after process.

nanowires have an average width of 5.9 ± 0.3 nm and height of 3.4 ± 0.7 , as determined by SEM and AFM analysis, respectively. At 120 $^{\circ}\text{C}$, nanowires start to disconnect and SEM images indicate an average width of ~ 5 nm, while the average height is 3 ± 1 nm, as determined by AFM measurements. Further increasing the temperature at 140 $^{\circ}\text{C}$ results in an almost complete disappearance of the nanowire features. These results are in agreement with an increased desorption of TMA molecules above 120 $^{\circ}\text{C}$, which is above T_g for the applied BCP [15, 17], while the almost complete disappearance of regular features above 140 $^{\circ}\text{C}$ can be attributed to temperature exceeding T_m .

Although SIS temperature alone is expected to have an impact on the nanowires morphology, also water pressure can determine the morphology of the produced alumina nanowires, and there could be an interplay between the two contributions. For this reason, a second test at 120 $^{\circ}\text{C}$ was performed reducing the water pressure from 2 Torr to less than 1 Torr (Figure 6.4). At lower water pressure, better connected nanowires can be obtained: the average width increases from ~ 4.7 nm to 6.6 ± 0.4 nm, a value comparable with nanowires produced at 90 $^{\circ}\text{C}$. Nonetheless, the features still present a more pronounced line roughness and many points of disconnection, remarking an effect of temperature irrespective of the water pressure.

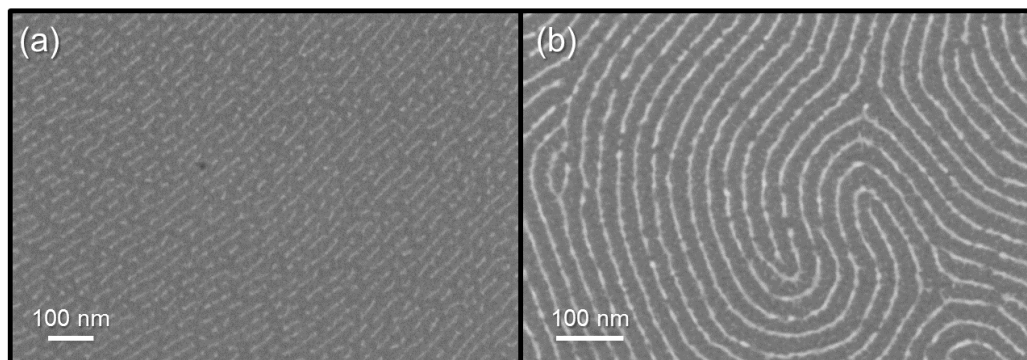


Figure 6.4: SEM images of PS-*b*-PMMA lamellae treated with one SIS cycle at 120°C. The water pressure reduced from 2 Torr (a) to less than 1 Torr (b).

6.3.2 Effect of precursor pressures

Water pressure

The amount of water vapor during SIS was found to have a great influence on the final structure of the alumina nanowires. Figure 6.5 shows the pressure inside the chamber during a complete SIS cycle for two different processes performed at 90°C with the same conditions except a different water pressure. The different amount of water in the chamber was controlled by adjusting the time width of the water pulse (0.3 s for the higher pressure, in blue, and 0.2 s for the lower pressure, in light blue). For the higher water pressure, the alumina nanowires shown in Figure 6.5(b) are disconnected in many points and have a less regular alignment. On the contrary, a reduction of the water exposure improves the nanowires morphology as shown in Figure 6.5(c). Regarding the measured width, alumina nanowires fabricated with the lower water pressure have a slightly wider width but compatible within the uncertainty: 6.5 ± 0.5 nm compared to 5.9 ± 0.3 nm. In summary, water pressure should be kept low enough to avoid a breakage of the nanowire structures. A pressure around 1 Torr was found to produce the best morphology.

The degradation and disconnection of the lamellar features in presence of higher water pressure could be related to the oxidizing environment that establishes in the chamber during the water exposure and possibly degrades the polymeric film. Further investigation is however required to fully ascertain the mechanism responsible for the nanowires morphology degradation.

It is worth to mention that repeating many H₂O exposure cycles, the internal water pressure inside the chamber slightly increases up to a saturation level. This happens in combination with a marked variation of the pressure decay curve after the H₂O pulse in semi-static mode. This is probably due to an absorption of water molecules by the interior of the steel chamber. Once that the saturation level is reached, an equilibrium establishes between water molecules absorbed and released by the chamber, and the pressure remains fairly constant during the whole exposure. An optimal control of the water pressure during SIS can be achieved by pre-conditioning the ALD chamber with repeated water pulses until a stable pressure is reached. This procedure becomes necessary contrarily to standard ALD processes due to the greater dependence of the semi-static mode on the chamber internal condition.

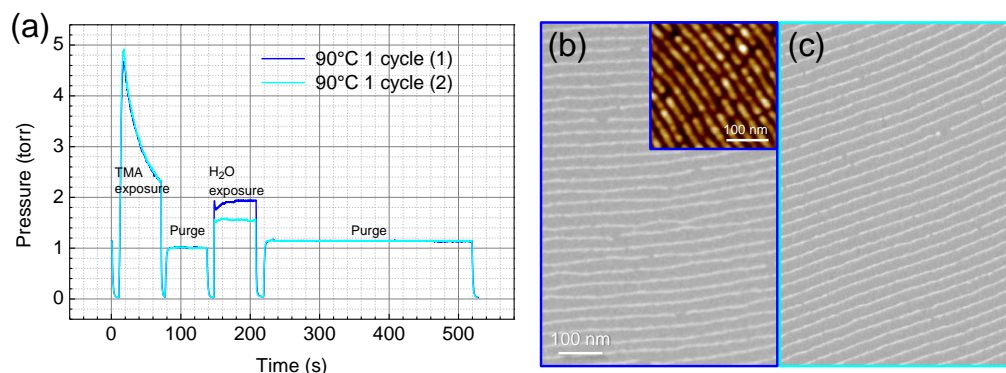


Figure 6.5: Comparison between two SIS cycles performed at 90°C with different water pressures. (a) Measured pressure in the reactor chamber during the whole cycle. (b) SEM image of Alumina nanowires obtained with the higher water dose. As inset, AFM topography from the same sample. (c) SEM image of Alumina nanowires obtained with the reduced water pressure.

TMA pressure

Considering now the effect of TMA pressure, the variation of this parameter was found to have a less evident impact on the morphology of the alumina nanowires. In Figure 6.6, two processes are compared with similar water pressures but TMA pressure varying of a factor two. The resulting alumina features shown in Figures 6.6 (b) and (c) have in both cases a smooth and continuous morphology, while the nanowires produced with the higher TMA pressure have a slightly larger average width of 7.1 ± 0.6 nm, still compatible with the average width of 6.5 ± 0.6 nm found for the smaller TMA pressure.

A possible explanation for the poor dependence on the TMA dose during the first SIS cycle can be related to a complete coordination of the available reactive carbonyl groups inside the PMMA domains with TMA molecules. Indeed, in case that a long enough time is given to the TMA molecules to diffuse throughout the entire thickness of the PMMA film[17], the number of reactive sites likely limits the maximum amount of infiltrated precursor. If this saturation limit is reached, any additional TMA dose does not translate in a significant mass uptake by the PMMA [16].

6.3.3 Study as a function of the number of SIS cycles

Starting from the untreated PS-*b*-PMMA lamellar domains shown in Figure 6.7(a), increasing the number of SIS cycles progressively enlarges the width of the obtained alumina nanowires. Figure 6.7 summarizes the obtained structures before SIS and after SIS at 90°C. This study was carried out with a water pressure around 1 Torr. After SIS, an oxygen plasma treatment was applied to remove carbon components, leaving only alumina nanowires on the sample substrate.

The adopted BCP film has a symmetric content of PMMA and PS components, thus the lamellar spacing of 26.0 ± 0.1 nm (as determined from the first peak of the Fourier transform of SEM images) translates in a PMMA width of 13 nm. Increasing the number of cycles leads to a progressive increase of the nanowires width in an almost linear fashion, while the spacing remains fixed within the measurement uncertainty. In this way, the width of the alumina nanowires can be finely tuned, and dimensions smaller

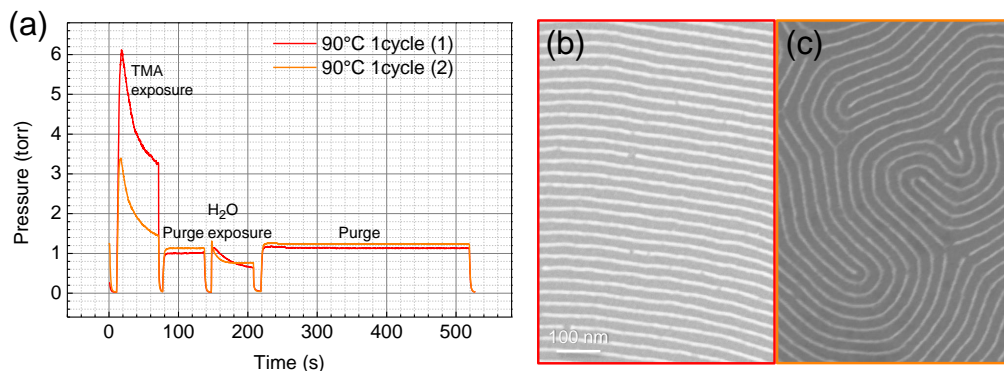


Figure 6.6: Comparison between two SIS cycles performed at 90°C with different TMA pressures. (a) Measured pressure in the reactor chamber during the whole cycle. (b) SEM image of Alumina nanowires obtained with the higher TMA dose. (c) SEM image of Alumina nanowires obtained with the reduced TMA dose. The lower correlation length of this latter sample does not impact the SIS study.

than the original template can be achieved. The average width and spacing of the obtained alumina nanowires are reported in Figure 6.8 as a function of the number of SIS cycles. One cycle is sufficient to produce nanowires with an average width of 7 ± 1 nm in optimal processing conditions, even if the average width also depends on the water pressure as described above. The average dimension then increases with the number of cycles and after 15 cycles reaches a value of 16 ± 2 nm, which is above the initial template width. In this latter case the formed structures appear wavy and not perfectly separated. It is therefore possible that the lateral growth starts to permeate the PS domains, leaving spurious material in between the infiltrated domains.

In order to determine the average thickness of the produced alumina nanostructure, two alternative approaches were applied. One way is to exploit AFM topography analysis. However, AFM tips can hardly span throughout the whole height of too close structures, causing an underestimation of the real height. For the topography tips used (10 nm curvature radius), this method can give reliable results only for lamellae infiltrated with no more than one cycle. Another approach is to determine the fraction occupied by the nanostructures from SEM images and then fit ellipsometry spectra (SE) using this data to obtain the height of only the alumina portion (Figure 6.9). First of all, a threshold was applied to SEM images and the area fraction occupied by lamellar features (f_L) was extracted. This step is facilitated by the fact that two well-distinguished peaks (one for the alumina structures and one for the background) can be usually distinguished in the intensity histogram, due to the high material contrast. Alternatively, f_L can be estimated from the average lamellar width (W_L) and spacing (L_0) using the formula

$$f_L = \frac{W_L}{L_0}$$

Afterward, the SE spectrum was fitted considering two contributions with fixed ratio, one for the void fraction and one for the alumina material. From this fit, the actual height of the alumina nanowires was determined with the only assumption of a perfectly square profile. This method, although indirect, can prove useful in case of close structures,

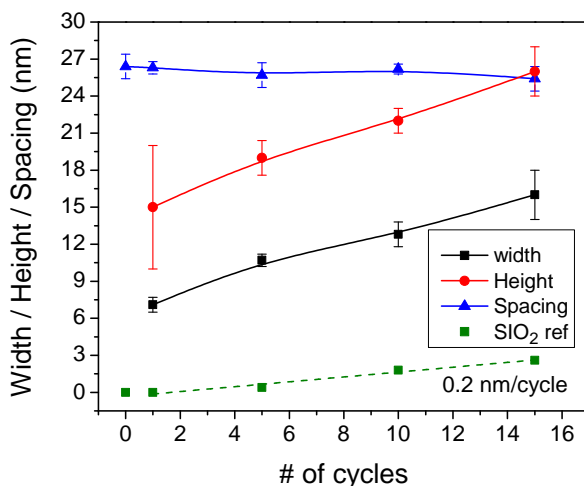


Figure 6.8: Width, thickness, and spacing of the lamellar domains after infiltration as a function of the number of SIS cycles. Width and spacing were determined from SEM images, while heights were estimated through SE fitting. SIS was carried out at 90°C with a water pressure around 1 Torr. In green, it is reported the Al₂O₃ thickness grown by standard ALD on a SiO₂ substrate inserted in the chamber for reference.

when AFM analysis finds its limit. It is worth to note that both AFM and SE methods gave very similar results in terms of both average values and uncertainties.

The average height derived by SE fitting is reported in Figure 6.8. The trend as a function of SIS cycles follows a linear increase similar to the one observed for the average width, while the higher value denotes an aspect ratio of roughly 2.

In Figure 6.8 the thickness of the Al₂O₃ film deposited on the SiO₂ substrate by standard ALD growth is inserted for comparison. The standard Al₂O₃ growth per cycle using TMA-based ALD process at 90 °C is only 0.2 nm/cycle, with an almost linear growth. SIS process proceeds in a different way. Instead of requiring many TMA and H₂O cycles, TMA fills the PMMA domains and bonds to chemically active sites in the bulk of the polymer, leading to a three-dimensional matrix which the subsequent water exposure turns into alumina. This leads to an offset at one cycle and to a higher growth per cycle of 0.7 nm/cycle.

6.3.4 XPS analysis of the nanostructured alumina

A survey of the XPS signal coming from alumina nanowires produced by 1 and 5 SIS cycle at 90°C and 1 cycle at 120°C (1 Torr water pressure) is reported in Figure 6.10. The visible peaks are clearly attributable to oxygen, carbon, silicon, and aluminum atoms. The analyzed system is composed of a double layer, with aluminum and part of the oxygen signal coming from the nanowire structures, while silicon and the remaining part of the oxygen signal are coming from the substrate.

For the SIS infiltrations at 90°C, a more detailed analysis of the high resolution spectra reveals a distance of 456.4 eV between Al2p peak and the O1s sub-peak related to Al–O bond. This value is coherent with stoichiometric alumina. Al2p peaks reported in Figure

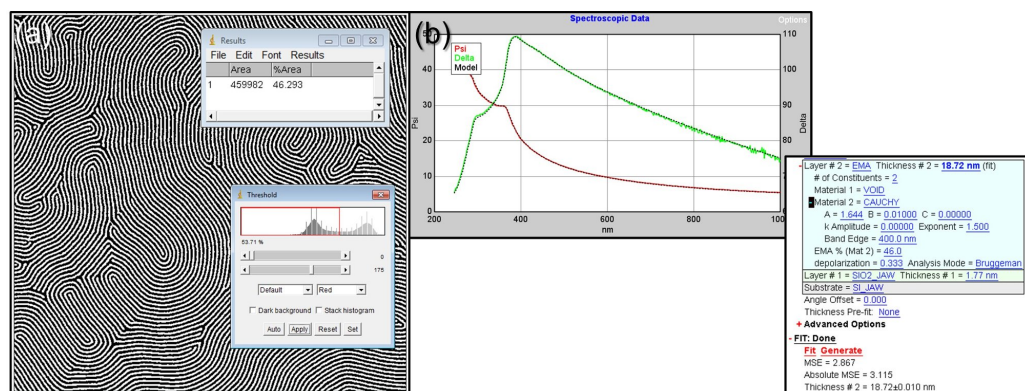


Figure 6.9: Procedure for the determination of the average height of the nanostructures. Sample data is referred to 5 SIS cycles. (a) SEM image binarized by threshold for the estimation of the area fraction of the alumina features. (b) Fit of the SE spectrum using void and Al_2O_3 components. A Cauchy model with typical optical constants was used for the alumina.

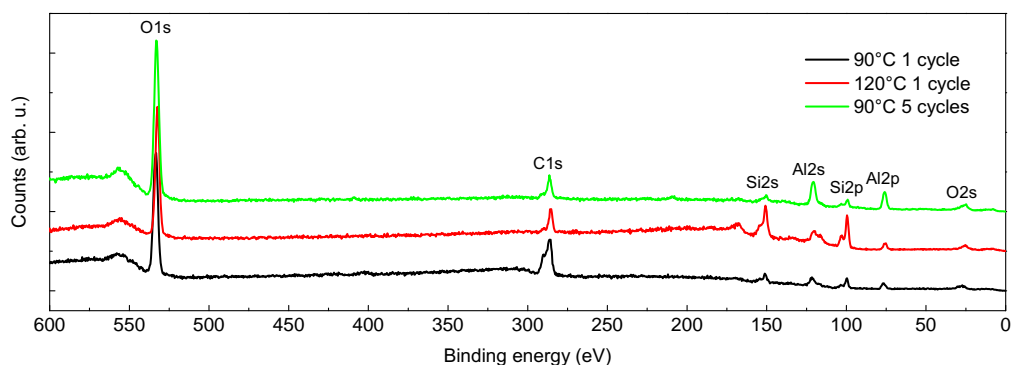


Figure 6.10: XPS spectrum surveys of alumina nanowires obtained from infiltration of PS-*b*-PMMA lamellae at 90°C (1 and 5 cycles) and 120°C.

6.11 can be fitted with a single peak of 1.8–1.9 FWHM. This width is only slightly above the value reported for pure and stoichiometric Al_2O_3 , probably due to charging effect or other non-idealities.

The comparison of the spectra acquired after 1 and 5 cycles in Figure 6.11 clearly reveals the increased amount of aluminum corresponding to additional cycles. The 3:1 ratio between the Al2p peak areas is compatible with the increased width and height dimensions after 5 cycles, while the no major variation of the alumina composition can be detected.

The same peaks can be observed in Figure 6.10 for samples infiltrated at 90 and 120°C. In the latter case the smaller Al2p peak width of 1.6 eV can be related to the lower height of the produced features (5.1 ± 0.8 nm, as determined by SE data fit), which causes a smaller charging effect. The lower height of the features also determines a lower Al peak and an increased signal coming from the silicon substrate, as clearly visible in Figure 6.10.

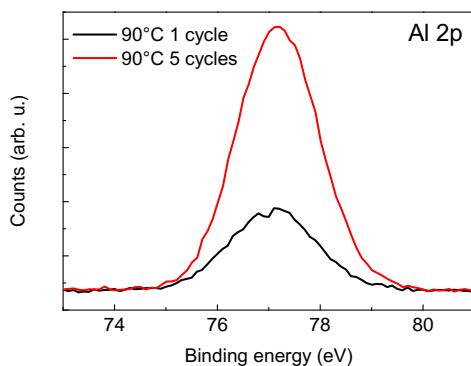


Figure 6.11: High resolution spectra of the Al₂p signals obtained after 1 and 5 SIS cycles at 90°C.

6.3.5 Sequential infiltration in random copolymer

The results above highlight the possibility to obtain highly periodic alumina nanowires. In order to obtain BCP lamellar domains with orientation perpendicular to the substrate, the SiO₂ surface should be neutralized and a layer of random copolymer was added for this purpose. The RCP layer contains MMA molecules, thus carbonyl groups are present also in this layer and can act as reactive sites for TMA trapping. With the final aim to produce disconnected oxide nanowires, it is necessary to investigate the effect of the SIS procedure on the RCP layer.

Two different RCPs were used in this study. One with a final thickness of 19.2 ± 0.5 nm after grafting and one with a grafted thickness of 6.9 ± 0.1 nm. After SIS at 90 °C for 1 cycle and oxygen plasma to remove carbon components, only ~ 0.7 nm were left on the surface in both cases. This means that after 1 cycle any alumina layer between nanowires is below 1 nm and can be easily removed by a short dry etching process which avoids excessive deterioration of the nanowires. On the other hand, infiltrating for 15 cycles the resulting alumina layer was ~ 10 nm for the thin RCP of 7 nm and ~ 15 nm for the thick RCP of 19 nm. These values are below the average height of the infiltrated lamellar structures after 15 cycles, however a long etching step would be required in this case to separate the alumina nanostructures [10].

6.3.6 Cylindrical structures

An cylinder-forming BCP with M_w of 67 Kg/mol was spun directly on top of the SiO₂ substrate to obtain a single layer of cylindrical domains oriented parallel to the sample surface.

Figure 6.12 displays the parallel cylinders before and after SIS at 90 °C for 1 cycle (~ 1.5 Torr water pressure). After removing carbon components using an oxygen plasma step, the alumina nanowires have an average width of 6.8 ± 0.4 nm, a spacing of 35 ± 3 nm, and an average thickness measured by AFM of 4 ± 1 nm. Starting from a cylinder-forming BCP, the final thickness of the alumina nanowires is below what can be obtained with lamellar templates. However, without any RCP layer no etching step is required to fully separate the produced features.

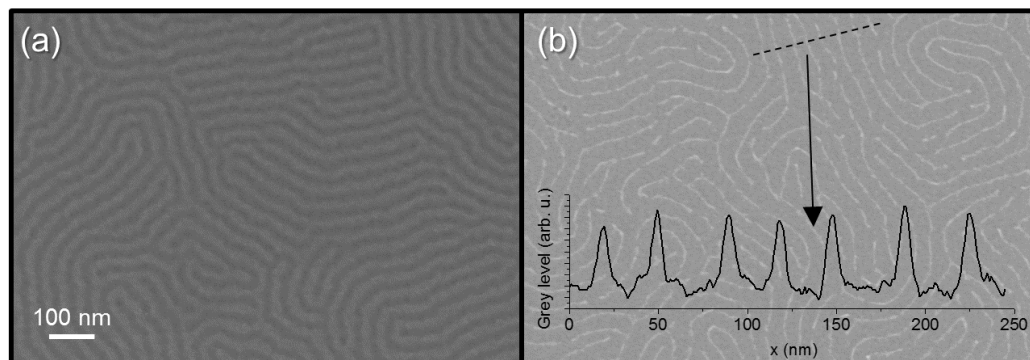


Figure 6.12: (a) PS-*b*-PMMA cylinders parallel to the substrate. (b) Alumina nanowires fabricated by SIS from PS-*b*-PMMA cylinders.

6.4 Perspectives

The study of the SIS method applied to BCP self-assembled templates highlights the possibility to define aligned alumina nanowires with an entirely bottom-up approach. The main parameters affecting the nanowires morphology were investigated, defining the optimal range of precursor pressures and processing temperature. In particular, water pressure was found to deeply influence the nanowires morphology, with the best structures produced with a water pressure of about 1 Torr. For the optimal processing conditions, XPS analysis revealed a good quality of the oxide with mainly Al_2O_3 stoichiometry and no major contaminants.

The number of SIS cycles allows to finely tune the height and width of the alumina nanowires. With the lamellar-forming BCP used as testing ground (M_w of 51 Kg mol^{-1}) it is possible to produce features with a width varying between 7 nm and 16 nm and height between 15 nm and 26 nm, while the number of SIS cycles does not affect the nanowire spacing, which remains fixed at 26 nm as defined by the self-assembled template. Preliminary results also evidenced a limited line roughness. The roughness measured by AFM analysis on the upper surface of the oxide nanowires is $1.2 \pm 0.2 \text{ nm}$, while the line edge roughness is $\sim 2.3 \text{ nm}$.

The study of the SIS process was conducted on flat BCP films. Even if in these films lamellar or cylindrical structures have random orientation, nanowires aligned over a length scale up to $1 \mu\text{m}$ can be achieved thanks to the μm -long correlation length. For practical applications, features aligned over longer length scales can be achieved by pre-patterning the substrate using a TSA approach. In this case, the produced nanostructures can be also aligned and registered in the desired direction and position.

Alumina nanowires can be exploited for lateral patterning of the oxide switching material in RRAM devices. This method allows to study of the switching properties as a function of scaling oxide thickness and width down to a few nm. The proposed fabrication method can be exploited in innovative integration approaches combining bottom-up and top-down techniques. As an example, Figure 6.13 displays a possible schematic of metal electrodes defined by electron beam lithography (EBL) for the investigation of resistance switching properties in oxide nanowires with random orientation. As visible in Figure 6.13(c), the metal electrodes can be made as close as 70 nm in order to limit the

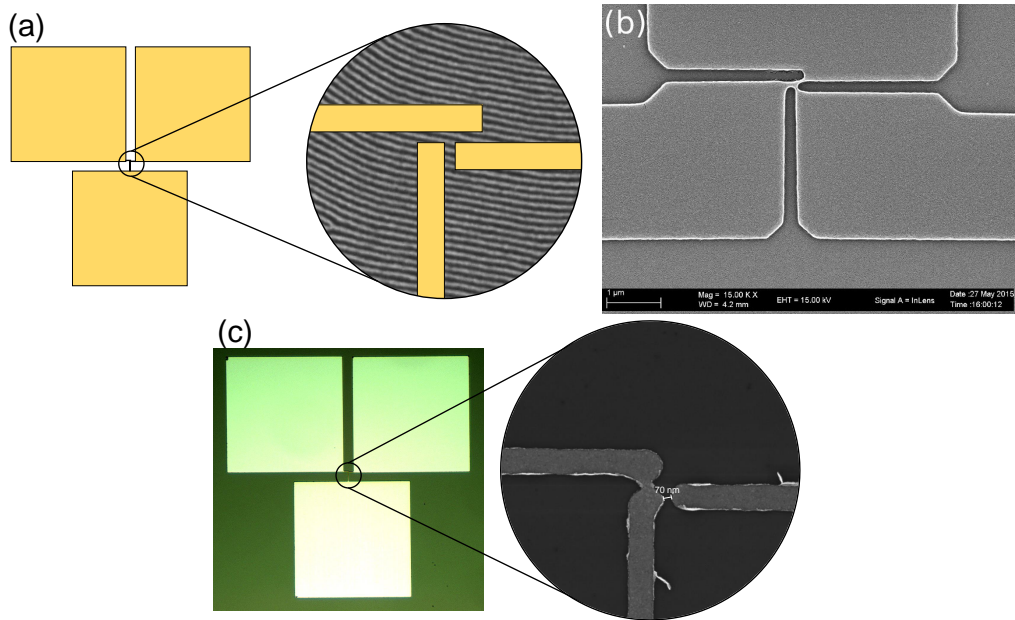


Figure 6.13: Example of configuration for metal electrodes fabricated by EBL for the contact of oxide nanowires. (a) Sketch of the test structure. (b) SEM image of the test structure defined by EBL on a flat substrate before metal lift-off. (c) Optical microscope image and SEM image (detail) of the test structure after lift-off of Pt/Ti metal electrodes. The gap can be made as small as 70 nm.

electric field necessary for the forming operation.

Another interesting perspective for the SIS technique is the patterning of other functional oxides like HfO_2 , which is currently under development, and other materials. As an example, metallic nanowires would be highly valuable for the direct patterning of nanoscale metal lines in future very high density integration schemes.

Other approaches exist for the direct patterning of oxide or metal nanostructures by bottom-up templates without relying on a pattern transfer procedure. One example is the adoption of functional BCPs which already contain the required elements. Periodic patterns formed by PS-*b*-PDMS BCP can be for example turned into self-assembled SiO_x nanostructures by a simple oxygen plasma treatment which removes carbon components and oxidizes the Si-containing polymer backbone. The same procedure can be applied to PS-*b*-PFS BCP for the formation of Fe-containing nanostructures [18]. In the ongoing research activity it is currently under evaluation the possibility to integrate patterned SiO_x nanowires formed by self-assembled PS-*b*-PDMS templates in nanoscale RRAM devices with various metal electrodes.

6.5 Conclusions of the thesis

The PhD activity focused on the fabrication and characterization of oxide-based resistive switching devices (RRAM). In the first part, the metal–insulator–metal material stack of HfO₂-based devices was characterized by photoemission spectroscopy and DC electrical tests were performed in order to assess the device properties. Memory cells with a Pt/HfO₂/TiN stack and an un-doped oxide layer were compared with cells in which the oxide was doped with different concentrations of Aluminum atoms. Aluminum doping of the oxide was confirmed as a viable route to improve the device uniformity at a moderate concentration of about 4%. However, high Al concentration of about 7% resulted in a marked deterioration of the high resistance state (HRS) retention through the appearance of sudden retention failure in about 50% of the inspected cells. A higher number of active traps in the dielectric barrier created upon reset, which is likely connected with the worsening of the HRS retention, was also qualitatively confirmed by analysis of the random telegraph noise traces. In conclusion, a careful selection of the Al doping concentration is necessary in order to find a balance between uniformity improvement and worsening of the retention properties.

In a following part of the thesis, the fabrication of nanoscale devices based on thin HfO₂ films is presented. A novel approach based on block copolymer templates was adopted in order to produce ordered arrays of nanoscale metal electrodes with very high density on top of the HfO₂ surface. In particular, this self-assembly technique was developed on top of HfO₂ substrates and the control achievable on the characteristic dimensions of the produced nanostructures was investigated. Metal electrodes with diameter down to 20 nm were produced, with a density of 10¹¹ devices/cm². The selective contact of distinct nanodevices was possible thanks to the sharp conductive tip of the conductive atomic force microscope (C-AFM). In this study, electrodes with a diameter of 28 nm were used in order to better distinguish among different devices. The electrical analysis of the initial state of the devices unveiled a variability closely related to the inherent oxide non-homogeneity at the nanoscale caused by randomly spread leaky sites with an areal density approximately one-fifth of the patterned device density. Subsequently, selected memory cells were switched between low and high resistance states in a reversible way, thus proving the non volatile resistance memory effect at the nanoscale. The electrical analysis allowed to unveil a crosstalk phenomenon arising between two memory cells during both set and reset programming operations. Based on the experimental characterization, a resistor model was developed to account for this phenomenon after a detailed investigation of the material stack. In particular, the use of continuous metal and oxide films was found to be responsible for the onset of sneak paths connecting different devices. This observation stands as a crucial issue when designing high density memory arrays and provides a missing piece of information for the understanding and practical development of very high density RRAM arrays.

The occurrence of the crosstalk suggests that alternative integration approaches are best suited for very high density RRAM arrays. In this context, nanowire oxide structures establish as a model system for the study of devices in which the functional oxide is highly scaled also in the lateral direction down to 10 nm and less. A novel fabrication method was identified which allows to directly transform one of the self-assembled polymeric units of a block copolymer template into inorganic functional materials. A study of this fabrication method is presented in the last chapter of this thesis and future outlooks based on this fabrication approach are envisaged.

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Appendices

Experimental techniques

A.1 Deposition methods

A.1.1 Sputter deposition

The sputtering method allows to deposit thin films of selected materials onto a surface. The application of a high potential difference between the anode and the cathode inside the chamber previously filled by inert gas allows to establish a gaseous plasma by electric discharge. For sufficiently energetic plasmas, the accelerated ions impinging on the target material on top of the cathode can eject particles that can travel through the evacuated chamber and deposit on the substrate (Figure A.1(b)). Depending on the conductivity of the target material, DC or RF energy sources are required to continuously maintain the plasma on-state, which also depends on the chamber pressure. A continuous control over the inlet gas source and on the chamber pressure allows to maintain a stable plasma and achieve a constant deposition rate.

The sputtering system adopted for metal deposition in the presented work is a Kurt J. Lesker PVD75 machine equipped with four different 4.2" TORUS magnetron sources in confocal configuration, as visible in Figure A.1(a). The elements available for deposition are Pt, Ta, Ti, and W. By adding a nitrogen gas flow during deposition, TiN and TaN films can also be deposited.

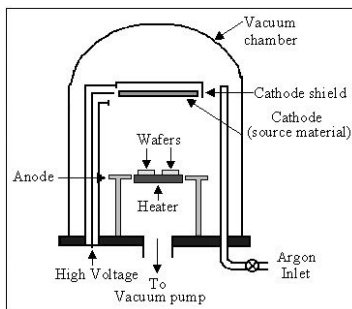


Figure A.1: (a) Schematic of a generic sputtering equipment. (b) The internal part of the Kurt J. Lesker PVD75. Two of the four confocal target sources are visible in the lower part of the picture. Above, the ring-shaped anode and the sample holder in its center.

A.1.2 electron beam evaporation

An alternative method for the deposition of a wide variety of materials is electron beam evaporation. In the evacuated chamber (base pressure of $\sim 10^{-7}$ mbar), an electronic current passing through a tungsten filament causes thermoionic emission of electrons, which are afterward collected by the anode plate and accelerated by a potential difference toward the cathode. A magnetic field bends the produced electron beam toward the crucible, where the impinging electrons locally heat the material. Depending on the material, above a particular power threshold the material in the crucible is evaporated and ejected molecules travel through the evacuated chamber, depositing on the sample surface.

The evaporation rate can be adjusted by varying the current in the filament, which in turn determines the number of emitted electrons. Two magnet poles allow to focus and to scan the electron beam over the crucible, ensuring a uniform evaporation. A water circuit around the crucible and the heated elements avoids overheating. For a schematic representation of the main parts composing the equipment, see Figure A.2(a).

The deposited film thickness can be monitored by measuring the resonant frequency of oscillation of the quartz crystal placed inside the chamber at the same distance from the crucible as of the sample. The resonant frequency changes as the material is evaporated on the crystal, and by knowing the density of the deposited material the evaporated thickness can be calculated.

This deposition method allows to deposit very thin film with high control over the deposited thickness. Moreover, the high vacuum maintained in the chamber during the deposition, typically around 10^{-6} mbar, guarantees a coverage of the sample only in those areas directly in sight of the crucible. This feature, together with a lower energy of the deposited atoms if compared to the sputter deposition, can facilitate the mask removal during lift-off processes.

The materials available for deposition comprise a wide range of elemental and molecular materials, from metals to semiconductors and oxides. The electron beam evaporation is used in this work to deposit the metal for the top electrode of the memory cells as an alternative to the sputter deposition method, in particular for nanoscale devices defined by block copolymer lithography.

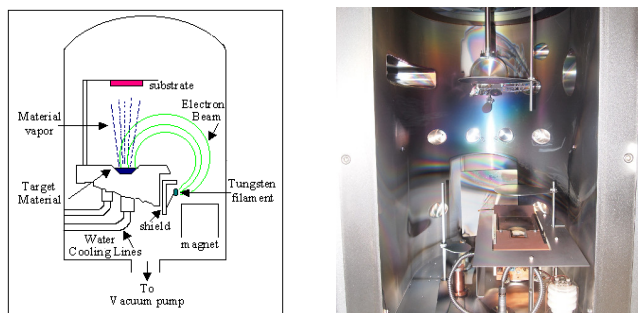


Figure A.2: (a) Schematic of a generic electron beam deposition equipment. (b) The electron beam deposition system by Kurt J. Lesker.

A.1.3 Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a growth technique originally introduced by Suntola and Antson in 1977 under the name of atomic layer epitaxy [1, 2]. Even if it belongs to the chemical vapor deposition (CVD) group, it differs from conventional CVD growth from many aspects. Based on an alternate exposure of the sample surface to two different gaseous precursors separated by purge steps, this deposition method brings the main advantages of high conformality to the substrate even in structures with high aspect ratio, optimal control over the deposited film thickness, and a uniform control on the deposited composition throughout the sample. These desirable characteristics directly derive from the cyclic, self-saturating nature of the ALD process [3, 4].

An ALD growth cycle is composed of four main steps (Figure A.3(a–d)). First, a substrate with a natural functionalization or treated to functionalize the surface is exposed to the first gaseous precursor. Contrary to standard CVD processes, the precursor is designed to react with the surface and not in the gas phase. The reaction by-products and any non reacted precursor are then expelled out of the reaction chamber by an inert carrier gas (usually N_2 or Ar) during a purging step. Subsequently, a counter reactant precursor (for oxides usually an oxidizing agent) is pulsed in the reaction chamber and reacts with the surface to complete the growth cycle, while any excess precursor together with eventual reaction by-products are afterward purged with an inert carrier gas.

In order to obtain a self-limiting and reproducible reaction between the precursor and the surface, the growth is usually operated in a specific temperature window. Within this window, the growth rate is almost constant as a function of temperature and a linear relationship applies between the number of ALD cycles and the deposited thickness. This allows an optimal control on the thickness, since the growth rate is typically well below $1 \text{ \AA}/\text{cycle}$. For temperatures outside the temperature window, various non-idealities can be encountered which affect the deposition rate and degrade the film quality. For too low temperatures, slow reaction kinetic or precursor condensation in the gas phase may occur, while for too high temperatures thermal decomposition of the precursor or a rapid desorption from the surface can prevent the ALD regime. Additionally, the deposition temperature can affect the functionalized surface (*e.g.* by changing the OH groups type and density by dehydroxylation), affecting the film growth in the initial stages. The temperature window strongly depends on the particular choice of the precursors, however most of the processes are typically operated between $50 \text{ }^\circ\text{C}$ and $400 \text{ }^\circ\text{C}$, a temperature range lower than most of the CVD processes.

The interesting ALD properties in terms of conformality and uniformity descend directly from the gas-surface limited reactions implied in the ALD process. However, the fact that the reactants should be given enough time to diffuse over the entire sample surface in addition to the cycling nature of the process highly limit the deposition rate. This issue is particularly relevant for high aspect ratio structures, for which the exposure time should be prolonged so that the gaseous precursors fill all sample structures.

Material compounds and doping The cycling nature of the ALD growth method allows to alternate multiple ALD processes for the deposition of material compounds. In addition to the aforementioned advantages typical of the ALD, the fine tuning of the "super cycle" combining the various processes allows to tailor the compound properties and to fabricate a broad range of compound stoichiometries. While the intense research on ALD precursors now allows to deposit many different materials (notably pure elements, oxides, nitrides, and sulfides), the main requirement for the combination of dif-

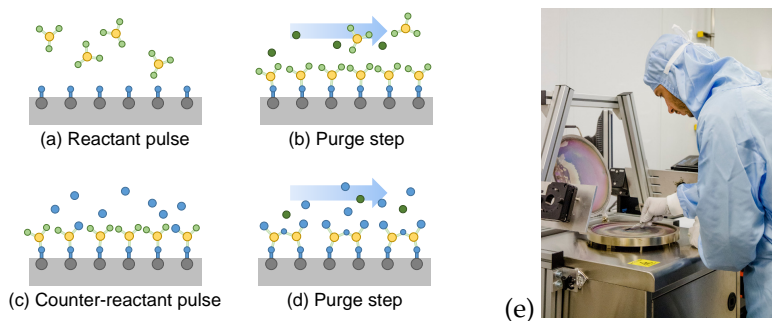


Figure A.3: (a–d) Schematic of the ALD reaction processes. (e) The Savannah 200 reactor from Cambridge Nanotech Inc.

ferent ALD cycles is their thermal compatibility, *i.e.* the temperature windows of the two processes should overlap.

Another interesting application of ALD is the introduction of layers containing a doping element alternated to the main deposition process. With this doping method, layers of “ δ -doping” can be obtained inside the main material matrix. The resulting as-deposited inhomogeneous film can be typically turned into a uniform composition with an annealing step [4].

A.2 Rapid thermal processing

Thermal processing is a post-deposition treatment that can be applied for different purposes depending on the process temperature and ambient condition. It is for example used to improve device performance by defects self-healing or doping activation, crystallize samples, oxidize layer when used with an oxidizing atmosphere, and reduce the potential barrier at the interface with metal electrodes. In this work, thermal processes were applied to induce block copolymer self-assembly.

A rapid thermal processing machine was used for this task instead of the commonly employed standard furnace. In this machine, the sample is heated directly by a radiant energy source (usually tungsten–halogen lamps) up to a few degrees per minute. During this fast thermal treatment, non-equilibrium processes are carried out since the heater is much hotter than the sample, while chamber walls remain cooler. The process can be carried out in vacuum or with a gas flow in order to rapidly cool down the sample and improve uniformity. Particular gases like oxygen, forming gas, and others can also be applied. The temperature inside the chamber is constantly monitored by a thermocouple or a pyrometer that provide a feedback for the closed-loop controlling the heating system.

All thermal treatments were carried out using the Jipelec JetFirst100 RTP machine shown in Figure A.4. The system includes a cold wall reaction chamber with maximum 4” wafer capability and 30 kW power multi-zone halogen lamp furnace with asymmetric lamps array. It can work between 20 °C and 1200 °C and with temperature ramps up to 100 °C/s. Furthermore, gas inlets are provided for O₂, N₂, and H₂(5%)–N₂ mixture (forming gas). Chamber valves ensure the capability of working between 1 and 1000 mbar. JetFirst100 allows working with pyrometer or with K-type thermocouples

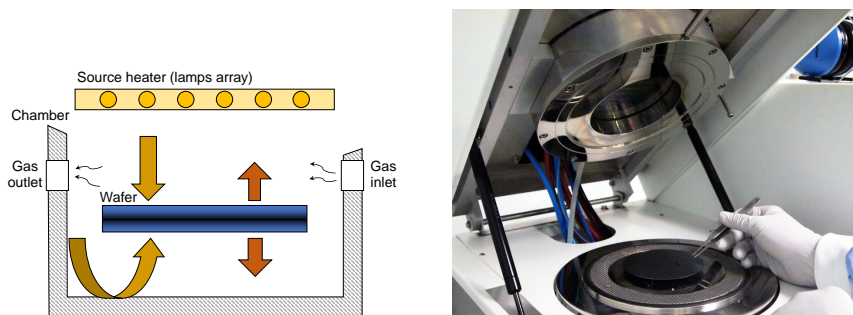


Figure A.4: (a) Schematic of the electron signals produced by the electron beam. (b) Photograph of the interior of an RTP machine with asymmetric heat by upper lamps array. (b) Photograph of the inner part of the Jipelec JetFirst100 RTP machine.

as temperature detectors. The Jipelec pyrometer detects the temperature at the center of the back side of the shield and works between 600 °C upward. Two thermocouple have access into the chamber for working range between 20 °C and 1200 °C.

The physics of RTP is dominated by radiative and irradiative heat transfers and optical properties of the wafer and of the environment. Typically, the tungsten lamp filament works at temperature between 1500 °C and 2500 °C. The heat transmission scheme of the RTP machine is reported in Figure A.4.

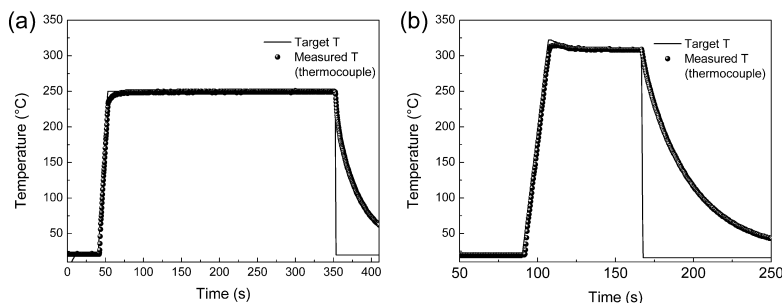


Figure A.5: Thermal ramps acquired with the Jipelec JetFirst100 RTP machine. If the rising ramp is immediately followed by the plateau (a), the actual temperature measured by the thermocouple follows a rounded profile. In order to obtain a nearly flat trend, a small overshoot should be interted after the rising ramp (b).

In order to perform reproducible thermal annealing on BCP, RTP ramps were carefully calibrated as depicted in Figure A.5. If the set temperature is simply rise up to the target value with a slope corresponding to the chosen processing ramp (22 °C/s in this work), a rounded transition can be noticed passing from the rising ramp to the plateau region. This smooth transition is not an issue when long processing times are implied (*i.e.* ≥ 5 min). On the contrary, when fast processes are carried out, the effective temperature measured by the thermocouple can steadily follow the set temperature by adding a small overshoot in the rising ramp and exponentially decreasing the set temperature down to the plateau.

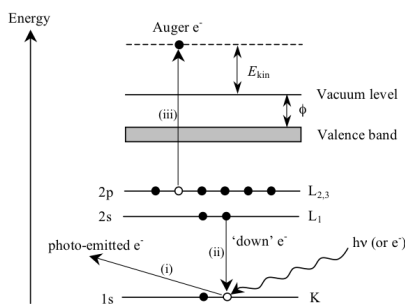


Figure A.6: Schematic of the photoemission process. A photon with sufficient energy can excite an electron to be emitted out of the inspected material. Upon energy relaxation, Auger electrons can also be emitted.

A.3 Top electrodes patterning by UV lithography

For electrical testing, the top electrodes of the memory devices need to be patterned with a defined area and shape. To this purpose, a positive photoresist was spin-coated over the dielectric layer and exposed to UV light through the lithographic mask of Figure 3.8. After development, the exposed parts of the resist were removed and the selected material for the top electrodes was deposited on top. Finally, a lift-off process in acetone removed the residual photoresist and the excess metal to defining the top electrodes.

The mask used for top electrodes patterning allows to produce capacitor structures with area between $1.6 \times 10^{-5} \text{ cm}^2$ and $1.6 \times 10^{-3} \text{ cm}^2$. This dimension permits an easy contact by tungsten probes.

A.4 X-Ray Photoemission Spectroscopy

XPS is a spectroscopy technique based on the absorption of a monochromatic X-Ray beam by the analyzed material, situated in a ultra high vacuum chamber. In the event that the impinging photons have high enough energy, an electron can be emitted (Figure A.6) with kinetic energy

$$E_K = h\nu - E_B - \phi$$

where $h\nu$ is the energy of the incoming photons; E_B is the binding energy of the electron, and ϕ is a parameter accounting for the alignment of the Fermi energy levels between the instrument and the specimen and depends on both the specific instrument and the measured material. By counting the number of photoemitted electrons as a function of their energy, it is possible to determine E_B for specific atomic orbitals in the analyzed specimen. The E_B peaks give a signature of the elemental composition at the parts per thousand range, while small shifts of the E_B for core electrons give indication of the chemical bonding of the element. Moreover, the specific peak intensities are connected with the amount of the elements inside the sample.

Due to the limited escape depth of the photoemitted electrons, the sampling depth is limited to a few nm below the surface, making XPS a surface-sensitive technique. However, the sampling depth can be varied by adjusting the angle between the sample and the detector apparatus, also called take-off angle. Close to normal take-off angle

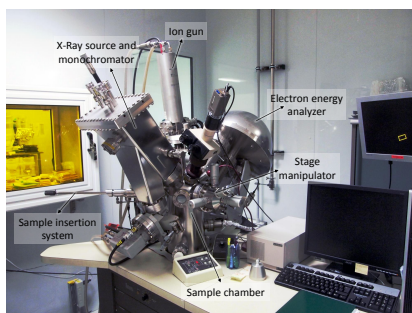


Figure A.7: PHI 5600 ESCA system. The main elements composing the XPS equipment are labeled.

values give the maximum depth sensitivity, while small take-off angles give information from the superficial region.

The PHI 5600 ESCA system used to acquire the XPS spectra is reported in Figure A.7. The equipment is composed of two X-Ray sources generated by Mg K_{α} (1256.6 eV) and Al K_{α} (1486.6 eV) spectral lines. The Al K_{α} source is followed by a monochromator to further decrease the line width and increase the energy resolution. The system is equipped with a hemispherical electron energy analyzer and objective lenses with an acceptance angle of 8° . The energy resolution depends on the choice of the pass energy and on the intrinsic line width of the photon source. The stage is provided with x, y and z manipulators to adjust the position of the sample and with an additional rotation degree of freedom for the selection of the take-off angle. In addition, an ion gun provides sputtering capability for the acquisition of depth profiles and cleaning of the sample surface.

A.5 Scanning electron microscopy

Scanning electron microscope (SEM) is a type of electron microscope that acquires images of the sample by scanning a high-energy beam of electrons in a raster scan pattern. The electrons interact with atoms in the sample producing a signal that contains information about surface topography, composition, and other properties such as electrical conductivity. The types of signals produced by an SEM include secondary electrons (SE), back-scattered electrons (BSE), characteristic X-rays, light (CL), specimen current (SC), and transmitted electrons (TE). A pictorial view of the emitted electrons useful for an SEM analysis is depicted in Figure A.8.

SE are low energy electrons (<50 eV) which are generated by inelastic scattering of primary electrons (PE) on the atomic core or on the electrons belonging to atomic shells of the sample material. BSE are beam electrons that are reflected from the sample by elastic scattering. They have energy higher than 50 eV and carry depth information. BSE are often used in analytical SEM along with the spectra made from the characteristic X-rays to obtain information about the chemical composition. The intensity of the BSE signal is strongly related to the atomic number (Z) of the specimen. Therefore, BSE images can provide information about the distribution of elements in the sample. Characteristic X-rays are emitted when the electron beam removes an inner shell electron from the sample, causing a higher energy electron to fill the shell and release energy. These characteristic X-rays are used to identify chemical composition and measure the abundance

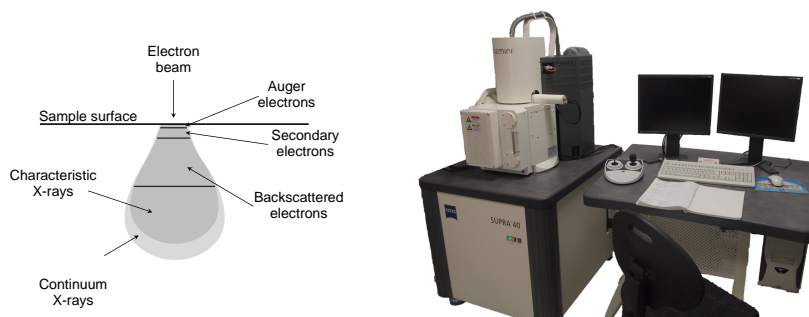


Figure A.8: (a) Schematic of the electron signals produced by the electron beam. (b) Photograph of the Zeiss SUPRA 40 SEM instrument with Gemini column.

of elements in the sample.

The most common electron detection mode for imaging reveals secondary electrons. Using this mode, SEM can produce high resolution images of the sample surface, revealing details less than 1 nm in size. Due to the very narrow electron beam, SEM micrographs have a large depth of field yielding a characteristic three-dimensional appearance useful for understanding the surface structure of a sample. A wide range of magnifications is possible, from about 10 times to more than 500,000 times, about 250 times the magnification limit of the best optical microscopes.

Figure A.8 shows the Zeiss Supra 40 SEM used in this work. Supra 40 is a field emission (FE) SEM based on the Gemini column working in the accelerating voltage range from 20 eV up to 30 keV. The core the system is the accelerating column. Its main elements are: emitter gun, condenser lenses, shutter, field lenses, aperture, projector lens, deflecting coils, and secondary electron detector. An additional high resolution electron detector is included in the field lens at the bottom of the column. This in-lens detector allows higher collection efficiency due to its close vicinity to the sample (typically 4–5 mm) and provides an additional accelerating voltage of 8 kV.

The electron gun consists of three components: a cathode for emitting the electrons, an extractor anode, and a cathode lens to focus the emitted electrons into the electron beam. The cathode used by Gemini column is a ZrO/W Schottky junction of field emission type. The sharp needle-shaped cathode produces a high electrical field at the apex even at low extractor voltage (the field strength is usually 10^8 V/m). The apex is normally less than 100 nm of radius and has a distance of a few nanometer from the point where electrons are focused after the cathode lens. These characteristics allow an optimal beam focusing and reduced aberrations if compared to other types of cathode.

A.6 Atomic force microscopy

The atomic force microscope (AFM) is part of the larger family of scanning probe (SPM) equipments. These systems are based on a sharp needle-shaped probe scanning above the sample surface. The typical dimension of the probe tip lies around 0.1 – 10 nm and allows features down to the atomic level to be inspected. The fast development of SPM techniques starting from the end of 1980s is due to the ability of these analysis methods to provide an accurate and low cost characterization of the surface and to the broad class of material properties that can be investigated with these versatile tools.

The peculiarity of each scanning probe method depends on the particular tip–surface interaction that is exploited for the analysis. The atomic force microscope (AFM) was invented by Gerd Binnig, Calvin F. Quate, and Christopher Herber in 1986 [5]. In the AFM, the sharp tip of the scanning probe is either attracted or repulsed from the sample due to inter-atomic interactions. The inter-atomic potential is empirically modeled by the Lennard–Jones potential in the form of $U_{L-J} = U_0[-2(r_0/r)^6 + (r_0/r)^{12}]$, in which the major contribution is typically given by Van der Waals inter-atomic forces. The typical behavior is attractive at distances greater than r_0 due to dipole–dipole interactions, and highly repulsive at shorter distances due to Pauli exclusion principle. The interacting force can be decomposed in normal and tangent contributions with respect to the surface, which can be both measured by the deflection of the scanning probe.

During an AFM scan, the tip is held in close vicinity of the sample surface and is moved by the scanning device. Depending of the AFM equipment, either the sample or the AFM head can be moved laterally and vertically by piezoelectrical actuators for an accurate tip–sample positioning and scanning. The exact height position of the tip, together with its lateral deflection, is usually derived by a laser aligned at the tip of the cantilever. The laser beam is reflected by the cantilever tip toward a multi-element photodiode for a discrimination of lateral and vertical displacements. A feedback loop provides the necessary working condition by maintaining a fixed parameter throughout the scan. The image signal can have various sources depending on the type of analysis required. In many cases, the signal can come directly from the feedback loop, or it can be derived from other parameters like cantilever lateral deflection, oscillation frequency or phase.

AFM analysis can be operated in two general acquisition methodologies depending on the relative tip–surface distance. In contact mode, the tip is held close to the surface in the region where the tip–surface interacting force is highly repulsive ($-\frac{\partial F}{\partial r} < 0$) and a steep characteristic allows the instrument to be highly sensitive to inter-distance variations. In this region, the tip is made in direct contact with the surface and is subjected to high mechanical stress. Therefore, the interaction should be carefully calibrated to avoid a surface damage, especially in soft materials. In many cases, the tip–surface interaction is held constant by setting a proper set point in the feedback loop. This corresponds to a constant cantilever deflection detected by the photodiode. The contact mode allows to perform electrical investigation when a potential difference is applied between the tip and the surface [6, 7]. This operation is called conductive AFM (C–AFM) and was applied in the present work for the investigation of local conductivity in samples containing a thin HfO₂ film with and without top nanoelectrodes. Using a scanning conductive tip it was possible to acquire current maps of the dielectric surface, while fixing the tip position at selected points also switching operations were achieved.

When a direct contact of the tip is not needed, it is possible to minimize tip wearing using the tapping-mode, also called semi-contact mode. A mechanical oscillation is forced in the cantilever at a frequency close to the resonance peak, causing tip oscillations between 10 and 100 nm. The tip enters intermittently into the strongly repulsive region for a short time, and the interaction is minimized. The total force acting on the tip is the sum of Van der Waals and elastic contributions, which cause a variation of the amplitude and phase of oscillation due to dissipative interaction. In the feedback loop, the usual monitor parameter is the tip average deflection. The topography image is derived from the amount of tip vertical displacement necessary to maintain a constant

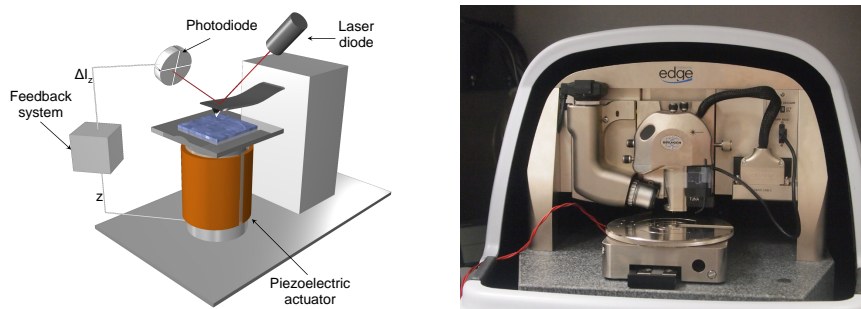


Figure A.9: (a) Schematic of a generic AFM system. (b) Photograph of Bruker Dimension Edge instrument.

average interaction, while the phase contrast gives information about the local stiffness of the surface. When DC and AC signals are applied to the tip, also other investigations become possible. An example is kelvin potential, which returns a value proportional to the local work function. Alternatively, a magnetic tip can be used to perform an analysis of the local magnetization.

The AFM and C-AFM analysis presented in this thesis were performed with a Bruker Dimension Edge instrument equipped with a TUNA electrometer with current range spanning from 1 pA to 1 μ A. The surface morphology characterization in tapping mode was acquired with sharp Si topography probes (PPP-NCHR, from Nanosensor) with a radius of curvature below 10 nm. The surface topography and simultaneous current maps were acquired in contact mode using Pt/Ir-coated tips (PPP-CONTPt, from Nanosensor, with a 25 nm coating on top Si tip with $\times 10$ nm curvature radius) or highly doped diamond-coated tips for improved wear resistance (CFT-CONTR, from Nanosensor, with 100 – 200 nm curvature radius but a nanoroughness in the 10 nm range due to diamond grains).

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List of Publications

As of January 2016

- J. Frascaroli, F. G. Volpe, S. Brivio, and S. Spiga, "Effect of Al doping on the retention behavior of HfO₂ resistive switching memories", *Microelectronic Engineering, Insulating Films on Semiconductors 2015* **147**, 104–107 (2015).
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Other publications not strictly related to the activity presented in this thesis

- J. Frascaroli, G. Seguini, E. Cianci, D. Saynova, J. van Roosmalen, and M. Perego, "Surface passivation for ultrathin Al₂O₃ layers grown at low temperature by thermal atomic layer deposition", *physica status solidi (a)* **210**, 732–736 (2013)
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Publications in preparation

- "Study on the variability of nanoscale resistive switching devices".
- "Active traps in Al-doped HfO₂ resistive switching memories probed by random telegraph signal".
- "Dielectric properties and local atomic coordination in Er-doped hafnium oxide films".
- "Effect of precursor pressure on oxide nanostructures fabricated by sequential infiltration of block copolymers".
- "Resistive switching in oxide nanowires: top-down meets bottom-up".

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