# Effects of Package Parasitics on Substrate and Interconnection Crosstalk in Mixed-Signal CMOS ICs

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*Abstract*- This paper presents an experimental evaluation of crosstalk effects due to current pulses drawn from voltage supplies in mixed analog-digital CMOS integrated circuits. A test chip was designed in 0.18-$\mu$m CMOS technology, integrated and mounted in two different ways, namely, in JLCC package and with flip-chip assembly technique, in order to compare measurement results. As expected, the circuit assembled with the flip-chip technique has better immunity to disturbances generated by the digital section, due to the lower values of interconnection parasitics.

## I. Introduction

In mixed-signal systemson-chip (SoC) design, crosstalk is one of the main difficulties to face. Indeed, micro-integrated SoCs exploit the ever increasing integration density offered by deep submicron fabrication technologies. However, designers must keep in mind that in a mixed-signal SoC, i.e. in a device where analog and digital circuits are integrated on the same chip, effects of digital switching noise on the analog section can be an adverse factor, affecting the overall system performance [1]. Therefore, a correct design methodology should take the digital switching noise into account from the early stages of the design process, and requires a fast and accurate analysis of current consumption during logic transitions, so as to evaluate the noise due to the switching activity of digital cells [2].

Several layout techniques have been proposed to attenuate the effects of the digital part of the integrated circuit on sensitive analog blocks. These techniques include physical separation of the analog and the digital section, insertion of guard rings, shielding with buried well.

However, the shielding technique must be chosen and layout must be optimized considering all possible paths for disturbance propagation, that depend on both on-chip and off-chip parasitics. Indeed, simulations and measurements demonstrate that interconnection parasitics can severely affect on-chip voltage stability. For this reason, the insertion of an improperly biased shield can have a negative effect, as disturbances can propagate through the shield itself when this is not biased at a constant voltage.

Therefore, designers must carefully evaluate the contribution of all parasitics to crosstalk, by adopting a realistic model of parasitics for simulations.

To evaluate the impact of package parasitics, we have designed a test chip, which has been fabricated and assembled into a package and with flip-chip technology. By measuring digital switching noise, we can compare crosstalk effects due to different mounting technologies.

## II. Model for Substrate and Interconnection Parasitics

Disturbances propagate from the digital to the analog part through different paths: the chip substrate, the on-chip interconnections, and the off-chip interconnections due to the package and the board. These contributions have different importance, depending on the integrated circuits (IC) fabrication and assembly technique.

The effects of the path through the substrate depend on the bulk resistivity. In ICs with a heavily doped bulk and an epitaxial layer, the substrate noise can be the main concern for crosstalk, as disturbances can propagate through the whole chip bulk without a remarkable attenuation [3].

On the other hand, in ICs with a lightly doped bulk, the substrate resistivity attenuates the noise propagation. In such a situation, physical separation between digital and analog parts helps to reduce crosstalk effects.

Interconnection parasitics affect the stability of bias voltages. In particular, series resistance and inductance, together with capacitances towards ground and between wires,

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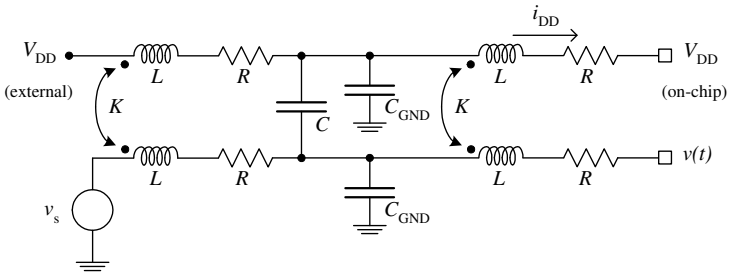


Figure 1. Equivalent circuit for digital switching noise due to interconnections.

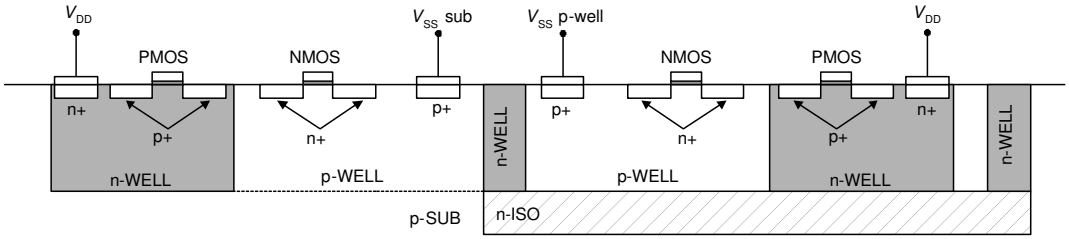


Figure 2. Schematic cross section view of NMOS and PMOS devices in the used technology.

constitute an $RLC$ network which can cause the internal supply voltages to be significantly different from the external voltages. This effect has been described as "ground bounce" and "$V_{\rm DD}$ bounce" [4].

Moreover, cross-capacitance and mutual inductance between bondwires cause electromagnetic coupling between digital and analog supplies. Fig. 1 illustrates a model of bonding and package parasitics for two adjacent wires [5]. The mutual inductances $K$ and the cross-capacitance $C$ account for electromagnetic coupling between wires. The instantaneous current $i_{\rm DD}$ due to digital switching of logic gates produces a voltage drop, which affects the on-chip digital supply $V_{\rm DD}$, and propagates to the adjacent wires through both capacitive coupling due to the capacitance $C$ between wires and inductive coupling due to the mutual inductance represented by $K$. Consequently, the analog on-chip voltage $v(t)$ can differ from the external voltage $v_s$.

From these considerations, it is apparent that an accurate design of a mixed-signal circuit must account for parasitics.

## III. Test Chip and Board Description

The test chip was designed in a 0.18-$\mu$m CMOS technology with high-resistivity p-type substrate, twin wells, and an n-isolation layer that can be used for shielding purposes. Fig. 2 shows a vertical section of MOS devices with and without the n-isolation layer.

Local p-wells are isolated from the global p-substrate by the n-isolation layer (buried n-iso contacted with lateral n-wells), as shown on the rightmost side of Fig. 2. The isolated p-well is contacted to a ground ($V_{\rm SS}$ p-well) different from the substrate bias voltage ($V_{\rm SS}$ sub).

P-wells designed outside the n-isolation layer are connected through the common substrate, as shown on the leftmost side of Fig. 2.

A p-well guard ring, biased at the substrate voltage ($V_{\rm SS}$ sub), can be placed around devices. When the n-isolation layer is used together with the guard ring, the p-well guard ring is external to the n-isolation region.

The developed test chip includes digital noise injecting structures and analog noise collecting structures; all the building blocks were designed for a pipeline analog-to-digital (A/D) converter.

The layout of digital structures was redesigned in different configurations, to investigate which is the best solution in terms of crosstalk immunity. Six different injection structures were integrated. Each of them includes a non-overlapping two-phase clock generator, driven by an external clock working at a frequency of 2 MHz. The clock generator has two separate $V_{\rm DD}$ supplies, namely, a "digital" supply $V_{\rm DD}$ = 1.2 V (used for most digital cells), and an "analog" supply $V_{\rm DD}$ = 2.5 V (used for last stages driving analog CMOS switches). The six configurations differ in the distance from the collecting structures, the use of the n-iso layer, and the use of a p-well guard ring. P-wells laid out inside the n-iso layer are biased with dedicated ground pads. The analog noise-collecting structure is a band-gap voltage reference.

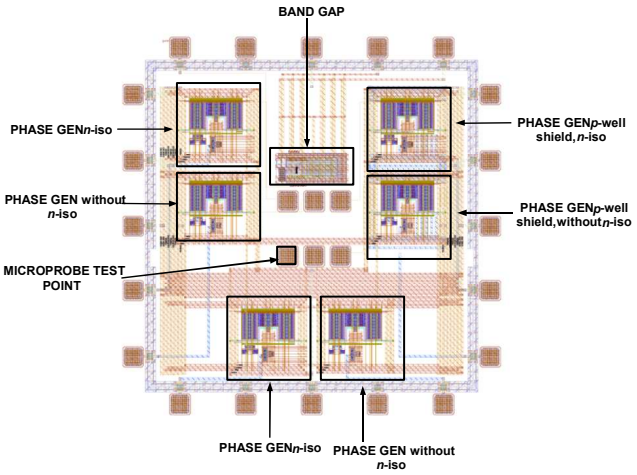


Figure 3. Layout of the test chip.

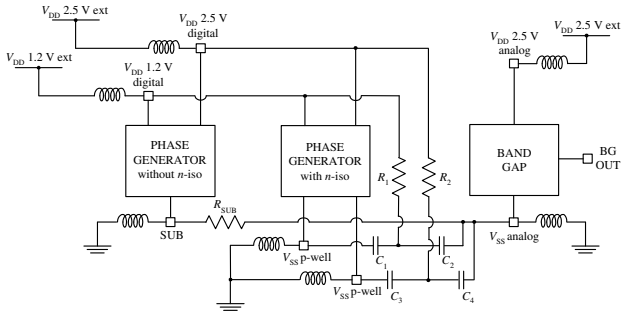


Figure 4. Schematic diagram of the test chip, including parasitic elements.

Fig. 3 illustrates the chip layout. The pads are spaced by 220 $\mu$m, to make flip-chip assembly easier. Therefore, off-chip interconnections are not at minimal distance, and parasitic coupling between adjacent wires is reduced. For this reason, at a first approximation, we consider only parasitic inductances due to bondwires and package (in the device assembled with chip-in-package technology), and neglect mutual inductances and capacitances between wires. Under the above assumptions, the simplified schematic diagram of the test chip is shown in Fig. 4. Capacitances $C_1$, $C_2$, $C_3$ and $C_4$ model reverse-biased junctions between n-iso and p-wells ($C_1$ and $C_3$), and between n-iso and substrate ($C_2$ and $C_4$). Resistances $R_1$ and $R_2$ account for the resistivity of the n-iso layer.

The chip was mounted on the test board with two different mounting techniques: chip-in-package (Fig. 5) and flip-chip on board (Fig. 6).

When using the first technique, the chip was assembled into a JLCC-24 (24-pin ceramic J-leaded chip carrier) pack-

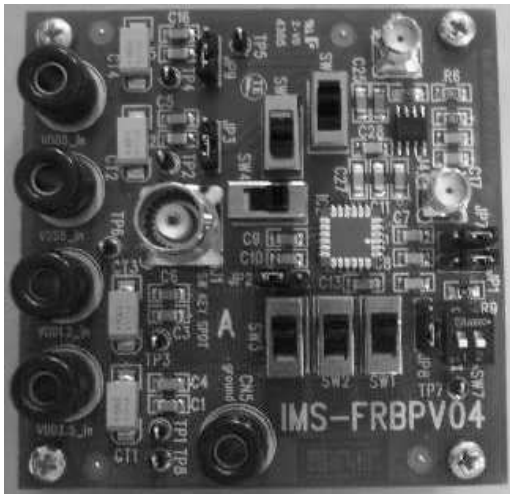


Figure 5. Test board with chip-in-package.

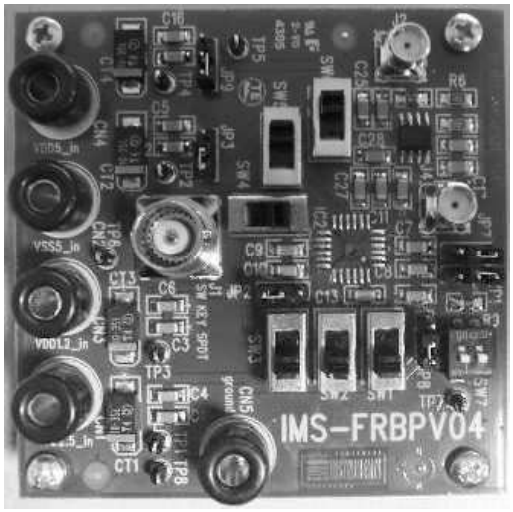


Figure 6. Test board with flip-chip.

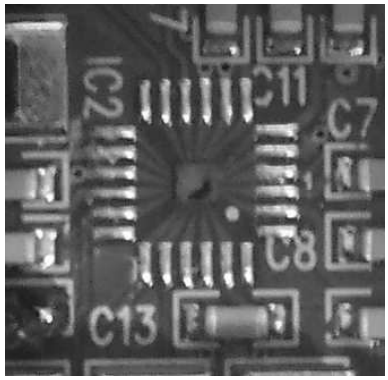


Figure 7. Detail of the flip-chip on board.

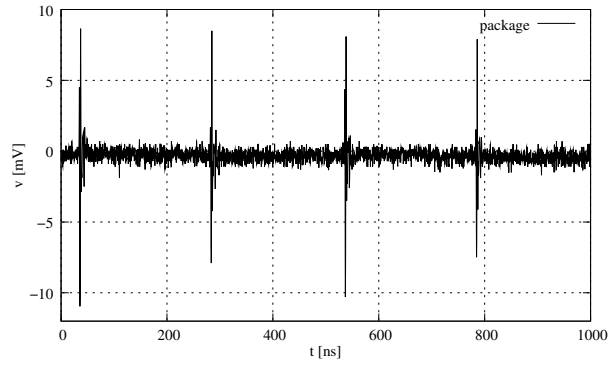


Figure 8. Measured ac-coupled band-gap output voltage for the chip-in-package.

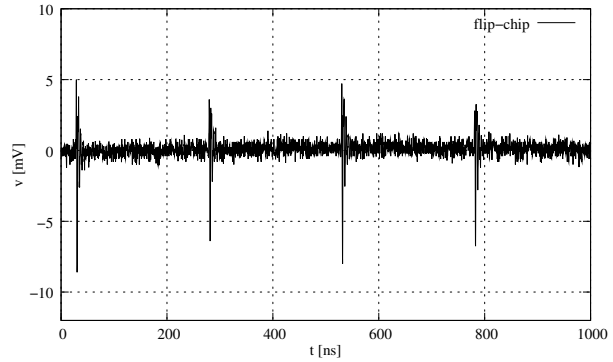


Figure 9. Measured ac-coupled band-gap output voltage for the flip-chip on board.

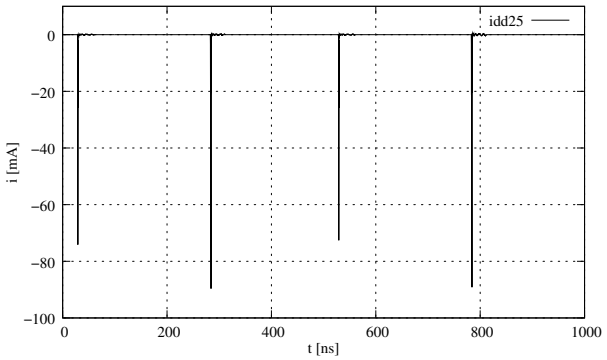


Figure 10. Simulated waveform of the digital supply current $i_{\mathrm{DD}}$ ($V_{\mathrm{DD}}$ = 2.5 V).

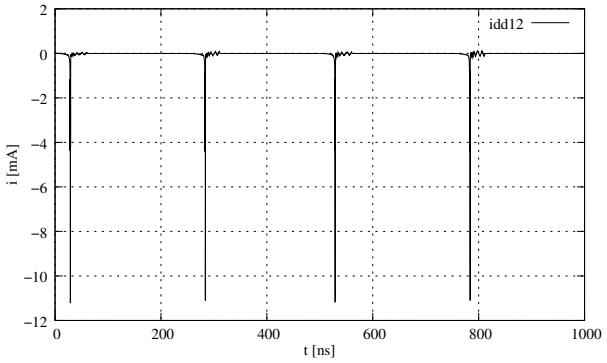


Figure 11. Simulated waveform of the digital supply current $i_{\mathrm{DD}}$ ($V_{\mathrm{DD}}$ = 1.2 V).

age. As the chip has only 20 pads, one pin per side is not connected. The length of bondwires is 1 mm, which leads to a parasitic inductance of about 1 nH. Moreover, J-shaped pins have a total length of about 3.5 mm, thus contributing with an additional inductance of (about) 2 nH.

When using the flip-chip technique, the chip is assembled directly on the board. Fig. 7 shows a detail of the flip-chip on board. This assembling technique completely eliminates additional parasitic elements due to the package.

It is worth remarking that the two boards in Figs. 5 and 6 are identical. As the JLCC-24 package has the chip cavity on the lower side, the orientation of the chip and the relative position of contacts are the same for the two test boards. In Fig. 7, the solder areas for the JLCC package and the conductive traces converging towards the flip-chip are apparent.

## IV. Measurement Results

The test chips, assembled as described above, were fed with a 2-MHz clock signal provided through an external clock generator.

Figs. 8 and 9 show the time-domain switching noise voltage at the band-gap reference output of the test chip when one of the clock phase generators is running. Figs. 8 and 9 were obtained when activating the leftmost clock generator on the bottom side in Fig. 3. The measured effects of the other clock generators in Fig. 3 are similar, and band-gap output waveforms differ only in amplitude. All signals were acquired with a 2.5-GHz digitizing oscilloscope.

Figs. 10 and 11 show the simulated current waveforms of the $V_{\mathrm{DD}}$ supply current of the digital clock phase generator. We can observe that the largest peak currents are drawn from $V_{\mathrm{DD}}$ = 2.5 V, as the final stage is designed to drive a 2.5-V clock tree. The ground currents $i_{\mathrm{SS}}$ exhibits a similar waveform. By comparing Figs. 8 to 11, we can note that the effect of digital current spikes on the band-gap output voltage is limited to time intervals where the logic transitions occur.

Table 1 summarizes the measured peak-to-peak and rms values of the noise at the band-gap output. Measurements results from structures with and without p-well guard rings are not provided separately in the table, since there is no

TABLE 1. Measured peak-to-peak and rms values of ac-coupled disturbances at the band-gap output.

| | chip-in-package output noise voltage | | flip-chip output noise voltage | |
|---|---|---|---|---|
| distance, layout configuration | peak-to-peak | rms | peak-to-peak | rms |
| 470 $\mu$m, outside n-iso layer | 15.3 mV | 0.69 mV | 13.8 mV | 0.50 mV |
| 470 $\mu$m, inside n-iso layer | 22.5 mV | 0.81 mV | 16.8 mV | 0.57 mV |
| 750 $\mu$m, outside n-iso layer | 15.1 mV | 0.66 mV | 13.6 mV | 0.49 mV |
| 750 $\mu$m, inside n-iso layer | 19.9 mV | 0.76 mV | 13.6 mV | 0.49 mV |

significant difference between the obtained values.

Let us comment measurement results.

First of all, as expected, the flip-chip assembly technique reduces crosstalk noise in all layout configurations. This result is due to the absence of all bondwire and package parasitics (in particular, of the series inductance). Therefore, a first (obvious) result is that, from the crosstalk immunity viewpoint, a chip without package has better performance.

For the chip-in-package, the insertion of an n-iso shield worsen crosstalk performance. This effect is due to parasitic inductances in series with the n-iso biasing voltage. Indeed, high-frequency impedances and digital switching currents cause a "bouncing" effect in the bias voltage of the n-iso layer (i.e., in the "local" $V_{\rm DD}$ of digital blocks), which is capacitively coupled to the substrate (see Fig. 2). Disturbances injected by the n-iso bias voltage propagate through the substrate towards the analog sensitive blocks, and are attenuated by distance. This explains why the band-gap voltage reference is more sensitive to the closest clock phase generator. Injection of disturbances from wells into the substrate occurs also in blocks outside the n-iso layer; however, for such blocks, the capacitive coupling is reduced, due to both less area and less n-doping concentration of the n-wells directly placed above the substrate.

The dependence of crosstalk from distance indicates that substrate is one of the paths for crosstalk noise.

Other crosstalk paths are on-chip and off-chip interconnections. Such paths have the same importance in the chip-in-package and in the flip-chip test circuits, and coupling factors do not depend on the distance between digital and analog blocks. By reducing the series impedance of voltage supplies with flip-chip assembly technique, we lower the contribution to crosstalk due to substrate propagation.

## V. Conclusion

This paper has illustrated the effects of digital switching noise on analog sections in a mixed-signal CMOS test chip specifically designed for this purpose and mounted with different techniques, namely, chip-in-package and flip-chip. Experimental evidence indicates that the flip-chip assembly technique has better performance than the one with chip-in-package, due to reduction of parasitics.

Measurement results demonstrate that parasitic inductances can have an adverse effect on shielding, since shielding layers may contribute to disturbance propagation when they are not properly biased. Therefore, we can conclude that the optimal layout design of the chip depends on packaging and assembly technique.

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