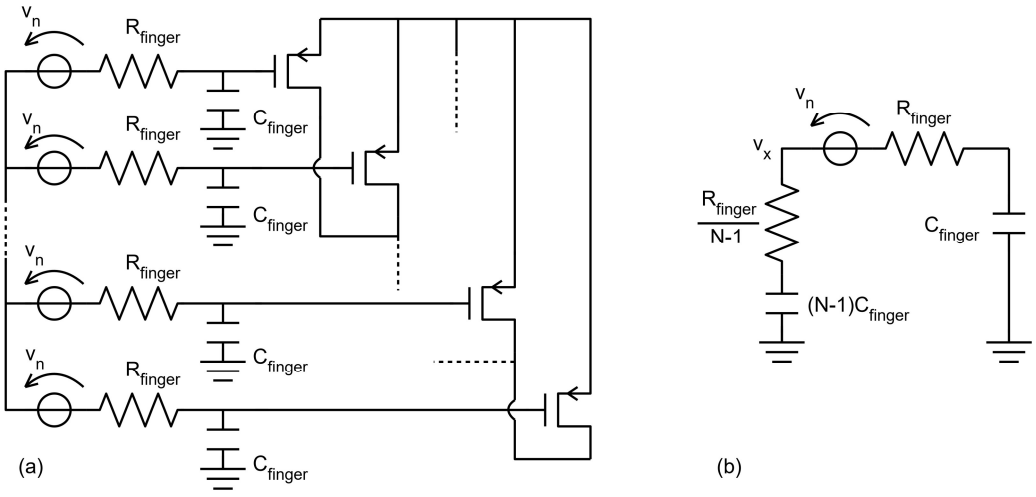

Figure 4.11: Input transistor folded N times modeled as N parallel equivalent transistors (a). Equivalent circuit for evaluating the noise contribution of each finger (b).

the impact of each finger on the electronic noise, each finger is considered individually, with the remaining ones assumed to be noiseless, as shown in the equivalent circuit of Fig. 4.11(b).

Denoting by i the current flowing through the loop, we can write the following equations:

$$\begin{cases} v_x = i\left(\dfrac{R_{finger}}{N-1} + \dfrac{1}{s(N-1)C_{finger}}\right) \\ v_n - v_x = i\left(R_{finger} + \dfrac{1}{sC_{finger}}\right) \end{cases} \tag{4.21}$$

By substituting the first expression into the second, we obtain:

$$v_n = i\frac{N}{N-1}\left(R_{finger} + \frac{1}{sC_{finger}}\right) \qquad v_x = \frac{v_n}{N} \tag{4.22}$$

Since $v_x^2 = v_n^2/N^2$, the input-referred power spectral density is:

$$S_v(f)_{finger} = \frac{4kTR_{finger}}{N^2} \tag{4.23}$$

As a consequence, the total noise contribution given by all fingers is:

$$S_v(f) = NS_v(f)_{finger} = \frac{4kTR_{finger}}{N} = \frac{4kTR_g}{N^2} \tag{4.24}$$

where the gate resistance, R_g, is equal to NR_{finger}. Hence, it can be seen that folding the gate N times reduces the thermal noise power spectral density by a factor N^2, thereby rendering this contribution negligible. In the implemented layout, the number of gate folds was set to $N = 100$.

Another important feature in the layout concerns the placement of the feedback capacitor as close as possible to the input node, in order to minimize parasitic effects introduced by the connection lines. Finally, it is important to emphasize that also the layout of the input stage resistor (R_1 in Fig. 4.2) must be taken into account. As a matter of fact,

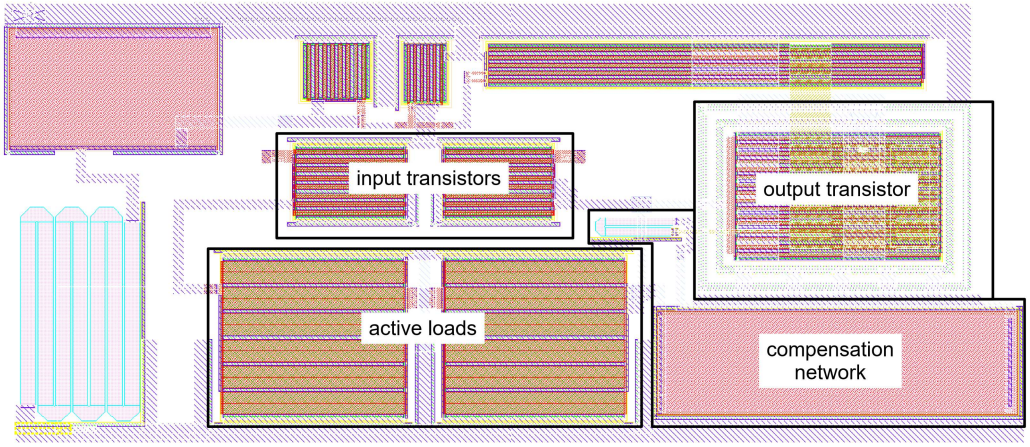

Figure 4.12: Layout of the line-driver connected to the single-ended preamplifier for hole-induced signals.

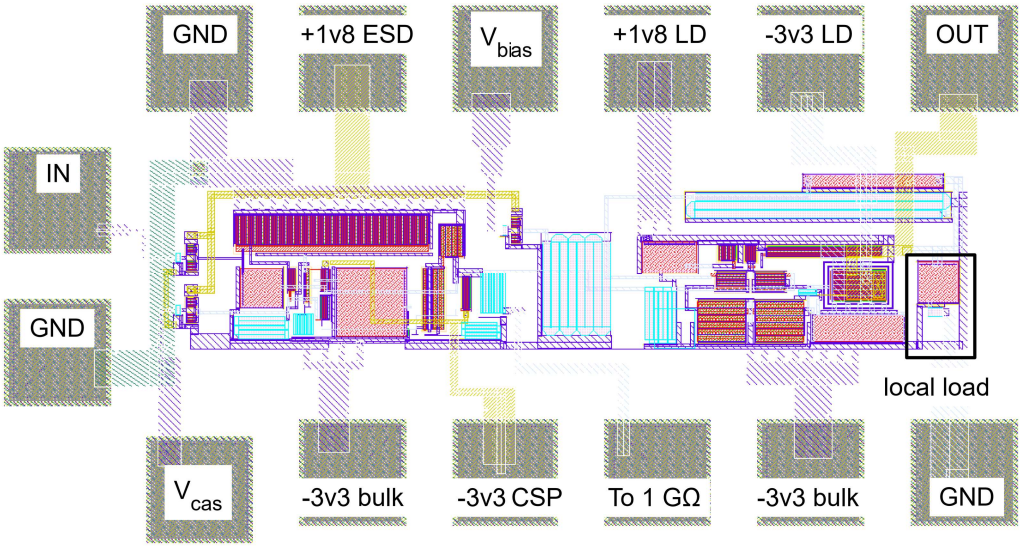

Figure 4.13: Complete layout of the single-ended charge sensitive preamplifier for for reading hole-collecting electrodes. The occupied area is 900 µm x 475 µm.

it can be characterized by a flicker noise component that can be reduced, especially in the worst-noise corner case, by increasing the device area.

The line-driver layout is shown in Fig. 4.12. As can be observed, an effort was made to preserve the symmetry of the input stage as much as possible, since it consists of a differential pair. Furthermore, particular attention was dedicated to the output transistor, which was equipped with a double guard ring. This design choice helps improve isolation from substrate noise and enhances protection against latch-up phenomena, thereby increasing the overall robustness and reliability of the circuit [44].

The complete layout of the CSP optimized for reading hole-collecting electrodes is reported in Fig. 4.13. To interface the integrated circuit with the external electronics, multiple pads were placed along the perimeter of the circuit and connected to the corresponding internal nodes. The size and structure of these pads are primarily determined

by reliability requirements and manufacturing tolerances associated with the wire bonding process. Considering a typical bond wire diameter of $25\,\mu\mathrm{m}$, pad dimensions were set to $80\,\mu\mathrm{m} \times 80\,\mu\mathrm{m}$, with a spacing of $40\,\mu\mathrm{m}$ between adjacent pads. Although larger pads simplify the bonding process, it is important to keep in mind that they also increase parasitic capacitance and occupy more die area, so their dimensions cannot be arbitrarily increased.

Additionally, the power supply pads have been deliberately separated to minimize cross-coupling. For example, the $-3.3\,\mathrm{V}$ supply line powering the line driver was kept electrically isolated from the bulk bias line. This separation helps prevent voltage fluctuations or noise on one line from affecting the other, thereby maintaining the proper operation and stability of the circuit.

4.2 Circuit Post-Layout Simulations

The circuit described in the previous paragraphs was accurately simulated using the analog test-bench shown in Fig. 4.14.

To emulate the delta-like current pulses generated by the detector, a $1\,\mathrm{pF}$ test capacitor, C_t, was placed in series with a step voltage source. Considering that the mean energy required to create an electron-hole pair in germanium is $2.96\,\mathrm{eV}$, a $1\,\mathrm{MeV}$ interaction produces approximately $3.4 \cdot 10^5$ charge carriers, corresponding to a total charge of about $54\,\mathrm{fC}$. To simulate this charge injection, a $54\,\mathrm{mV}$ voltage step can be applied to the test capacitor. Moreover, to reproduce the detector capacitance, an additional $15\,\mathrm{pF}$ capacitor, C_d, was included, as discussed in the previous chapter. The test-bench was completed with the $1\,\mathrm{G\Omega}$ feedback resistor, as well as the voltage sources required for the proper operation of the preamplifier and the line driver.

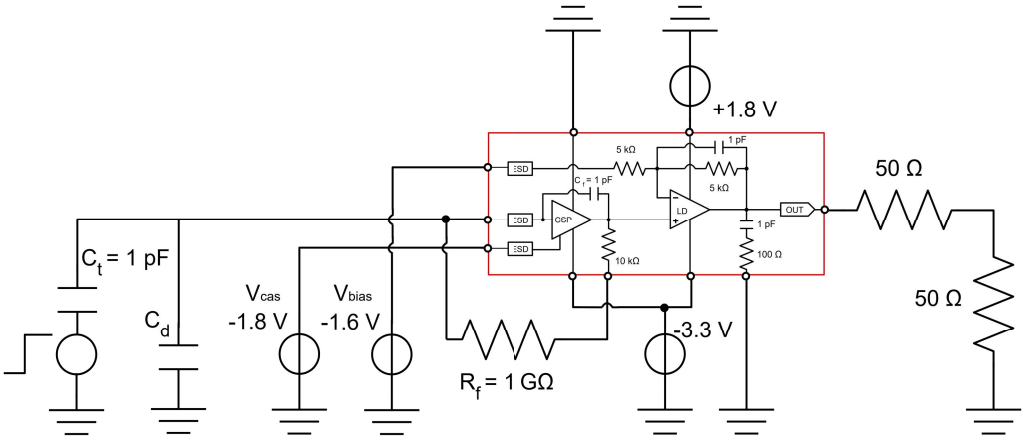

Figure 4.14: Schematic diagram of the test bench used to evaluate the performance of the single-ended ASIC preamplifier optimized for processing hole-induced signals. A $1\,\mathrm{pF}$ test capacitor, C_t, was added to transform the voltage step signal into a current delta-like pulse.

4.2.1 Circuit Stability and Linearity Performance

The circuit is characterized by a power consumption of $25\,\mathrm{mW}$ and a dynamic range of $1.35\,\mathrm{V}$, corresponding to an output equivalent energy range of the detection system

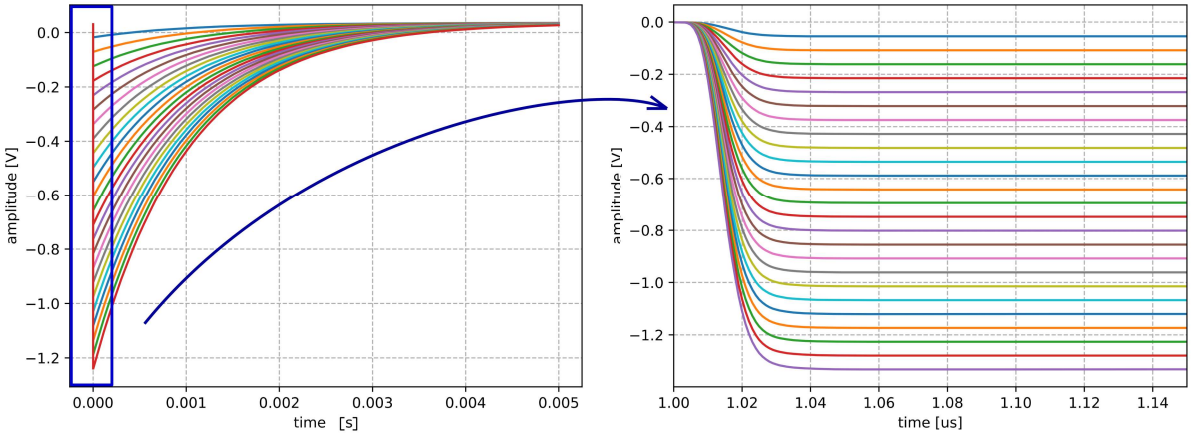

Figure 4.15: Post-layout simulations of the CSP output signals across the $50\,\Omega$ resistors (see Fig. 4.14). Interactions of energy between $1\,\mathrm{MeV}$ and $25\,\mathrm{MeV}$ are considered. The detector capacitance is $C_d = 15\,\mathrm{pF}$. As can be observed from the analysis of the signal falling edges, no ringing effects appear.

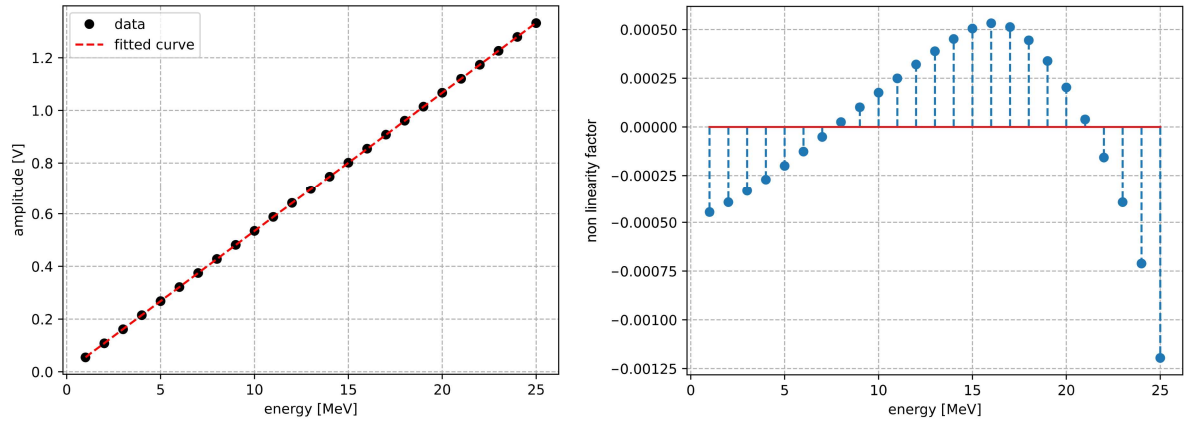

Figure 4.16: On the left, linear fit of the CSP output signal amplitudes. On the right, non-linearity factors over the CSP range.

equal to $25\,\mathrm{MeV}$. The output signals of the CSP, split by the $50\,\Omega$ resistors pair, are presented in Fig. 4.15. As can be observed, the edge analysis reveals no evidence of ringing or instability phenomena. Moreover, the output signal amplitudes were evaluated across different input voltage steps and a linear fit was performed on these data. Dividing the difference between the simulated and expected amplitudes by the input voltage range, the non-linearity factors of Fig. 4.16 were obtained. When focusing the analysis to the $15\,\mathrm{MeV}$ energy range, which is of interest for the high-resolution gamma spectroscopy experiments, the non-linearity factors of Fig. 4.17 were found. As can be observed, the integral non-linearity factor is lower than 0.04 ‰.

Since the detector capacitance has a direct impact on the CSP loop gain, we examined how C_d affects the preamplifier performance. Higher capacitance values generally slow down the preamplifier response, whereas lower values may introduce undesired ringing or even cause instability. To investigate this behavior, the circuit transient response and loop gain were analyzed for different detector capacitance values, as shown in Fig.

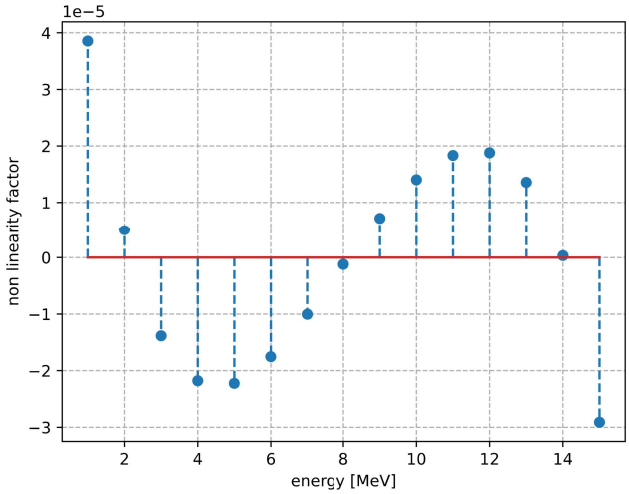

Figure 4.17: Non-linearity factors over the $15\,\mathrm{MeV}$ energy range of interest for the high-resolution gamma spectroscopy experiments. An integral non linearity factor lower than 0.04 ‰ was found.

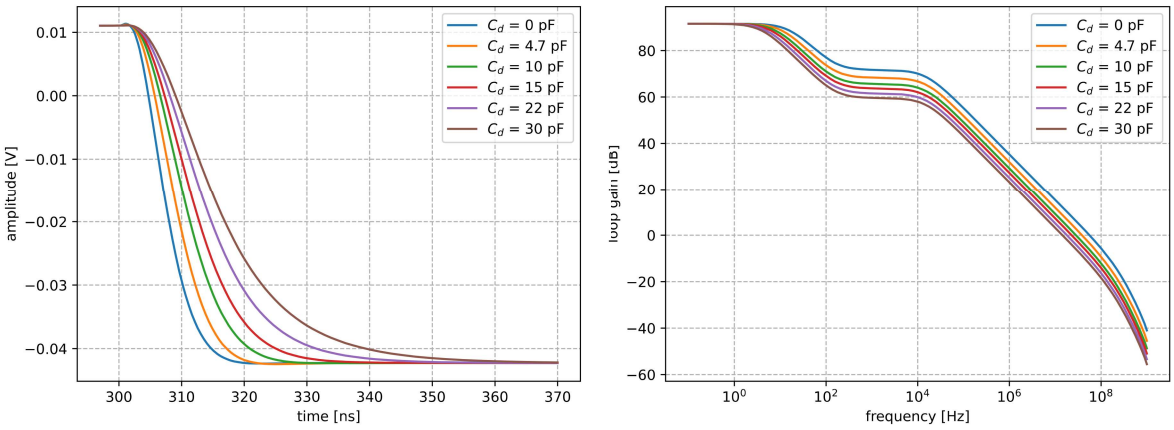

Figure 4.18: Post-layout simulations of amplitude and loop gain for different values of detector capacitance.

4.18. As can be seen, neither instability nor ringing effects occur even when C_d is set to zero. For completeness, Tab. 4.1 reports the CSP rise-time and phase margin for each simulated value of C_d.

4.2.2 Noise and Resolution

To evaluate the equivalent noise charge and resolution of the charge sensitive preamplifier designed, the behavioral description of the ORTEC-572 shaping amplifier was imported on the Cadence Virtuoso simulation environment. A dedicated block was created and connected to the CSP output node to emulate the shaping stage. This block operates by referencing a Verilog-A implementation of the shaper's transfer function.

Simulations were performed by applying voltage steps of $54\,\mathrm{mV}$ to the test capacitor, corresponding to an injected energy, E_{inj}, equal to $1\,\mathrm{MeV}$. The equivalent noise charge (ENC) was then evaluated for various shaping times using Eq. 3.63. From the equivalent

C_d [pF]	0	4.7	10	15	22	30
rise-time [ns]	9.0	10.6	12.9	15.4	19.4	24.3
phase margin	67.3°	72.7°	76.5°	79.9°	81.1°	82.8°

Table 4.1: Rise-time and phase margin post-layout simulations for different values of detector capacitance.

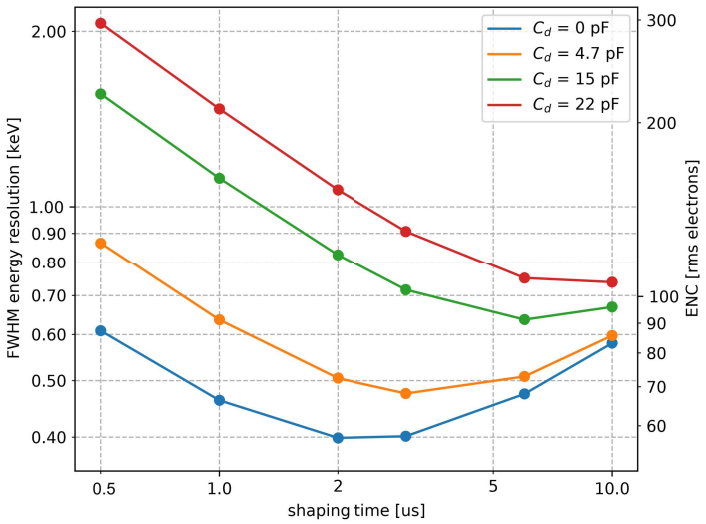

Figure 4.19: Post-layout simulations of equivalent noise charge and energy resolution, performed under typical process corner conditions. The charge-sensitive preamplifier (CSP) was connected to a custom block emulating the ORTEC-572 shaping amplifier.

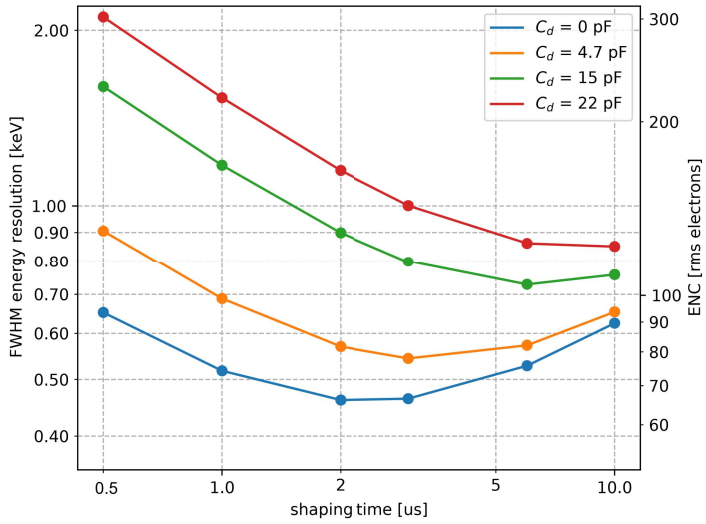

Figure 4.20: Post-layout simulations of equivalent noise charge and energy resolution, performed under the worst noise process corner conditions. The charge-sensitive preamplifier (CSP) was connected to a custom block emulating the ORTEC-572 shaping amplifier.

shaping time [μs]		0.5	1	2	3	6	10
C_d = 0 pF	RES_{fwhm} [keV]	0.61	0.46	0.40	0.40	0.47	0.58
	ENC [e^-_{rms}]	87	66	57	58	68	83
C_d = 4.7 pF	RES_{fwhm} [keV]	0.87	0.64	0.50	0.48	0.51	0.60
	ENC [e^-_{rms}]	124	91	72	68	73	85
C_d = 15 pF	RES_{fwhm} [keV]	1.56	1.12	0.83	0.72	0.63	0.67
	ENC [e^-_{rms}]	224	161	119	103	91	96
C_d = 22 pF	RES_{fwhm} [keV]	2.07	1.47	1.07	0.91	0.75	0.74
	ENC [e^-_{rms}]	296	211	153	130	108	106

Table 4.2: Equivalent noise charge and energy resolution under typical (mean) process corner conditions.

shaping time [μs]		0.5	1	2	3	6	10
C_d = 0 pF	RES_{fwhm} [keV]	0.65	0.52	0.46	0.4 6	0.53	0.62
	ENC [e^-_{rms}]	93	74	66	66	75	89
C_d = 4.7 pF	RES_{fwhm} [keV]	0.91	0.69	0.57	0.54	0.57	0.65
	ENC [e^-_{rms}]	129	98	81	77	82	93
C_d = 15 pF	RES_{fwhm} [keV]	1.60	1.17	0.90	0.80	0.73	0.76
	ENC [e^-_{rms}]	230	168	129	115	104	109
C_d = 22 pF	RES_{fwhm} [keV]	2.11	1.53	1.15	1.00	0.86	0.85
	ENC [e^-_{rms}]	302	220	165	144	124	122

Table 4.3: Equivalent noise charge and energy resolution under the worst noise process corner conditions.

noise charge, the circuit FWHM energy resolution was finally calculated:

$$RES_{FWHM} = 2.355 \cdot \frac{E_{inj}}{Q_{inj}} ENC \tag{4.25}$$

In this expression, Q_{inj} is the injected charge corresponding to the $1\,\mathrm{MeV}$ interaction.

Fig. 4.19 and Tab. 4.2 report the values of ENC and energy resolution for different detector capacitances under typical process corner conditions. In contrast, Fig. 4.20 and Tab. 4.3 present the corresponding values obtained under the worst noise process corner conditions. As observed, in both cases, when considering shaping times of $6\,\mu\mathrm{s}$ or $10\,\mu\mathrm{s}$, FWHM energy resolutions below $1\,\mathrm{keV}$ were achieved, even with detector capacitances of $15\,\mathrm{pF}$ or $22\,\mathrm{pF}$. This is an excellent result, making our circuit fully comparable to state-of-the-art discrete-component solutions used in gamma spectroscopy experiments [42][47]. Furthermore, being integrated, our circuit also offers the advantages of reduced power consumption and minimal area occupation.

We now analyze the post-layout simulations of the preamplifier input-referred power spectral density, reported in Fig. 4.21. The curves were fitted using the functional form described in Eq. 3.58. This allowed the extraction of the fit coefficients a, b and c, defined in Eq. 3.59, for various detector capacitance values.

The white parallel noise coefficient a does not depend on C_d and is equal to $1.66 \times 10^{-29}\,\mathrm{A^2\,Hz^{-1}}$, as expected from its theoretical definition.

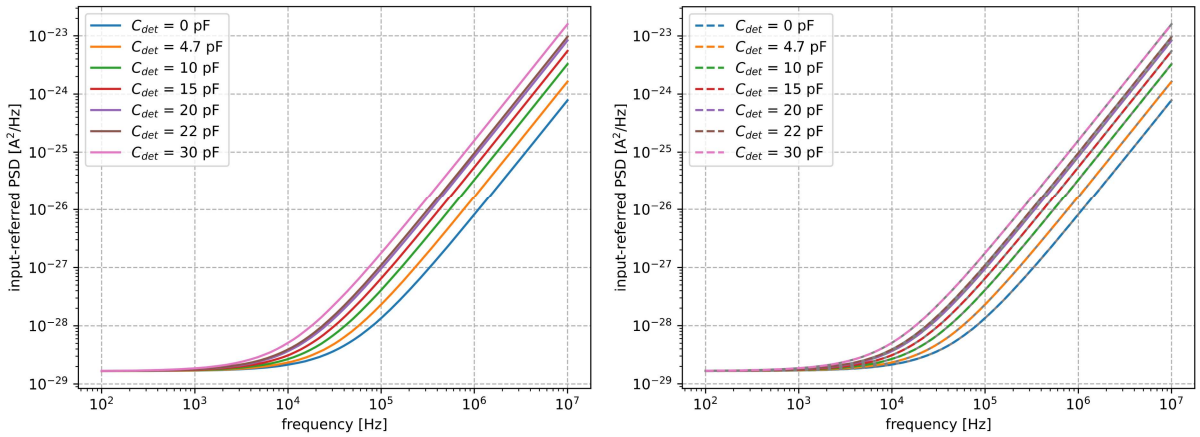

Figure 4.21: On the left, post-layout simulations of the CSP input-referred power spectral density. On the right, fit curves superimposed on the simulation data.

The flicker noise coefficient b, instead, is expected to show a quadratic dependence on the total input-referred capacitance. As previously discussed, this includes not only the detector capacitance, but also the feedback capacitance, the test capacitance and the intrinsic input capacitance of the circuit:

$$b = (2\pi C)^2 \cdot A_f = (2\pi)^2 \cdot A_f \cdot [(C_d + C_f + C_t) + C_{in}]^2 \tag{4.26}$$

Since C_f, C_t and C_d are known, we can fit this expression with the following function:

$$y = k \cdot (x + p)^2 \tag{4.27}$$

where x = $C_d + C_f + C_t$, y = b and the parameters k and p are the fit coefficients. By comparing this expression to the theoretical model, we can observe that the coefficient k corresponds to $(2\pi)^2 A_f$, while the parameter p corresponds to the unknown input capacitance. The results of this fit procedure are shown on the left side of Fig. 4.22. The mismatch between data and fitting curve may suggest that additional effects are not accounted for in the model we presented. Specifically, possible second-stage noise sources originating from the line-driver input transistor are neglected. To assess their impact on noise and resolution, we can consider the circuit shown in Fig. 4.23. The relationship between the voltage noise source, v_n, and the resulting feedback current, i_n, is described by the following equation:

$$i_n = \frac{1 + sC_f R_f}{R_f} v_n \longrightarrow i_n^2 = \frac{1 + (2\pi)^2 f^2 C_f^2 R_f^2}{R_f^2} \cdot v_n^2 \tag{4.28}$$

Over the frequency range of interest, 5×10^3 Hz $\leq f \leq 5 \times 10^4$ Hz, we can assume:

$$(2\pi)^2 f^2 C_f^2 R_f^2 \gg 1 \tag{4.29}$$

Thus, we can write:

$$S_{in}(f) = i_n^2 = \frac{(2\pi)^2 f^2 C_f^2 R_f^2}{R_f^2} \cdot v_n^2 = (2\pi)^2 C_f^2 f^2 \cdot v_n^2 \tag{4.30}$$

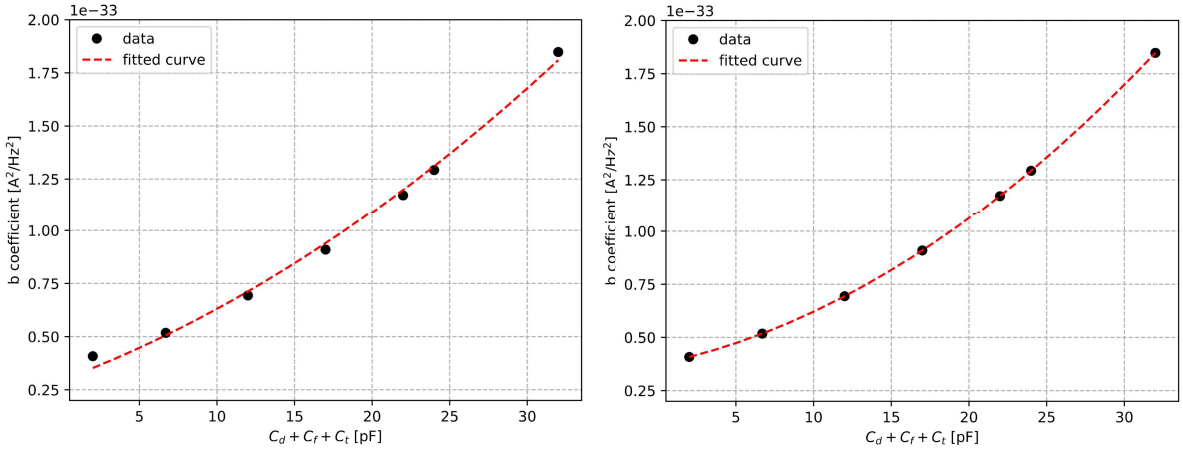

Figure 4.22: Fit of the b coefficients of the input-referred power spectral density using the curve $y = k \cdot (x + p)^2$ on the left and the curve $y = k \cdot (x + p)^2 + q$ on the right. As can be seen, this last curve closely matches the circuit simulation data, suggesting the presence of an additional second-stage noise contribution.

Considering the flicker noise contribution from the input transistor of the line-driver, $v_n^2 = A'_f/f$, we obtain the following result:

$$S_{in}(f) = (2\pi)^2 C_f^2 A'_f \cdot f \tag{4.31}$$

As can be observed, the flicker noise component of the line-driver input transistor overlaps perfectly with the corresponding one of the preamplifier input transistor, allowing us to rewrite the flicker noise coefficient b as follows:

$$b = (2\pi)^2 \cdot A_f \cdot [(C_d + C_f + C_t) + C_{in}]^2 + (2\pi)^2 C_f^2 A'_f \tag{4.32}$$

As a consequence, we can fit this coefficient with the following function:

$$y = k \cdot (x + p)^2 + q \tag{4.33}$$

The right side of Fig. 4.22 reports the outcome of the new fitting procedure. Since the coefficient p corresponds to C_{in}, we can find its value: C_{in} = 7.7 pF. This result is consistent with the approximate estimation given in Eq. 4.15. On the other side, we can determine, from the fit coefficients k and q, the flicker noise parameter of the CSP input transistor, A_f, and that of the line-driver input transistor, A'_f: A_f = 2.46 × 10^{-14} V^2, A'_f = 8.11 × 10^{-12} V^2.

The white series noise coefficient, c, is also expected to exhibit a quadratic dependence on the total input-referred capacitance:

$$c = (2\pi)^2 \frac{4kT\gamma}{g_m} (C_d + C_f + C_t + C_{in})^2 \tag{4.34}$$

Since we know C_{in} from the previous analysis, we can fit this coefficient with the following function:

$$y = k \cdot x^2 \tag{4.35}$$

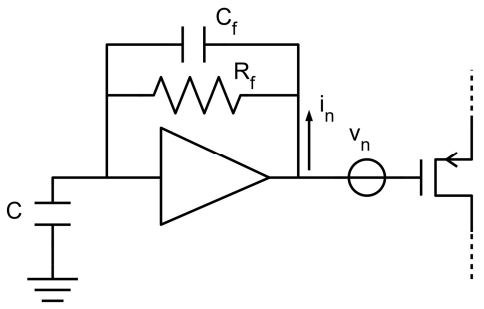

Figure 4.23: Circuit used to refer the flicker noise contribution of the line driver to the input node of the charge-sensitive preamplifier.

where y = c, x = $C_d + C_f + C_t + C_{in}$ and the fit coefficient k is equal to $4kT\gamma(2\pi)^2/g_m$. The outcomes of this fit procedure are illustrated on the left side of Fig. 4.24. As before, the mismatch between data and fitting curve may suggest that additional effects are not accounted for in our simple fitting model.

It is worth considering whether the input transistor of the line driver contributes with its white series noise. If so, it would be necessary to replace v_n^2 with $4kT\gamma(2\pi)^2/g'_m$ in Eq. 4.30, to find:

$$c = (2\pi)^2 \frac{4kT\gamma}{g_m}(C_d + C_f + C_t + C_{in})^2 + (2\pi)^2 C_f^2 \frac{4kT\gamma}{g'_m} \tag{4.36}$$

In this equation, g'_m is the line-driver input transistor transconductance. We can therefore fit the data using a curve similar to that shown in Eq. 4.33. However, this approach yields negative values of q, which have no physical meaning. We must therefore consider what other elements might be contributing within our circuit. To this end, let us consider the role of the ESD protection resistor, as illustrated in Fig. 4.25. We can write:

$$\begin{cases} i_n = \dfrac{v_x}{R_{esd}} \\ i_n = -s \cdot (C_d + C_t)(v_n + v_x) \end{cases} \tag{4.37}$$

By solving this system, we obtain:

$$i_n = -\frac{s(C_d + C_t)}{1 + s \cdot (C_d + C_t)R_{esd}} \tag{4.38}$$

which, in squared magnitude, becomes

$$i_n^2 = \frac{(2\pi)^2(C_d + C_t)^2 f^2}{1 + (2\pi)^2(C_d + C_t)^2 R_{esd}^2 f^2} \cdot v_n^2 \tag{4.39}$$

Since the frequency range of interest is $f > 10^5$ Hz, $C_d + C_t < 30$ pF and $R_{esd} < 100\,\Omega$, we can assume $(2\pi f)^2(C_d + C_t)^2 R_{esd}^2 \ll 1$. Thus we can write the ESD protection resistance contribution to the input-referred power spectral density as:

$$S_{in}(f) = i_n^2 = (2\pi)^2(C_d + C_t)^2 v_n^2 \cdot f^2 \tag{4.40}$$

This noise component overlaps perfectly with the white series one of the preamplifier input transistor, allowing us to rewrite the noise coefficient c as follows:

$$c = (2\pi)^2 \frac{4kT\gamma}{g_m}(C_d + C_f + C_t + C_{in})^2 + (2\pi)^2 4kTR_{esd}(C_d + C_t)^2 \tag{4.41}$$

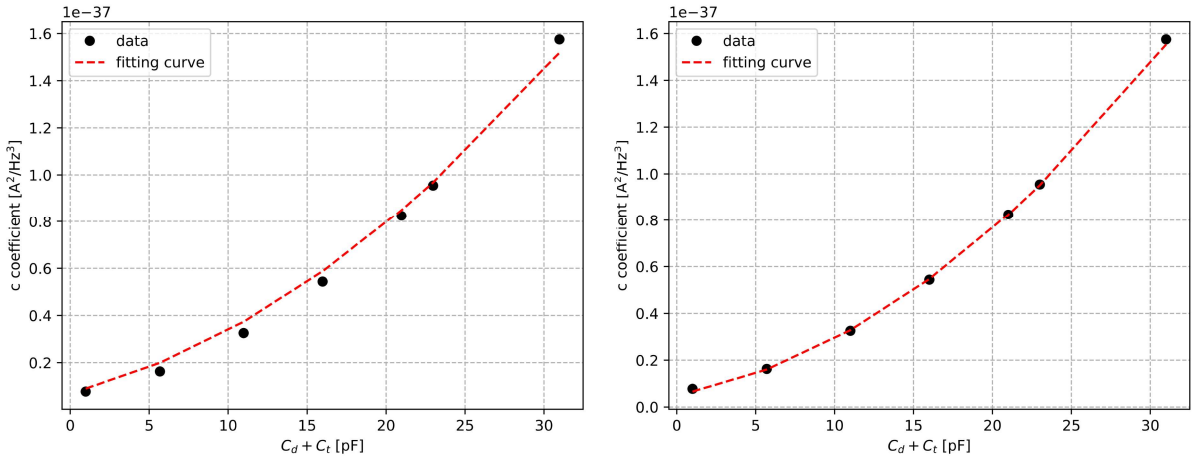

Figure 4.24: Fit of the white series noise coefficients c using the curve $y = k \cdot x^2$ on the left and the curve $y = \alpha \cdot (x + q)^2 + \beta \cdot x^2$ on the right. As shown, the latter provides an excellent match to the simulation data, suggesting an additional noise contribution due to the ESD protection resistor and the poly-silicon plane between it and the input transistor gate.

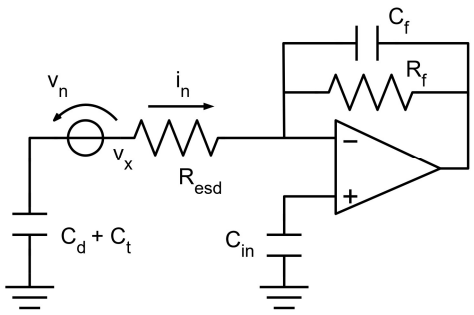

Figure 4.25: Circuit used to refer the noise contribution of the ESD protection resistance to the input node of the charge-sensitive preamplifier.

As a consequence, we can fit this coefficient with the function:

$$y = \alpha \cdot (x + q)^2 + \beta x^2 \tag{4.42}$$

where y = c, x = $C_d + C_t$, q is the known parameter $C_f + C_{in}$ and α and β are the fit coefficients. The right side of Fig. 4.24 reports the outcome of the new fitting procedure. From α, we derive a value of g_m equal to $6.2\,\mathrm{mS}$, which is lower than the one predicted at the end of Sec. 4.1.1. From β, on the other hand, we obtain the following value of resistance: $R_{esd} = 68\,\Omega$. It is evident that this value deviates from the $30\,\Omega$ used for the ESD protection. Although the precision of low-ohmic-value resistors is not guaranteed by the foundry, this discrepancy suggests the need to identify a potential source of additional input resistance in the circuit. We are confident that the source of this excess resistance lies in the poly-silicon plane placed between the gate of the input transistor of the preamplifier and the ESD protection resistor (dashed red rectangle of Fig. 4.10). This layer was introduced as part of the design strategy to mitigate the flicker noise contribution and its presence remains beneficial for improving the overall resolution of the circuit.

To further investigate the impact of different noise sources, we finally analyze the individual contributions to the equivalent noise charge for a $15\,\mathrm{pF}$ detector capacitance

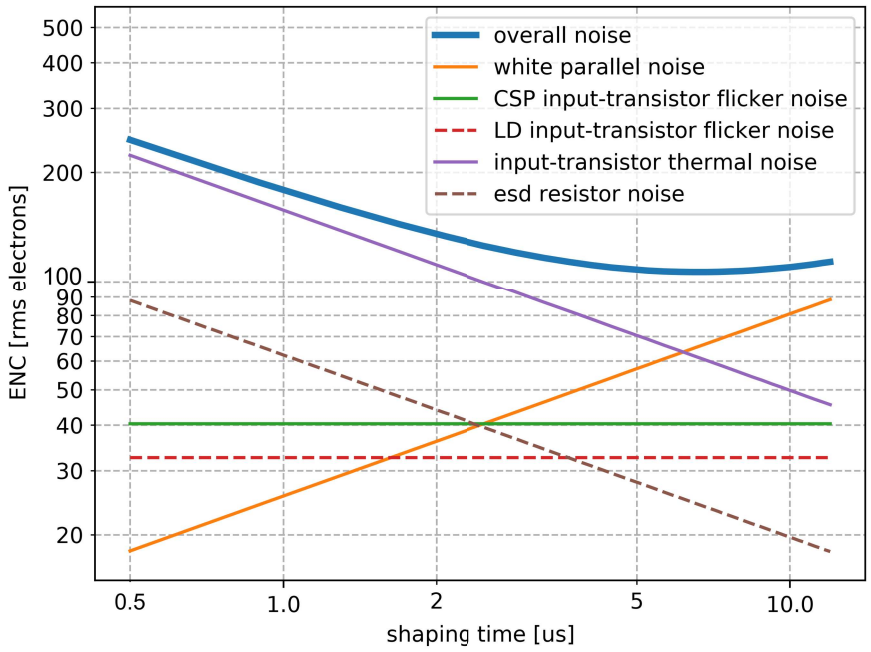

Figure 4.26: Individual noise contributions to the equivalent noise charge for a 15 pF detector capacitance and a simulated ORTEC 572 quasi-Gaussian shaping amplifier. The flicker noise from the line-driver input transistor is smaller but comparable to that of the preamplifier input transistor, while the protection resistor and the poly-silicon plane contribute only minimally to the series white noise.

and an ORTEC 572 quasi-Gaussian shaping amplifier. The results are shown in Fig. 4.26. As observed, the flicker noise contribution from the line-driver input transistor is smaller, yet still comparable to that of the CSP input transistor. In contrast, the contributions from the protection resistor and the poly-silicon plane introduced during layout have a relatively minor effect on the series white noise. These findings emphasize the relative significance of each noise source in determining the overall noise performance and provide useful guidance for both device design and layout optimization strategies.

4.3 Experimental Results

The chip was submitted to the foundry in early July 2024 and was received in February 2025. In Fig. 4.27 the die glued and wire bonded on a PTFE substrate is shown.

The charge sensitive preamplifier optimized for hole-collecting electrodes, described in the previous sections, was characterized on a dedicated test bench similar to the one used for the simulations (Section 4.2) and implemented on a two-layers printed circuit board (PCB). This PCB, made of a PTFE substrate, was directly realized in our laboratory by combining toner transfer and chemical etching techniques. The ASIC was directly glued on the PCB using a bi-component epoxy adhesive and wire bonded. This operation was carried out using a 4123 manual wedge-bonder from Kulicke and Soffa Industries, which was set-up and operated in-house. Silicon-aluminum alloy wires with a diameter of 25 µm were employed. Fig. 4.28 illustrates the PCB with the CSP test circuit.

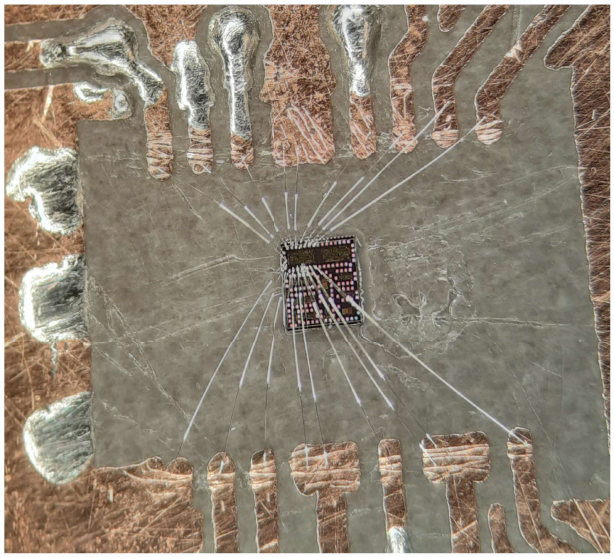

Figure 4.27: Optical microscope image of the ASIC bonded onto a PTFE substrate. The ASIC integrates multiple charge sensitive preamplifiers, including different versions optimized for either positive or negative polarity signals, with both single-ended and differential output.

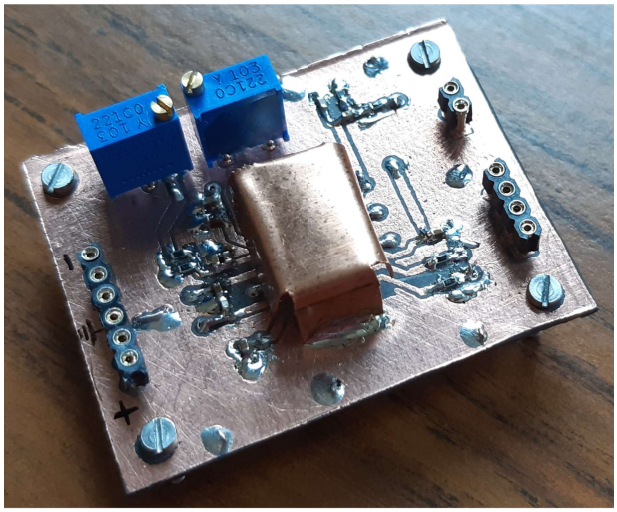

Figure 4.28: Photograph of the PCB used to test the charge sensitive preamplifier optimized for hole-collecting electrodes. The circuit is shielded by a small copper cover, which protects the bonding wires and acts as a Faraday cage. The bias voltages for nodes V_{cas} and V_{bias} are derived by partitioning the negative supply voltage using two trimmer resistors. The bottom side of the PCB houses the power supply decoupling capacitors and the 1 GΩ feedback resistor, which is close to the input node to minimize the copper connections parasitic effects.

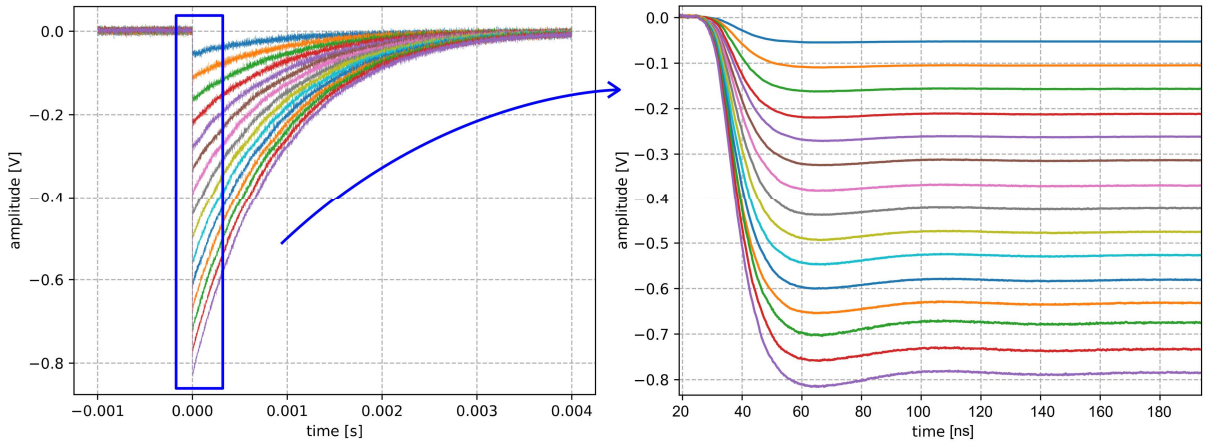

Figure 4.29: CSP output waveforms for injected pulses with equivalent energy between $1\,\mathrm{MeV}$ and $15\,\mathrm{MeV}$. A $15\,\mathrm{pF}$ detector capacitor was connected between the input node of the circuit and ground. The left panel shows the full signal shape, while the right panel zooms in on the falling edges. A slight ripple is visible, however the overall signal integrity is maintained.

4.3.1 Dynamic Range and Linearity

The circuit operates with a power consumption of $25.2\,\mathrm{mW}$ and achieves an equivalent dynamic range of $21\,\mathrm{MeV}$. Fig. 4.29 shows the CSP output waveforms for input pulses corresponding to equivalent energies between $1\,\mathrm{MeV}$ and $15\,\mathrm{MeV}$, which represent the range of interest for gamma spectroscopy experiments. A zoom on the falling edges of the signals reveals a slight ripple that doesn't compromise their integrity and the circuit resolution.

To evaluate the CSP linearity, we employed the electronic chain illustrated in Fig. 4.30. A model PB-5 high-precision pulse generator from Berkeley Nucleonics Corporation was matched and connected to the test capacitor to generate delta-like current pulses to be injected into the preamplifier. The preamplifier output node was then routed to an ORTEC-572 quasi gaussian shaping amplifier, followed by an ORTEC-926-M32 Multi Channel Analyzer (MCA), which was interfaced with a PC via USB. Energy-equivalent pulses in the range between $1\,\mathrm{MeV}$ and $15\,\mathrm{MeV}$ were generated, and the corresponding signal amplitudes at the output of the shaper were acquired and digitized. A linear fit was then performed on these data. Following the procedure described in Sec. 4.2.1, the differences between the expected and measured values were evaluated and normalized to the whole dynamic range. This method allowed us to evaluate the non-linearity factors of Fig. 4.31. The circuit shows an integral non-linearity factor lower than 0.3 ‰ over the $15\,\mathrm{MeV}$ equivalent range. Finally, Tab. 4.4 summarizes the measured rise times corresponding to various detector capacitances. These values are higher than the corresponding simulated ones, possibly due to the parasitic capacitance of the PCB substrate where the ASIC is mounted and tested: this parameter, in fact, is not accounted for in the simulation software. Moreover, we can neglect the rise-time of the precision pulse generator used.

4.3.2 Noise and Resolution Measurements

To evaluate the CSP equivalent noise charge and resolution, the circuit was connected to an ORTEC-572 quasi gaussian shaping amplifier. $1\,\mathrm{MeV}$ equivalent pulses were injected into the CSP through the test capacitor. For different values of detector capacitance C_d

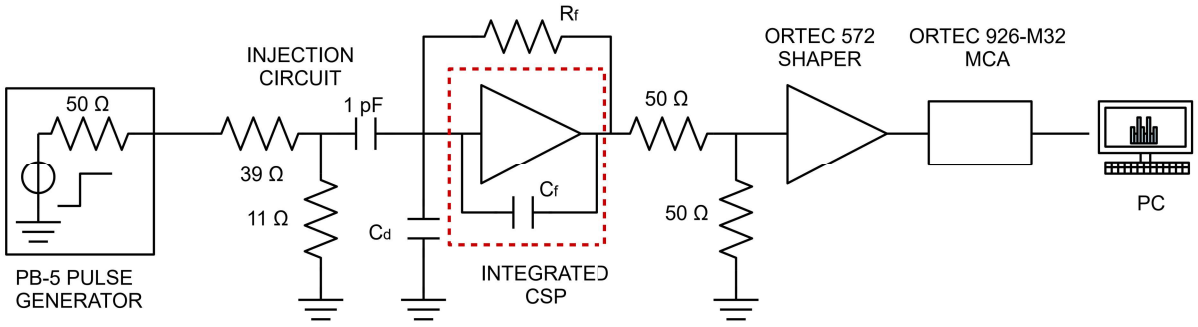

Figure 4.30: Electronic chain used to evaluate the linearity performance of our integrated charge sensitive preamplifier. It includes a high-precision model PB-5 pulse generator from Berkeley Nucleonics Corporation, an ORTEC-572 shaping amplifier and an ORTEC-926-M32 Multi Channel Analyzer (MCA).

C_d [pF]	0	4.7	15	22
measured rise-time [ns]	18.8	19.9	22.8	25.2
simulated rise-time [ns]	9.0	10.6	15.41	19.35

Table 4.4: Measured and simulated rise-times for different values of detector capacitance.

and shaping time τ, the amplitudes V_{shaper} of the shaper output signals were measured, along with the noise root mean square values, $V_{noise}(rms)$. Based on the signal-to-noise ratio definition given in Eq. 3.61, the ENC was calculated using the following relation:

$$\frac{V_{shaper}}{V_{noise}(rms)} = \frac{Q_{inj}}{ENC} \tag{4.43}$$

In this expression, Q_{inj} represents the charge injected into the CSP, which corresponds to $3.4 \cdot 10^5$ electrons, as described at the beginning of Sec. 4.2. Using the ENCs values, the associated CSP full width at half maximum (FWHM) energy resolution was calculated for the different capacitances C_d and shaping times τ according to Eq. 4.25. The experimental results, which are consistent with the simulations previously discussed, are reported in Tab. 4.5 and Fig. 4.32.

shaping time [μs]		0.5	1	2	3	6	10
C_d = 0 pF	RES$_{fwhm}$ [keV]	0.55	0.49	0.50	0.50	0.56	0.64
	ENC [e^-_{rms}]	78	70	70	71	80	91
C_d = 4.7 pF	RES$_{fwhm}$ [keV]	0.81	0.69	0.63	0.61	0.65	0.70
	ENC [e^-_{rms}]	115	98	90	87	93	101
C_d = 15 pF	RES$_{fwhm}$ [keV]	1.41	1.15	0.93	0.85	0.76	0.75
	ENC [e^-_{rms}]	202	164	133	122	109	108
C_d = 22 pF	RES$_{fwhm}$ [keV]	1.80	1.45	1.16	1.03	0.89	0.86
	ENC [e^-_{rms}]	259	208	166	147	127	123

Table 4.5: CSP equivalent noise charge and energy resolution measurements. The circuit was mounted and tested on a PTFE-based PCB. 1 MeV equivalent pulses were injected and an ORTEC-572 shaping amplifier was connected to the CSP output.

For a 15 pF detector capacitance, an equivalent noise charge of 109 rms electrons was measured with a 6 µs shaping time, corresponding to a relative energy resolution

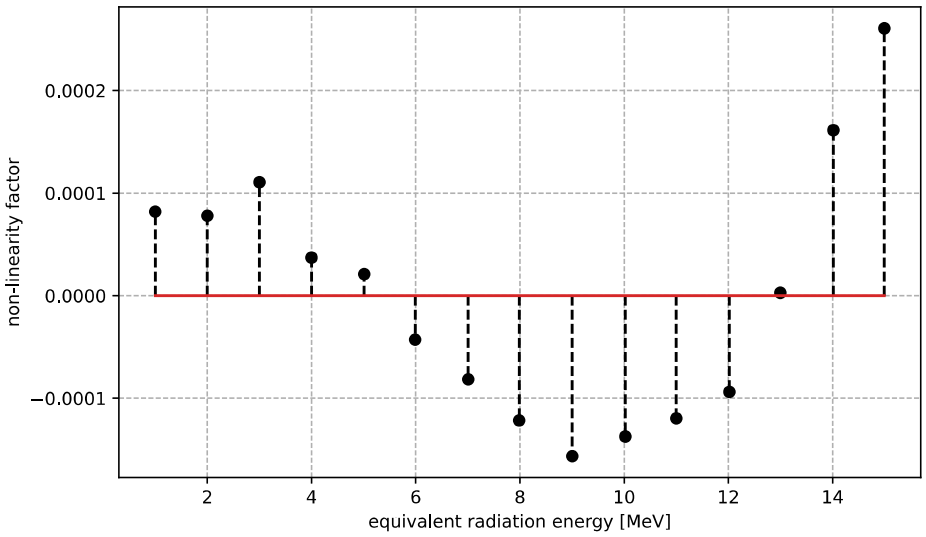

Figure 4.31: Measured non-linearity factors over the 15 MeV equivalent energy range of interest for the high-resolution gamma spectroscopy experiments. An integral non linearity factor lower than 0.3 ‰ was found.

of 0.76 ‰ at 1 MeV. Increasing the shaping time to 10 µs led to a slightly lower ENC of 108 rms electrons, with a relative resolution of 0.75 ‰. These are excellent results for gamma-ray spectroscopy with high-purity germanium detectors and demonstrate the high performance of the developed front-end electronics. As a matter of fact, if we considered an ideal detector, its intrinsic energy resolution would be only limited by the statistical fluctuations of the ionization process, and thus described by the Fano law[8]. For 1 MeV interactions, we would find:

$$\sigma_{Fano} = \sqrt{F \cdot N} = \sqrt{0.13 \cdot \frac{10^6\,\mathrm{eV}}{2.96\,\mathrm{eV}}} = 209\ e^- \tag{4.44}$$

Since the overall energy resolution is given by the quadratic sum of the detector's intrinsic resolution and the contribution from the read-out electronics (see Eq. 3.64), the fact that the equivalent noise charge measured in our system is only half that of the ideal detector clearly demonstrates the excellent performance of our charge sensitive preamplifier. This result underscores the effectiveness of our circuit design in minimizing electronic noise and highlights the high level of optimization achieved.

Even when increasing the detector capacitance to 22 pF the system maintains outstanding performance at typical spectroscopic shaping times: the ENC remains below 130 rms electrons, corresponding to a relative energy resolution better than 0.9 ‰.

The results obtained with our circuit were also compared, for a 15 pF detector capacitance, with those achieved using the discrete-component preamplifier designed for the PANDORA experiment [42]. As shown by the data in Tab. 4.6 and the plots in Fig. 4.33, our CSP is fully comparable with state-of-the-art solutions.