Quality assurance and testing of the ATLAS Liquid argon Calorimeter Power Distribution Board

UR: Milano Statale

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INTRODUCTION

At CERN, located in Genève in Switzerland, very important experiments are installed and are working since 2009. These experiments have led to significant advances in understanding the physics of elementary particles also denoted as High Energy Physics (HEP). The cited experiments are able to operate powerful proton-proton collider, which works since 2009, to obtain increasing performance. To increase even more our knowledge of the fundamental constituents of matter and their interactions, the research programs at CERN provide a continuous update of the Large Hadron Collider (LHC), the experiments to carry out investigations in new areas before not investigated but also, secondarily, it becomes mandatory a continuously updated of electronics that otherwise could not work with the new levels of luminosity.

ATLAS is a very complex experiment and it has been designed and built to detect very high energetic events. It has observed a particle as massive as the Higgs boson. A very important measurements have been obtained by the detector which consists of three main sub-systems: the inner tracking system, the calorimeter and the muon spectrometer. The description of the Calorimeter can be found in the papers and documents in literature and is here briefly reported for sake of completeness (this description is so very similar to the ones that it is possible to read on many other and more specific papers). The calorimeter system is composed of sampling detectors and is housed in one barrel and two endcap cryostats. The barrel is made of a LAr Electromagnetic Calorimeter (often denoted as EC), surrounded by a hadronic calorimeter made of steel and scintillating tile (often denoted TileCal). In the endcap region of the detector all of the calorimetry uses LAr as the active material. The EC is made of alternating layers of accordion–shaped lead absorbers and electrodes. Liquid argon is than insert between these layers and act as active medium. Interactions in the absorbers transform the incident energy into a shower of particles that are detected by the sensing element. Finally, by means a complex analysis of the signals coming from all detectors, it is possible to evaluate the energies of the particles generated from the collision event.

Definitively, the LAr calorimeter of the ATLAS experiment, located at the Large Hadron Collider (LHC) in Geneva, is a very complex apparatus as shown in **Fig. 1**.

It is designed to precisely detect very high energetic events. It has observed a particle as massive as the Higgs boson, i.e. near 125 GeV. The electronic readout structure is very complicated since it has to process the detector's output data at very high speeds. Particular attention should be devoted to the LAr electromagnetic calorimeter and the front-end electronics that are the settings of this project.

Beams of particles from the LHC collide at the center of the ATLAS detector making collision debris in the form of new particles, which fly out from the collision point in all directions. The different detectors placed around the collision point are designed to record the paths, momentum, and energy of the particles, allowing them to be individually identified.

Each detector has its own electronic chain associated so that different information on the particle can be reconstructed (momentum, direction, energy, ...).

Radiation exposure in the experiment is very consistent as well, and is composed of ionizing and non-ionizing particles, constituting a very hostile environment for electronics and in particular for programmable logic devices.

Inside the LHC, bunches of up to 10^{11} protons (p) will collide 40 million times per second to provide 14 TeV proton-proton collisions at a design luminosity of 10^{34} $cm^{-2}s^{-1}$. The LHC will also collide heavy ions, in particular lead nuclei, at 5.5 TeV per nucleon pair, at a design luminosity of 10^{27} $cm^{-2}s^{-1}$.

The experiment is under continuous development to measure more precisely the parameters of interest in order to effectively search for new physics phenomena and validate models for physics beyond the Standard Model (SM).

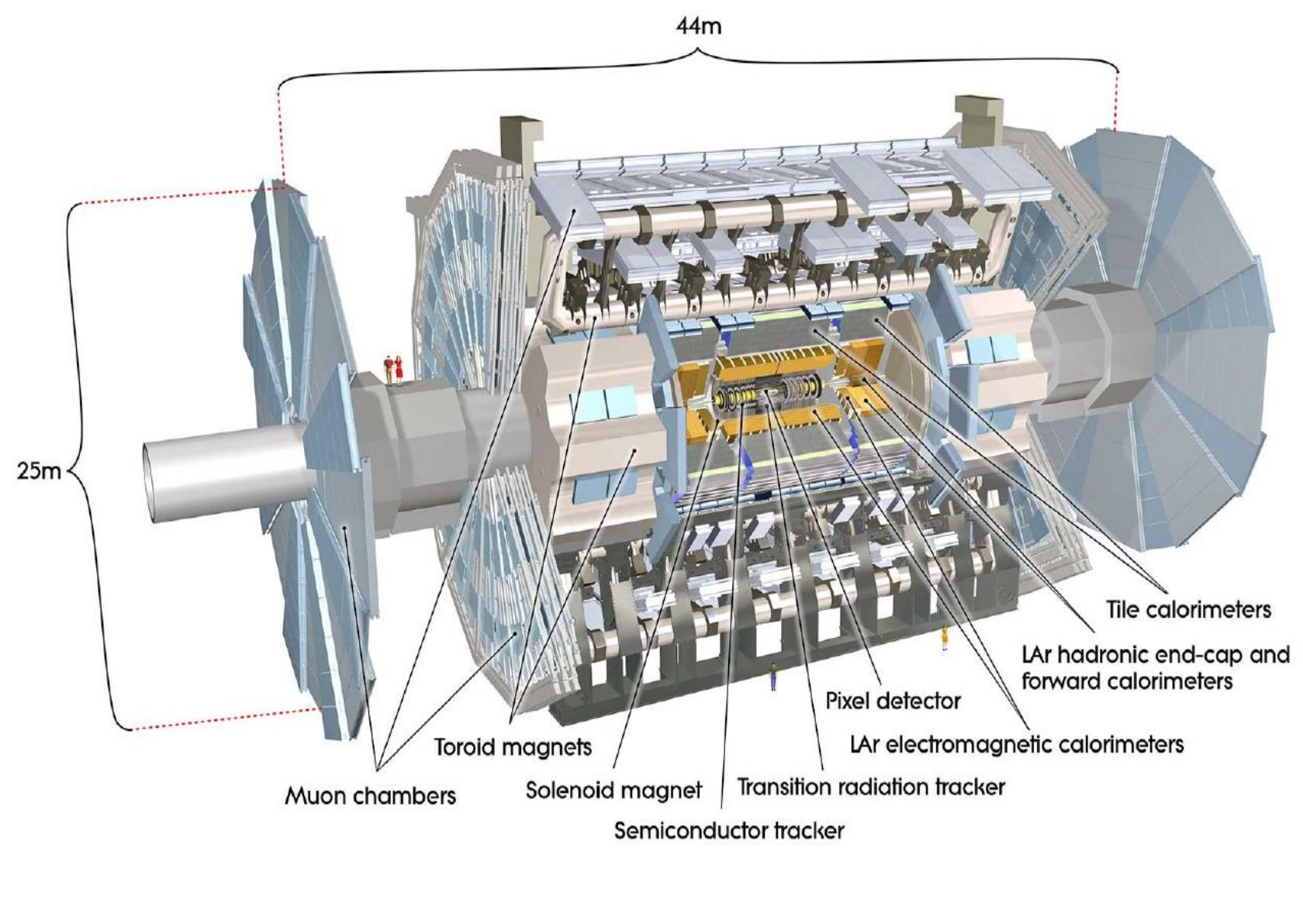

Fig. 1. The main structure of the ATLAS experiment.

After the 2015-2018 data taking campaign (Run 2), an upgrade plan (Phase-I upgrade) started to enhance the physics reach of the experiment during the upcoming operation at increasing LHC luminosities (Run3, started in 2022) **Fig. 2** .

In particular, for the liquid argon calorimeter, to avoid efficiency losses and enhance the physics reach, it was decided to increase the trigger readout granularity by up to a factor of ten, summing the the transverse energy (ET) of calorimeter cells in areas smaller than the previous configuration (these smaller clusters of cells are called Super Cells). In addition, the precision and range of the ET measurement is also increased.

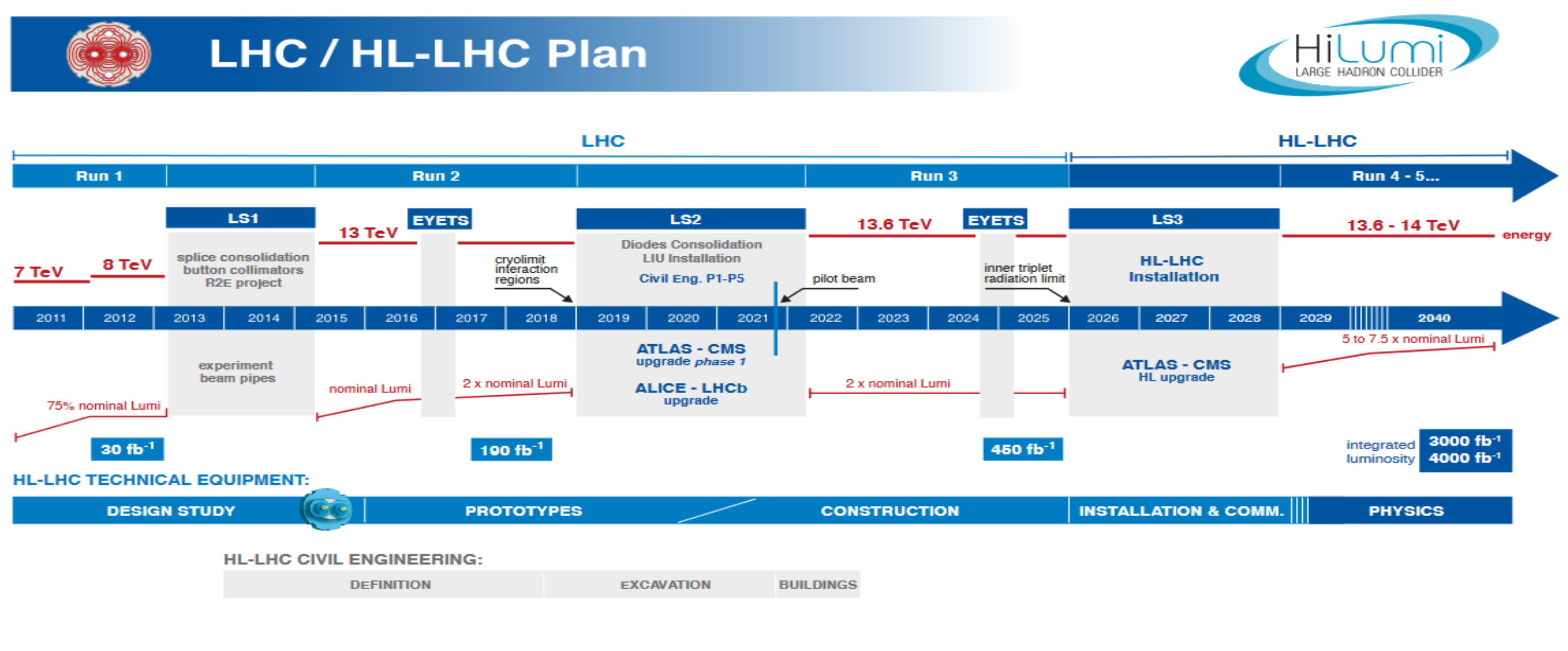

Fig. 2. LHC roadmap to the complete development of the structure. This roadmap is constantly updated

The Lar Trigger Digitizer Board (LTDB) processes and digitizes up to 320 Super Cell signals and transmits them via optical links to the Back-End. Power distribution on the LTDB is provided by the PDB mezzanine card.

POWER DISTRIBUTION BOARD

The choice of developing a separate board for the generation of the supply voltages for the LTDB ensures forward compatibility in the future Phase-II upgrade, for which a different power distribution scheme for the Front-End electronics is planned. The Power Distribution Board (PDB), mounted on the LTDB, uses some of the existing supply voltages as input and converts them to the needed values using LTM4619 DC/DC converters (from Analog Device, Inc.) for the digital part and LHC4913 (positive voltage) and LHC7913 (negative voltage) regulators (from STMicroelectronics) for the analog part. All the PDB produced have been tested in Milano by a custom test board, internally designed and manufactured, controlled by an Arduino. The PDB consists of digital and analog parts to power the corresponding sections of the LTDB. The block diagram of the power scheme is shown in **Fig. 3**. From the +6 V line taken from the Front-End Crate (FEC) power bus, the following voltages are created for the digital part of the LTDB: +1.2V,+1.5V,+2.5V and +3.3V. This is achieved using LTM4619 DC-DC converters. This is a DC-DC μModule regulator operating over input voltage ranges of 4.5 V to 26.5 V and supports two outputs with voltage ranges of 0.8 V to 5 V. It delivers 4 A continuous current (5 A peak) for each output. The analog voltages are generated as follows. From the +7 V(-7 V) of the FEC power bus, the +5 V(-5 V) is generated using the LHC4913 (LHC7913) Low-DropOut (LDO) linear voltage regulator. The LHC4913 is a positive Voltage Regulator that has a fixed output voltages: 2.5 V, 3.0 V, 3.3 V, 5.0 V or 8.0 V and an input voltage ranging from 3 V to 12 V. The LHC7913, instead is a negative Voltage Regulator with an input voltage range from -3 V to -9 V. The LHC4913 is also used to generate +2.5 V, starting from the +6 V of the power bus, (with an intermediate step down at +4 V, using an LTM4916, to avoid a large voltage drop on the LDO). The PDB is radiation tolerant and able to operate in presence of maximum magnetic field expected in the LTDB position (lower than 0.1 T). The radiation tolerance requirements for the PDB are less stringent than for the rest of the LTDB component since the board will have to operate only for the LHC Run 3 and will be replaced before the start of the HL-LHC. The board is manufactured as a ten-layer PCB of 1.6 mm thickness, reinforced with a fiberglass (G10) frame glued on the top side. When mounted on the LTDB motherboard, the total maximum vertical height is about 5.4 mm. One PDB is show in **Fig. 4**. An automated set-up has been developed to test the correctness of all output voltages of the PDBs at full load before they were shipped to LTDB assembly site.

The PDBs passing the tests above are then subjected to a highly accelerated stress screening (HASS) test, where the PDBs are placed in a chamber and undergo ten thermal cycles between 0 °C and 60 °C for about 12 hours. The goal of the HASS test is to find any failures due to component infant mortality, cold solder joints, etc. After HASS testing, each PDB is installed on an LTDB for re-testing, where the voltage of all outputs is measured, control and monitoring signals are tested, and the power rail ramp-up time (from 10 % to 90 % of the rising edge) for the GBTx is measured as well. If the PDB passes this re-testing, it can be used on the LTDB for integration testing. A picture of the PDB mounted on the LTDB is showed in **Fig. 5**.

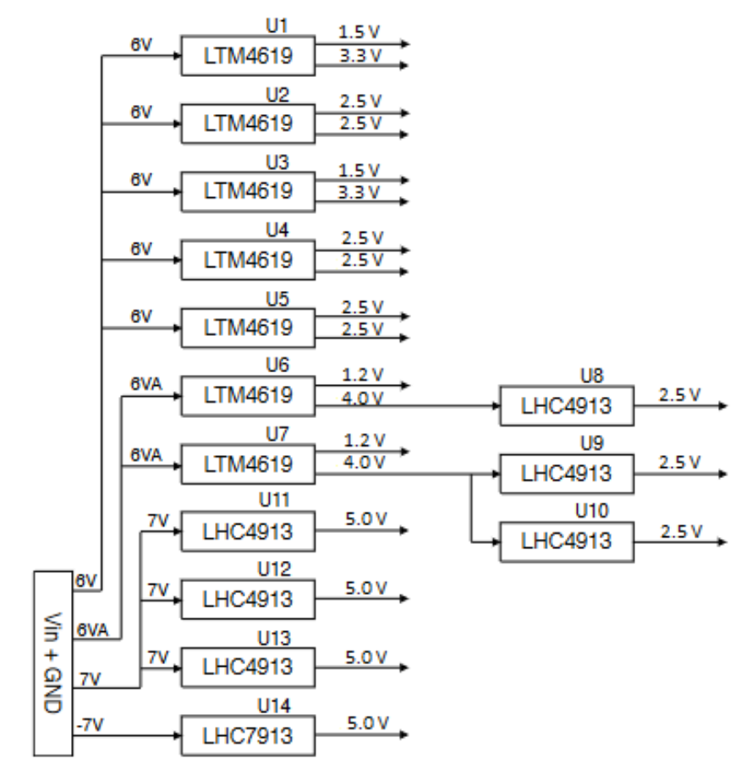

Fig. 3. Power scheme of the PDB

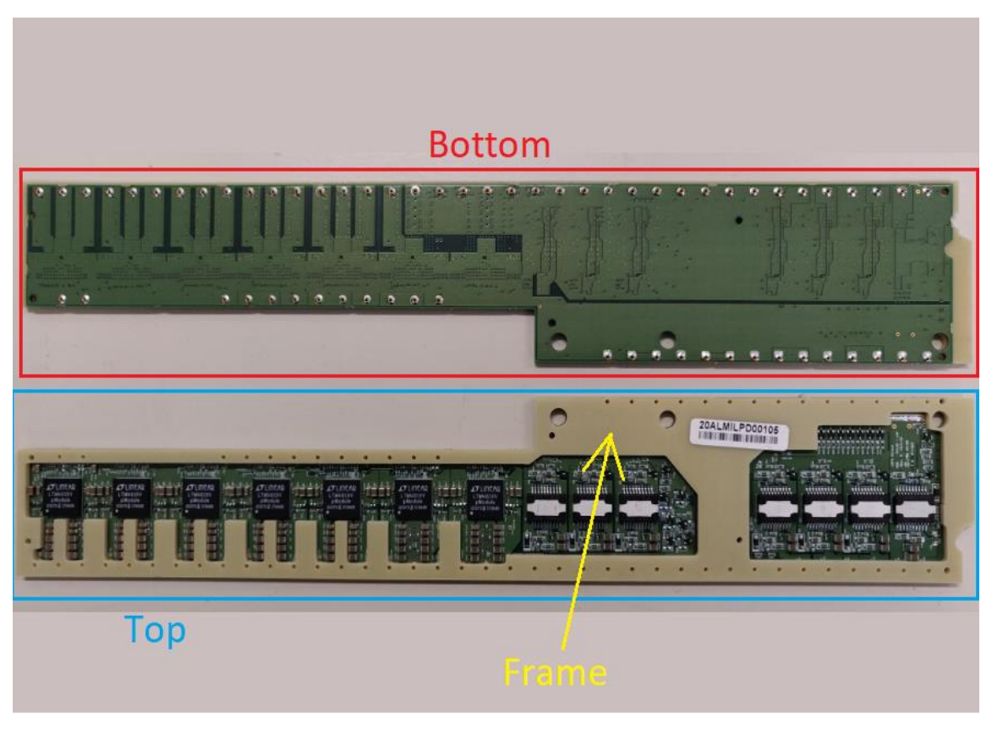

Fig. 4. Picture of a PDB as seen from the top and the bottom.

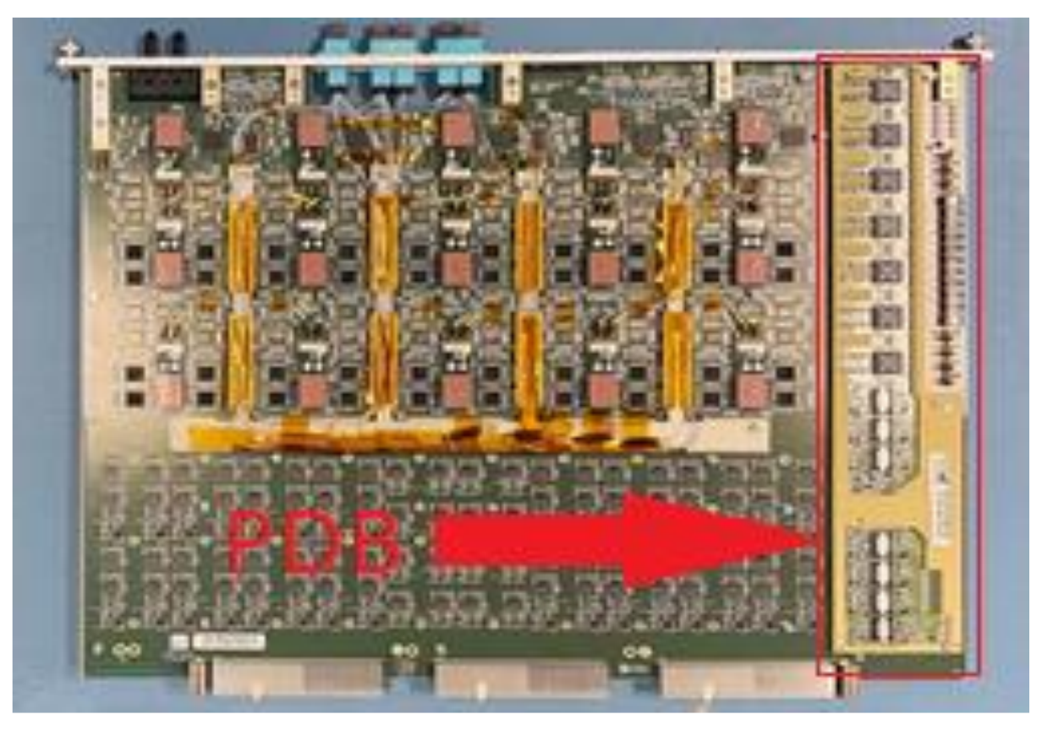

Fig. 5. Picture of the PDB mounted on the LTDB. The PDB is located on the right side of the picture

QUALITY ASSURANCE, CONTROL, AND TEST SETUP

The LTDB quality assurance and control (QA/QC) involves the testing of three main components: the cooling interface is tested for leaks, the PDB are tested to meet the requirements on voltage and current of the outputs, and each LTDB with a qualified PDB installed is subjected to functionality testing and - integrated with the test stand - to performance testing as detailed below. Each PDB module is tested with a standalone test stand to verify basic functionality before it is cleared to be installed on an LTDB motherboard. The input and output voltages and current are measured to obtain efficiency information. All test data and analysis results are examined and logged into a database. A PDB module is accepted if it passes the following requirements: the output voltage is within ±2.5 % of the nominal value; the output voltage ripple is within 10 mV peak-to-peak; and the efficiency is better than 70 % at nominal load. All PDBs were tested in university of Milano by an automated method before being shipped for further testing steps. All the PDBs have label with an unique code. In this way any action on the PDBs can be catalogued and we can check the action done on any PDB. The tests focused, primarily, on verifying that all controller outputs met specifications. The setup for these tests essentially consists of a board for testing a single PDB, which is powered by the power supplies described in the previous section. Each output of the PDB is connected to a resistive load that simulates the actual load after installation in the experiment. Through an additional electronic circuit and an Arduino, all output voltages are controlled both at no-load and load in a sequential way.

EXPERIMENTAL TEST

An example of the data acquired on a PDB by automatic procedure is shown in **Tab 1**. In the first column of the **Tab 1** are show the name of the outputs, in the second the output voltage without load, and the third the output voltage with load. The last 4 LHCs present an output at about 5 V. To test the output of these regulators, it was necessary to insert an auxiliary circuit, a voltage divider, to decrease the output voltage so that it could be read with the Arduino.

This device has a limit on the input voltage on the analog channels equal to the supply voltage of the Arduino board. Since the voltage of the last 4 LHCs is close to this value we could have some reading errors and therefore it was decided to adopt the voltage divider solution. All boards mounted within the experiment were tested with this setup and checked, one by one, to see if the voltage requirements of the outputs were met. Table1 shows an example of a PDB tested with this system and shows the output voltage values of individual components with and without resistive load. Each value was measured by taking the average of 100 values. Noise tests were also added. A sample of boards were chosen to test the RMS noise of DCDCs and regulators. **Fig. 6** shows a histogram that compares the RMS distribution for the 2.5 V obtained from the LTM4913s (output U2, U4, U5) and LTM 4619s (output U8, U9, U10). The signal output from the LHCs appears to be less noisy than that output from the LTMs. The measurement were done with a true RMS voltmeter (Rohde & Schwarz URE3 30MHz RMS/Peak Voltmeter) with 2 MHz bandwidth and includes the data of 9 PDBs. The other outputs of the LTMs and LHCs were also tested and found to heve noise compatible with those shown in **Fig. 6**. Other tests were done to verify the noise spectrum of LTMs and LHCs. **Fig. 7** shows the noise spectrum of an LTM that outputs 2.5 V. One can see the peak of the first harmonic around 775 kHz with an amplitude of 49.88 dB*m*V. This frequency corresponds to the switching frequency of the DCDC. **Fig. 8** show the noise spectrum of an LHC with 2.5 V outputs. The amplitude of the 775 kHz peek is reduced to 35.98 dB*m*V. These noise tests were not conducted as necessary for quality assurance purposes, but for further control about the quality of the components mounted on the boards. These tests were not performed on all components on the boards but on a sample. For example, in **Fig. 6** the obtained experimental results on 27 LHCs and 54 LTMs depicted.

PCB number: 002-007 04-20 **Board number: 20ALMILPD00113**		
Output	No load	Load
LTM1-1V5A	1.514 V	1.508 V
LTM1-3V3	3.354 V	3.348 V
LTM2-2V5A1	2.549 V	2.545 V
LTM2-2V5A2	2.544 V	2.539 V
LTM3-1V5B	1.515 V	1.507 V
LTM3-3V3B	3.352 V	3.348 V
LTM4-2V5B1	2.545 V	2.545 V
LTM4-2V5B2	2.550 V	2.531 V
LTM5-2V5B3	2.549 V	2.539 V
LTM5-2V5B4	2.541 V	2.535 V
LTM6-1V2ADCA	1.219 V	1.218 V
LTM7-1V2ADCB	1.250 V	1.245 V
LHC1-2V5ADCA	2.578 V	2.528 V
LHC2-2V5ADCB1	2.574 V	2.550 V
LHC3-2V5ADCB2	2.524 V	2.519 V
LHC4-5VA1	2.514 V	2.520 V
LHC5-5VA2	2.534 V	2.534 V
LHC6-5VA3	2.551 V	2.554 V
LHC7-5VAN	2.353 V	2.352 V

Tab. 1. Example of a data taking on a PDB of each output both with and without load

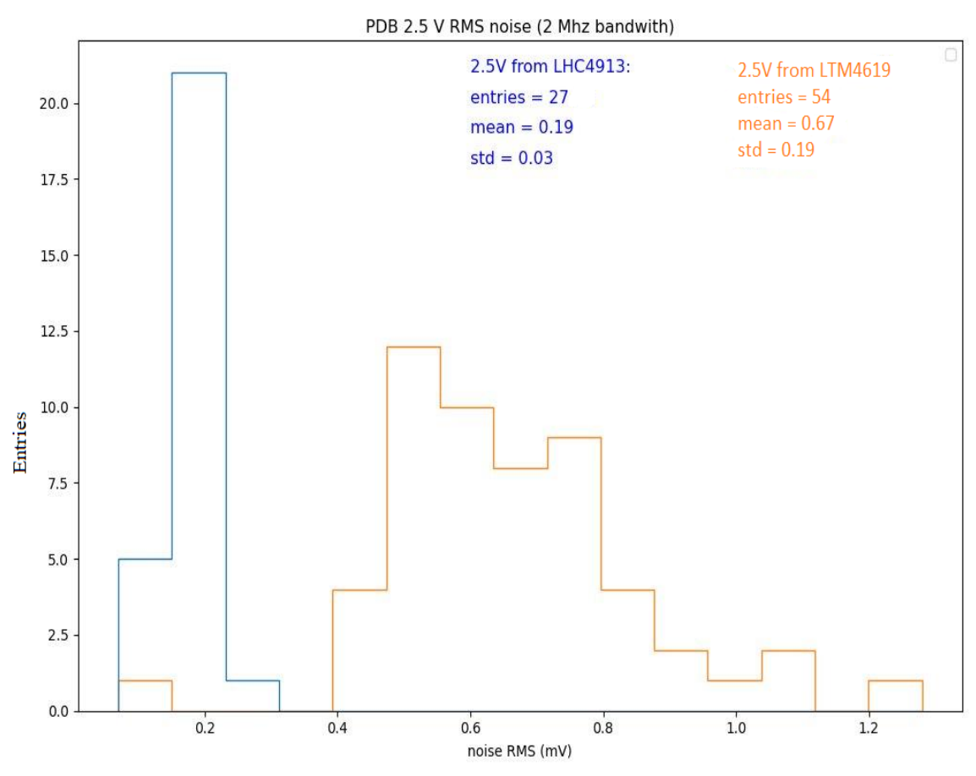

Fig. 6. Histogram of noise RMS of LTMs and LHCs 2.5 V outputs

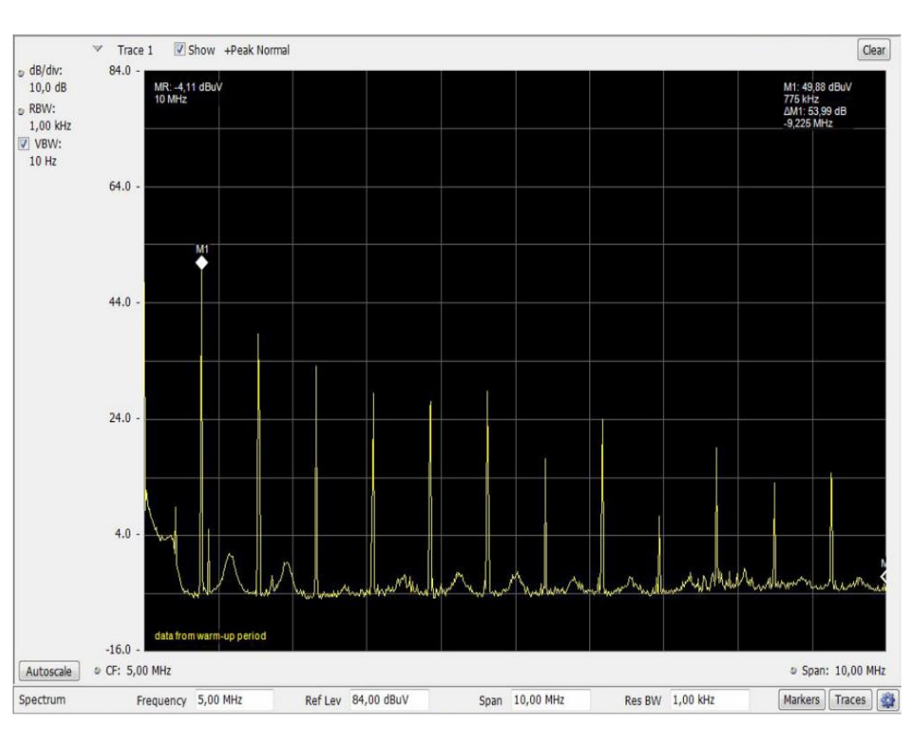

Fig. 7. Noise spectrum of LTM4913 with 2.5 output voltage

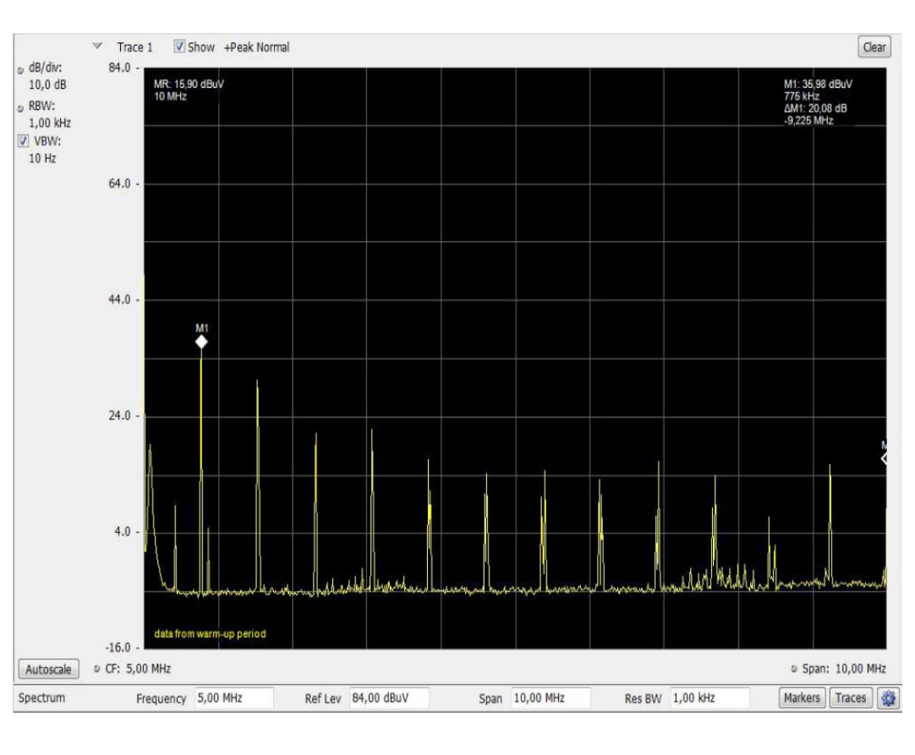

Fig. 8. Noise spectrum of LHC4619 with 2.5 output voltage

CONCLUSIONS

This poster gives a brief overview of the tests performed for the production of the power distribution mezzanine of the new trigger board of the ATLAS liquid argon calorimeter. The board, the test setup and the list of tests performed are presented. Results of the noise performance of the board are also presented. All the needed boards have been produced, installed on the trigger board, and successfully commissioned.