LAr in Phase 2

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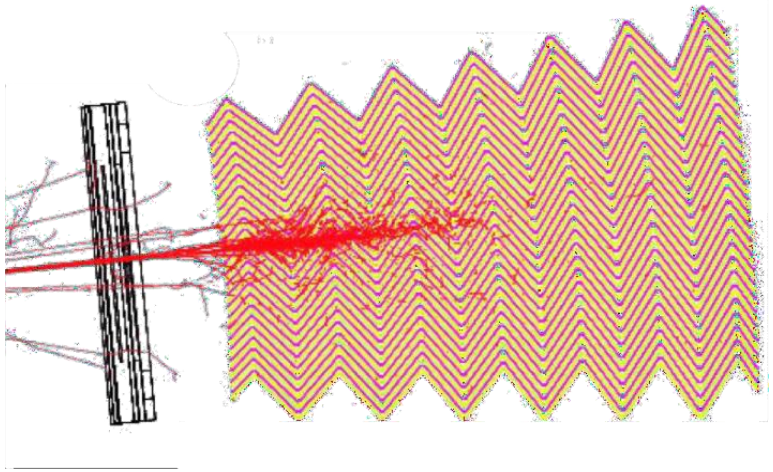
XVI workshop ATLAS Italia
19th September 2023

Outline

- Phase 2 Upgrade status
  - LAr electronics upgrade
  - New power supply system
  - New power distribution system
  - Status of the activities

The Liquid-Argon Calorimeters

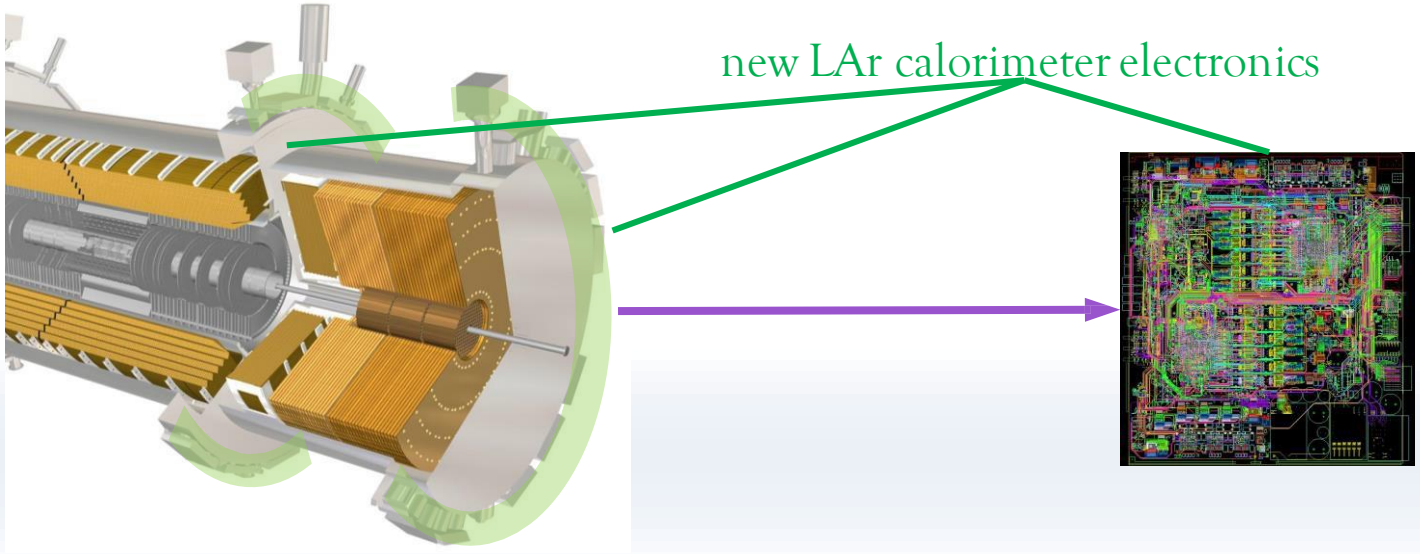


- The liquid-argon (LAr) calorimeters measures the energy of electrons, photons and hadronic particles in each of the 182.000 calorimeter cells
- New calorimeter electronics is needed to cope with improved ATLAS trigger system:

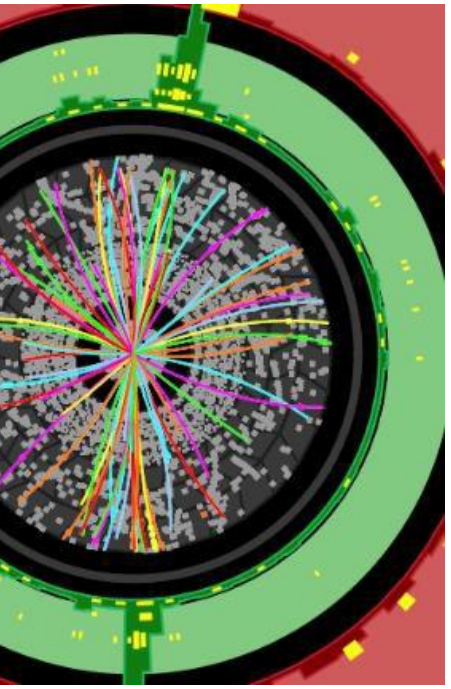
  trigger rate 100 kHz (today) → 1 MHz (HL-LHC)

  trigger latency 2.5 μs (today) → 10 μs (HL-LHC)

- Front-End electronics must be radiation tolerant for 10 years of HL-LHC operation and L_{int} = 3000 fb^{-1}
- The LAr calorimeters are intrinsically radiation tolerant and do not need to be replaced for HL-LHC operation



New Readout Electronics for the LAr Calorimeters

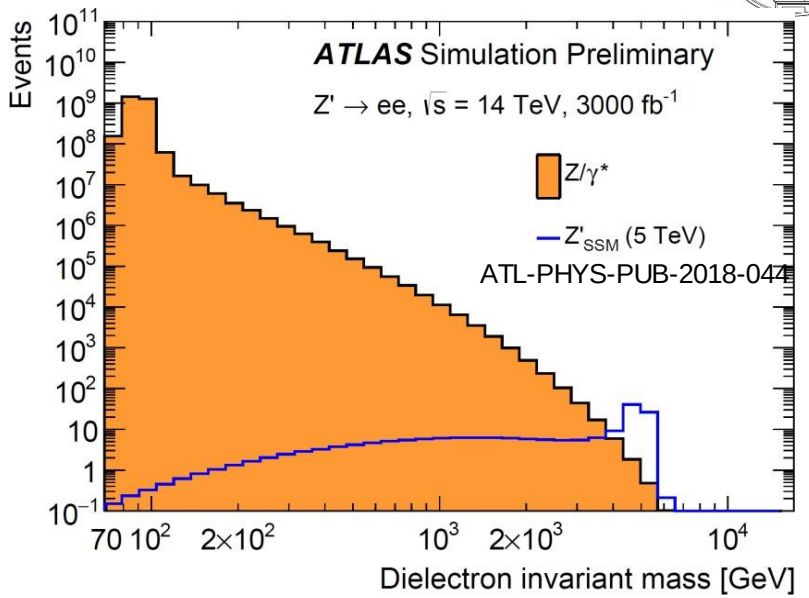


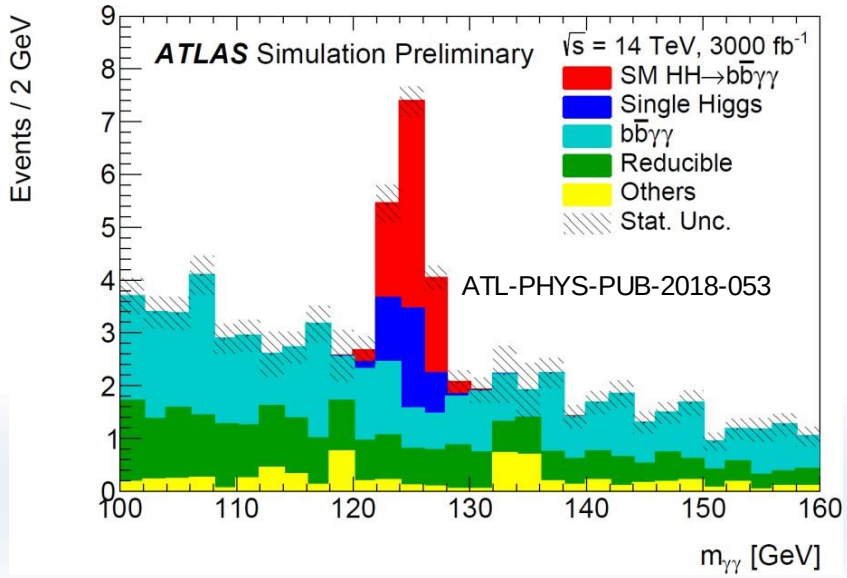
Run 427394 Event 3038977

- 16 bit dynamic range of cell energies from 50 MeV to 2-3 TeV

- Electronic noise must stay below intrinsic calorimeter resolution
- Very low noise preamplifier with 2 amplification gains:
  - Electrons with $E_T = m_Z/2$ and photons with $E_T = m_H/2$ are in same high-gain range to reduce energy calibration systematics

- Non-linearity below 0.1% up to energies of 300 GeV



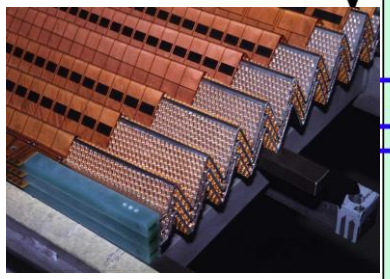


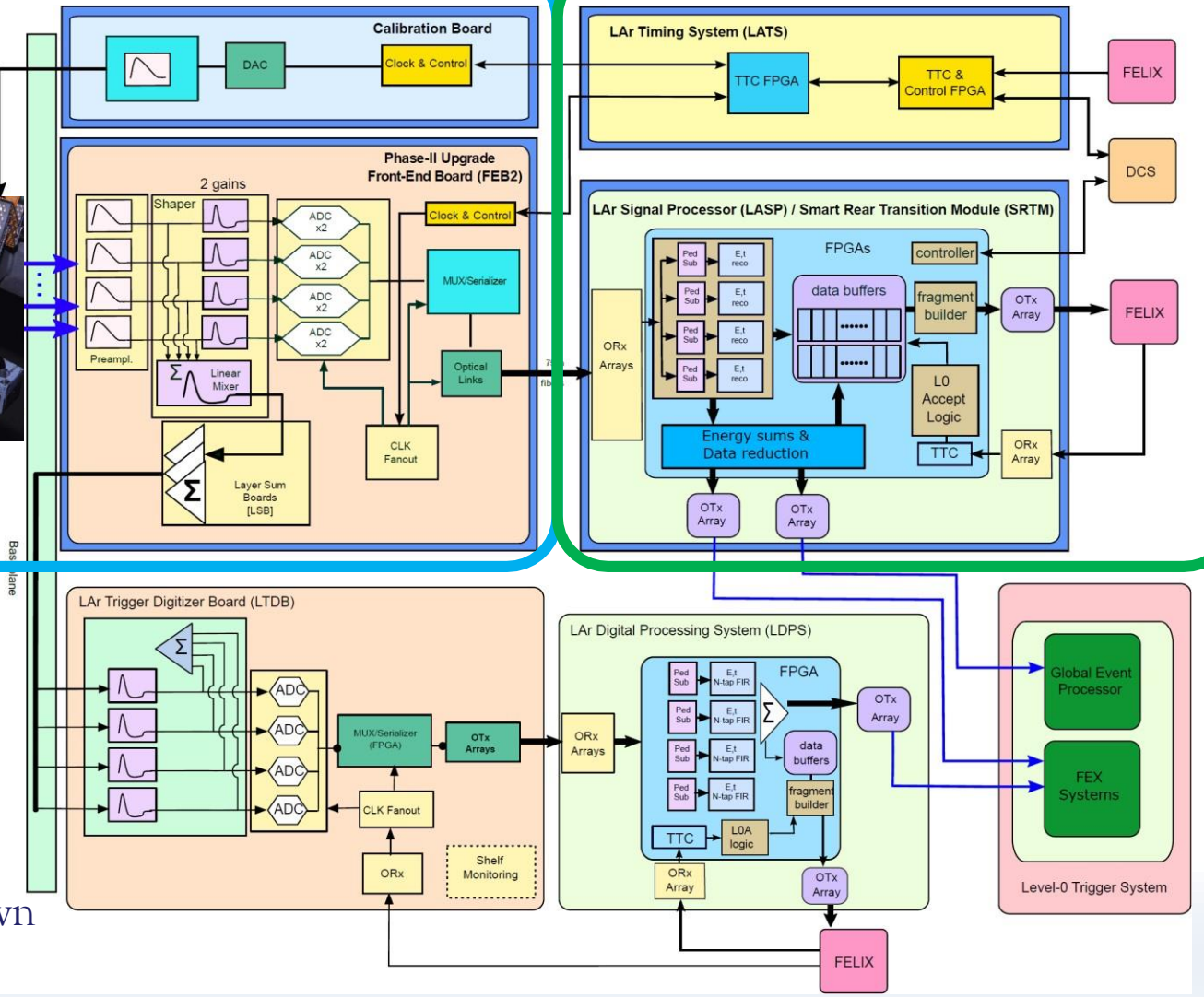
- Analog-to-digital conversion in every cell by two 14-bit ADCs with overlapping energy range to measure noise level and capture highest energy physics signals

Components of the Future LAr Calorimeter Readout

on-detector

off-detector





Digital Trigger readout already installed during LHC long- shutdown 2 (2019-2021)

- 1524 new front-end boards (FEB2) with pre-amplifier, shaper, ADC, layer sum-boards (LSB2) and digital data transmission
- 122 calibration boards for direct electronic signal injections
- Full-granularity, trigger-less readout with 36.000 optical fibers at 10.24 Gb/s each
- 278 LAr Signal Processors (LASP) with 2 FPGAs each
- LAr timing system (LATS) for trigger/time/control (TTC)

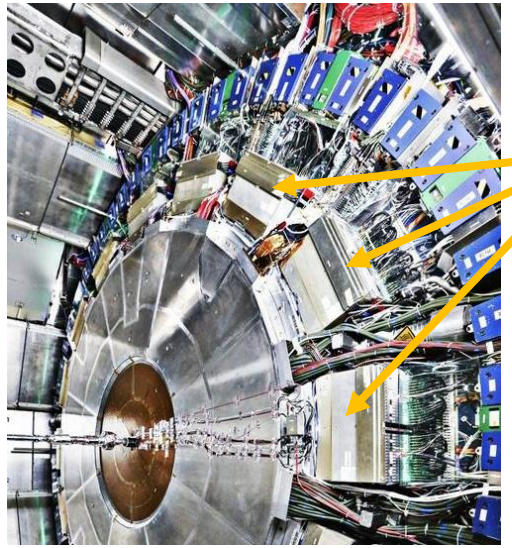
New ATLAS global and forward trigger systems will receive full-granularity calorimeter data at 40 MHz

Front-end Board (FEB2)

- Each front-end board covers up to 128 calorimeter cells

- Performance requirements:
  - coherent noise <5% of the total noise in each channel
  - electronics contribution to the crosstalk < 1%
  - clock distribution with <5 ps jitter for stable ADC operation
  - power consumption <1 W per channel

- First full prototype version in production:



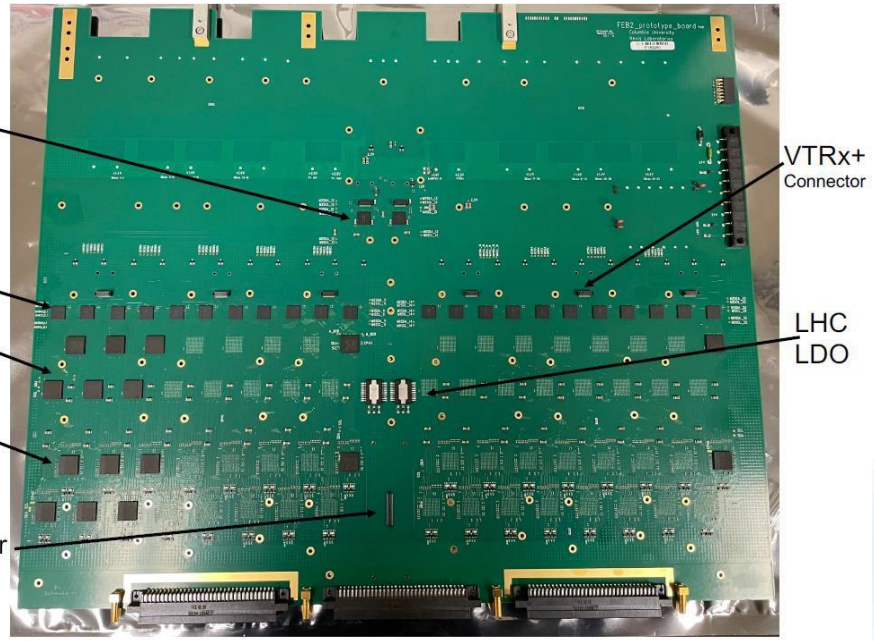
control & clock

digital data transmission

ADC

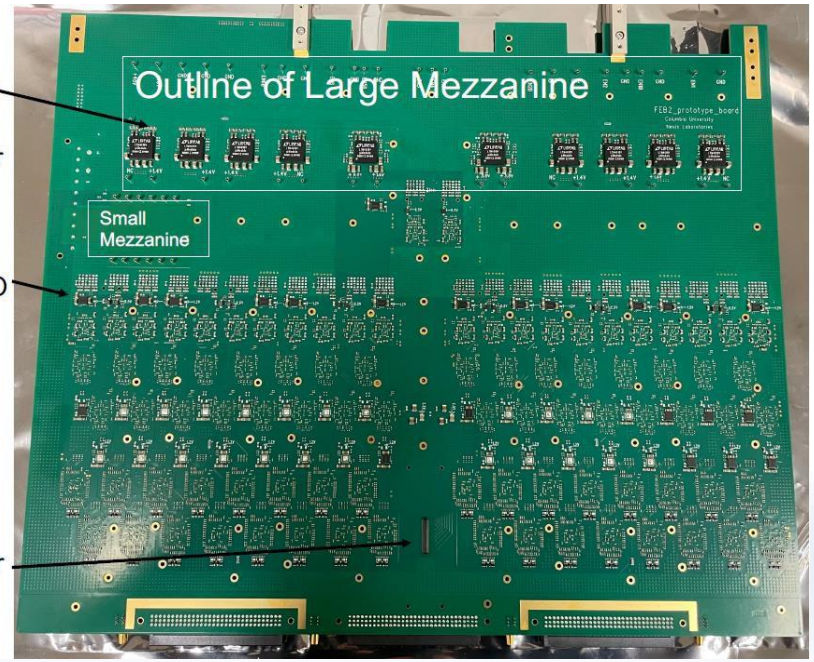
pre-amp/shaper

analog layer sums



power conversion

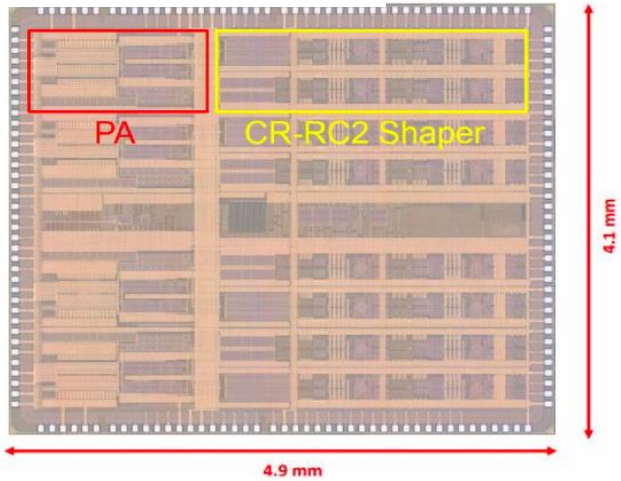
voltage regulators



FEB2 ASICs: Preamp/Shaper & ADC

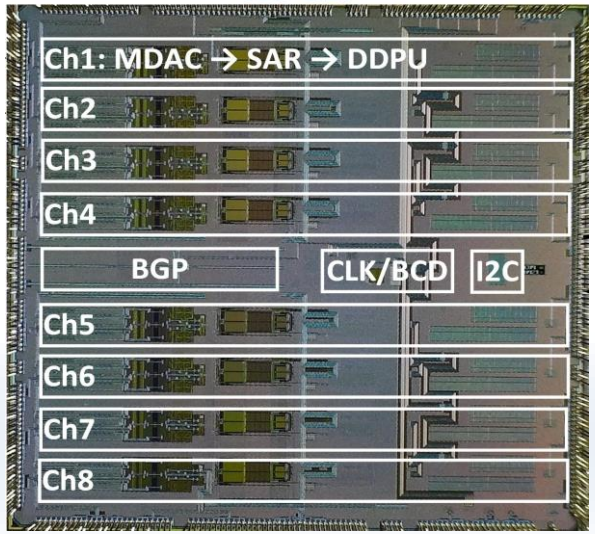
- **ALFE2: prototype custom ASIC in 130nm CMOS TSMC technology with 4 channels per ASIC (~80k total)**
- Analog processing on signals (amplification, splitting into 2 gain scales, bipolar CR-$(RC)^2$ shaping function) for differential outputs to ADC + L0 trigger
- Extensive test campaign shows ALFE-2 meets the specification
- Engineering production run is completed
- Radiation test is ongoing
- Series testing in preparation

ALFE2



- **COLUTAv4: custom ASIC in 65nm CMOS technology (~80k total)**
  - 8-channels of Multiplying DAC (3 bits) followed by 12-bit Successive Approximation Register (SAR) DAC
  - Digital Data Processing Unit (DDPU) applies calibration bit weights and serially transmits data
  - 1.2 ADC counts of noise on pedestal
  - Tests of different chips: all > 11 ENOB
  - Pre-production of COLUTA ADC is completed
  - Preparation of mass production and automated series testing

COLUTAv4$_{VDD=1.2V}$



Upgrade Phase 2 - LVPS

All the LVPS will be moved in a more accessible area.

The output power will be 48 V for alle the LVPS

Milano is responsible for the new front-end board power supply system.

Deliverables for which Milano is responsible:

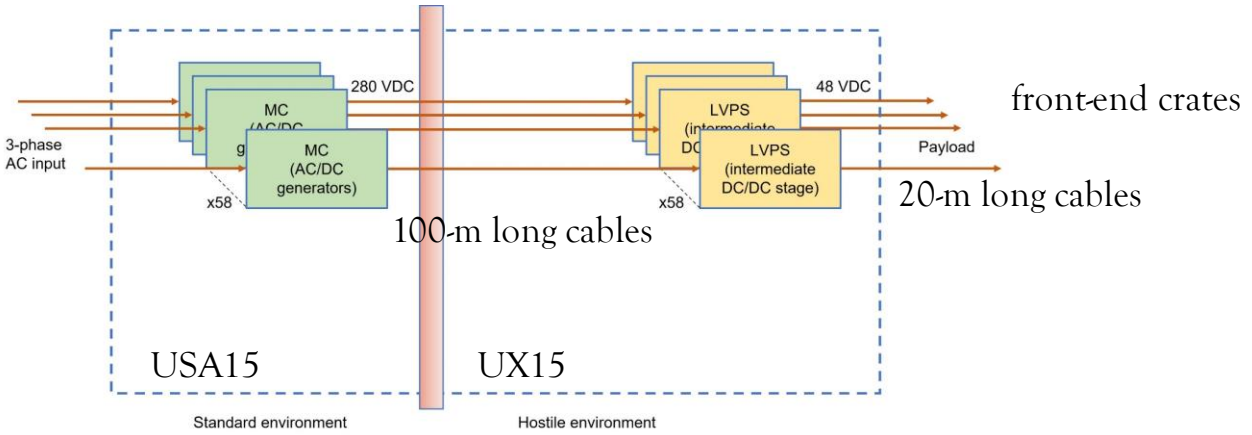
- 58 new power supplies
- 124 power supply mezzanines (PDB2) of the Phase I trigger board (LTDB) that replace the mezzanines (PDB) we already developed for Run 3

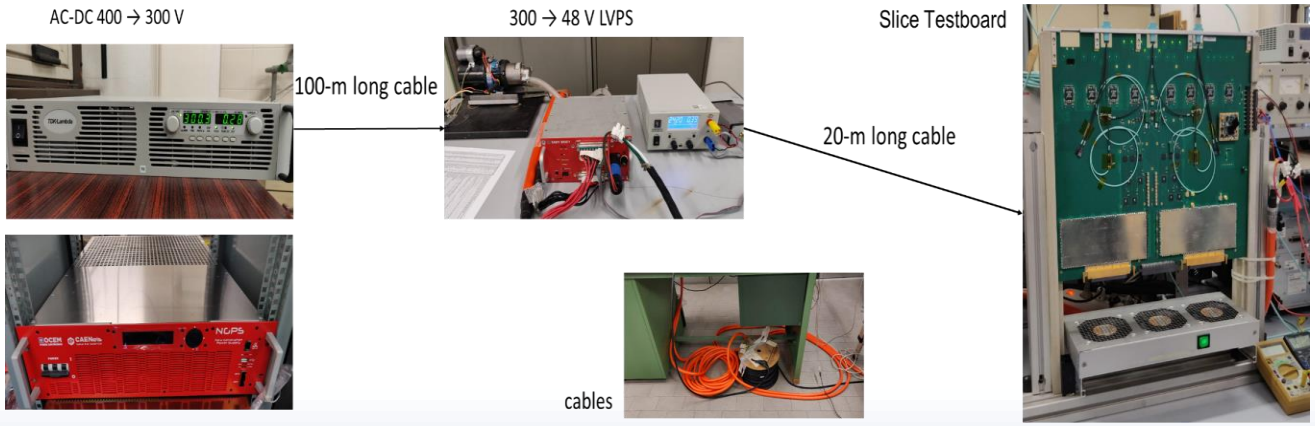
Lab testing over the past year with a similar set-up as ATLAS and a prototype to define the specifications for the new power supplies

The new PS designed and produced commercially to our specifications

- 250-400V input, 48 V output, power output 5.4 kW
- Magnetic field 0.6 T, radiation resistance (3.3 krad, 5.2x10^11 n/cm2)

Document writing for tender (via CERN) in advanced stage for submission for October to Procurement Office





Test set-up a Milano

Upgrade Phase 2 – Large mezzanine

In parallel big work to develop a solution to enable conversion on the front-end board (FEB2) from 48 V to the supply voltages of the electronics (1.2 V, 2.5 V)

Design and testing of various DC/DC converter solutions, implemented as mezzanines that can be tested on preprototypes/prototypes of the front-end board

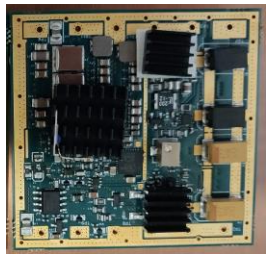
Various solutions was developed in the end the following solution was chosen:

- Rad hard solution based on components developed at CERN (GaN_Controller and bPOL12V) + commercial GaN EPC2152 (bPOL48V)

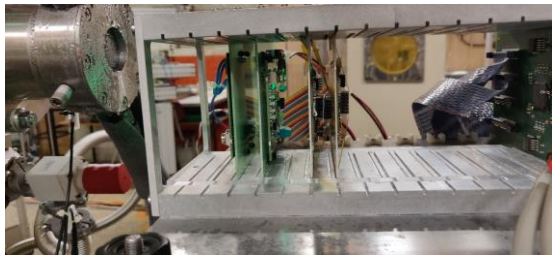
This solution is the baseline and we designed and produced a prototype

This board is under test in Milano this days, first results are god, features test : noise and magnetic field

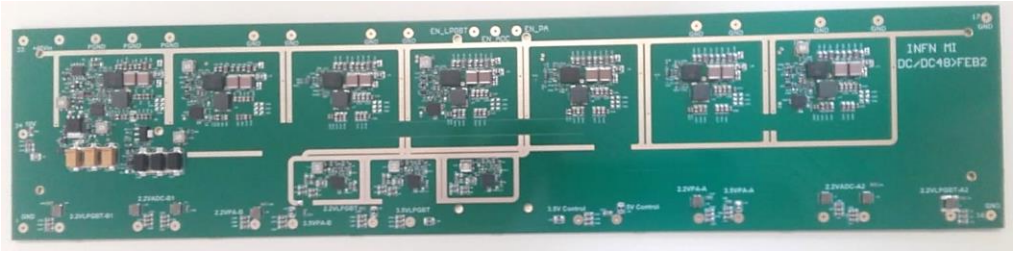
If board tests are positive, this solution will be integrated on prototype 2 front-end board



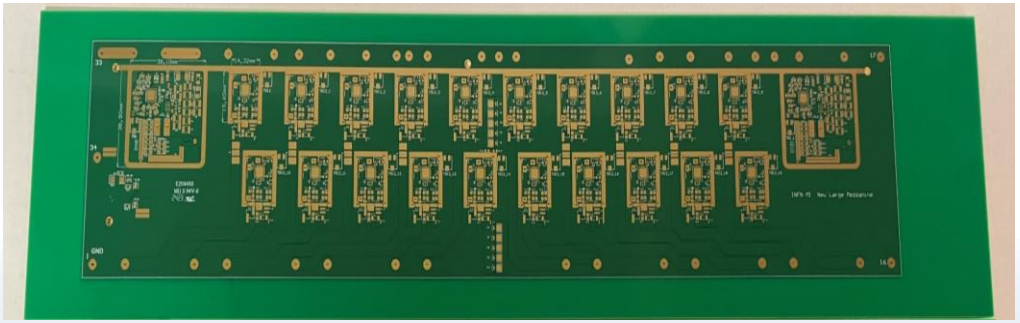
small mezzanine



Test with neutrons of the small mezzanine



large mezzanine 1 (OLD)



large mezzanine 2 (NEW)

Upgrade Phase 2 – PDB2

In parallel we are also developing the power mezzanine (PDB2) to replace the similar board (PDB1) mounted on current trigger boards

Reasons for replacement:

- Different supply voltages: 6 , 7 V → 48 V
- Radiation resistance

Same size, same pin out, same output voltages but powered at 48 V

Will use a solution similar to that developed for the front-end board

- Based on bPOL12V and bPOL48V

Design is on going and the first version will be ready by the end of the year

Given all the electronics upgrade, an integration test is planned at BNL in the fall of 2024

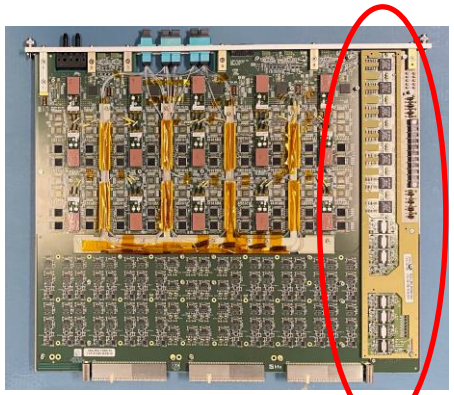
Set-up accurately reproducing the electrical and mechanical part of the calorimeter readout: cables, LVPS, crate with baseplane, cooling system. Already used at the time of calorimeter construction and constantly updated

Will now be upgraded with a full crate with FEB2 prototypes, trigger board, calibration board

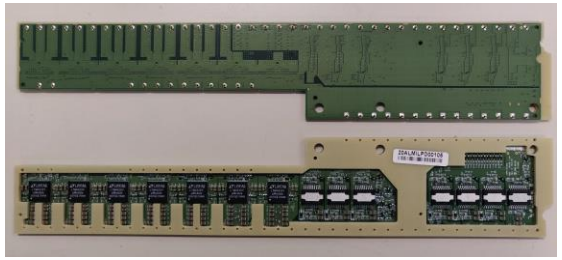
New complete supply chain (like the one we now have in Milan)

New off-detector electronics for readout

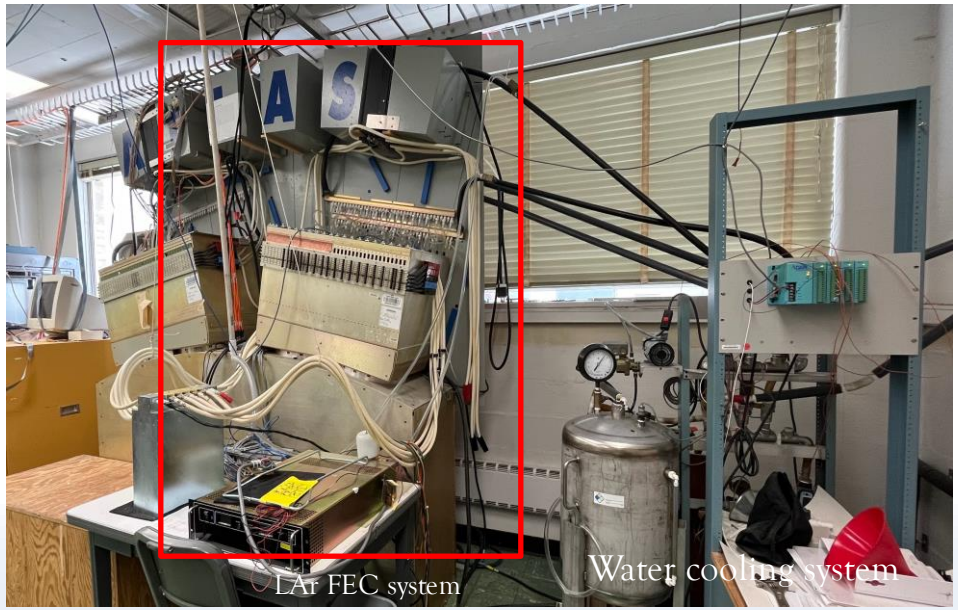
Will make noise, calibration, gain measurements, linearity, cross-talk measurements on the boards, in as close a configuration as possible to that of Phase 2



PDB mounted on the trigger board



PDB



Set-up in BNL

Conclusions

- The ATLAS LAr calorimeters readout electronics will be replaced by a more radiation-tolerant system, which supports trigger rates of 1 MHz and longer trigger latencies
- All components are in advanced prototype stage or about to start series production
- All ASICs and readout boards are expected to be ready for installation in 2026
- The tender of the LVPS will be submitted in October to procurement office
- The test for the large mezzanine will continue in Milano with noise and magnetic test
- A first design of the PDB2 will be ready by the end of the year

Istituto Nazionale di Fisica Nucleare

Thanks for the attention