Novel qutrit circuit design for multiplexer, De-multiplexer, and decoder

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Abstract
Designing conventional circuits present many challenges, including minimizing internal power dissipation. An approach to overcoming this problem is utilizing quantum technology, which has attracted significant attention as an alternative to Nanoscale CMOS technology. The reduction of energy dissipation makes quantum circuits an up-and-coming emerging technology. Ternary logic can potentially diminish the quantum circuit width, which is currently a limitation in quantum technologies. Using qutrit instead of qubit could play an essential role in the future of quantum computing. First, we propose two approaches for quantum ternary decoder circuit in this context. Then, we propose a quantum ternary multiplexer and quantum ternary demultiplexer to exploit the constructed quantum ternary decoder circuit. Techniques to achieve lower quantum cost are of importance. We considered two types of circuits, one in which the output states are always restored to the initial input states and the other in which the states of the output are irrelevant. We compare the proposed quantum ternary circuits with their existing counterparts and present the improvements. It is possible to realize the proposed designs using macro-level ternary gates that are based on the ion-trap realizable ternary 2-qutrit Muthukrishnan–Stroud and 1-qutrit permutation gates.

Keywords Quantum computing · Qutrit · Quantum ternary logic · Restoration technique · Non-restoration technique

1 Introduction

According to Moore's law, computer processing power has steadily increased in the last few decades owing to the escalating transistor density on chips. To reduce the width and

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increase the number of transistors, the problem of electron interaction and the creation of unwanted capacitors should be considered [1, 2]. It will eventually be impossible to keep downsizing the current technology forever since this will eventually reach the fundamental physical limits of atomic structures. Rolf Landauer demonstrated that losing every bit of information in irreversible conventional circuits leads to an internal power dissipation of at least *kTln2* Joules, where *T* is the absolute temperature of the environment and *k* is the Boltzmann constant [3]. Scientists have sought alternatives to CMOS technology due to a growing demand for lower power consumption and higher processing power [4].

It is believed that quantum computing has a great deal of potential to parallelize information processing. In quantum computing, quantum mechanical systems are used to process quantum information. Various quantum technologies have been introduced in the literature: ion trap systems in which information is represented as the energy levels of individual ions; optical quantum systems, which represent information using different polarizations of photons; silicon NMR systems where information stored in the spin of the nucleus of an atom or superconductor [5–10].

The quantum computer is a promising candidate for the next generation of computers, which are more powerful than classical ones. They are believed to solve intractable problems that the current classical computers cannot solve. Since quantum computing is inherently reversible and information is not lost in reversible computations, the use of quantum gates prevents power dissipation [11, 12]. Quantum gates implement permutation functions and have the same number of outputs and inputs [13–16]. Fan-out and feedback from output to input are prohibited when designing quantum reversible circuits [17]. The research on quantum computers is moving towards avoiding energy loss and designing computers with high speed [11].

Qudit circuits and more specifically qutrit ones in quantum technology are recently investigated by researchers due to their advantages over their binary counterparts, including logarithmic reductions in the number of qudits [10, 50–52]. For a Hilbert space of *N* dimensions, in a quantum binary system, the required number of qubits is equal to [18–20]:

$$n_2 = \log_2 N \tag{1}$$

However, in a quantum 3-valued system, the required number of qudits is:

$$n_3 = \log_3 N \tag{2}$$

$$n_3 = \log_3 N = \frac{\log_2 N}{\log_2 3} = \frac{n_2}{\log_2 3} = \left(\frac{1}{\log_2 3}\right)n_2 = \frac{1}{1.585}n_2 = 0.63n_2 \tag{3}$$

As can be seen in Eq. (3), a *3*-valued quantum system requires 0.63 times the memory of the respective binary quantum system. Therefore, logarithmic reduction in the number of qudits can be considered the main advantage of a 3-valued quantum system over a binary quantum system [18–20].

From the points discussed above, it can be concluded that in quantum ternary systems, 0.37 times fewer qutrits are required than the required qubits in the quantum

binary systems [18–20]. In this work, we will focus on qutrit systems. Compared to qubit systems, qutrit systems simplify the decomposition and reduce resources, requiring fewer qubits and less memory. Investigating qutrit systems are essential since we have access to a limited number of qudits. However, the preparation, control, accessibility, fault tolerance, runtime, reliability, noise, and error rate issues, which are difficult to surmount, also need to be investigated. Since using qutrit systems, a smaller amount of energy separates states beyond zero and one; hence noise and control issues become challenging. An inverse engineering method is proposed in [58] for the dynamical control of three-level open systems by considering energy relaxation and dephasing. This paper shows that by using a superconducting qutrit platform, the error rate of the controls is significantly reduced. Authors in [51] discussed constructing any qutrit multiple-controlled Clifford + T unitary using just Clifford + T gates and without using any ancilla lines. They proposed ancilla-free Clifford + T implementations of multiple-controlled T gates as well as all versions of qutrit multiple-controlled Toffoli gate, while the analogous results for qubits are impossible [51]. An implementation of ternary classical reversible functions on n-trits as an ancilla-free qutrit unitary is also provided in [51]. Quantum systems are highly sensitive to errors, and it is even possible for a state to be changed when interacting with the environment [57, 62]. In [62], an error-correcting code is proposed which can correct a single error in a qutrit. Fault tolerance in quantum circuits can be determined by the entangling gate and the interaction network topology [59]. It is important to optimize the number of quantum units as well as the depth of a quantum circuit in order to minimize the effect of noise in the output. The authors in [61] discussed the advantages of using qutrit systems instead of qubit systems in scalar quantum electrodynamics. In [60], qutrit systems were shown to outperform qubits in terms of reliability and runtime.

Any combinational logic circuit can be implemented in a binary system using multiplexers and basic logic gates, which is also true for ternary logic [53]. Many quantum ternary circuits implementation for different types of computational units of quantum systems, including full adder, half adder, parallel adder/subtractor, subtractor, multiplier, decoder, encoder, demultiplexer, and multiplexer, can be found in the literature [20–31, 57]. Decoder, multiplexer, and demultiplexer circuits are major sub-circuits needed for constructing ternary quantum oracles and ternary system designs such as communication systems, computer memory, and arithmetic logic unit [54]. In [31], a quantum ternary decoder with a quantum cost of 57 is presented.

Moreover, quantum ternary multiplexer and demultiplexer are introduced in [30], with a quantum cost of 102. This paper focuses on synthesizing more efficient quantum ternary decoders, multiplexers, and demultiplexers compared to existing designs in [30, 31]. Moreover, we present the characteristics of the proposed circuits with respect to quantum cost, depth, number of garbage outputs, and number of constant inputs. The synthesized circuits are usually evaluated by minimizing these important parameters, which leads to better efficiency of the quantum ternary logic design [32–34]. In the literature, these parameters are defined as follows:

- **_Total quantum cost_** is the number of 1-qutrit permutation gates required to realize the quantum ternary circuit.

- *Depth* is the number of timesteps required to realize the corresponding quantum circuit [49]. One or more quantum ternary gates that act on disjoint qutrit can be executed in each timestep in parallel.
- *The number of constant inputs* is the number of inputs to be kept constant at *0, 1*, or *2* in order to synthesize a logic function.
- *The number of Garbage outputs* is the number of unused outputs to maintain the reversibility of the logic functions.

The paper is organized as follows: Sect. 2 presents ternary logic and ternary Galois Field, and quantum ternary gates, which are used in the following sections to design our proposed circuits. Section 3 presents the realization of our proposed quantum reversible ternary decoder, multiplexer, and demultiplexer circuits. In Sect. 4, the assessment of the proposed circuits is discussed, and finally, the conclusion is given in Sect. 5.

2 Preliminaries

The basic concepts of quantum ternary logic are presented in this section. We will also introduce ternary Galois Field 3 (GF3) and corresponding multiplication and addition operations in GF3. Moreover, this section includes quantum ternary permutation, Muthukrishnan-Stroud, and Controlled Feynman gates, which were used to construct our proposed designs in the next sections.

2.1 Quantum ternary logic and qutrit

In quantum multiple-valued logic, quantum ternary logic is the most popular type. In comparison with binary logic, quantum ternary logic offers several advantages, including higher security [35, 36], stronger quantum information processing [37], higher density of stored information, reduced interconnection complexity and area [38], lower power consumption and improved fault tolerance [39]. Ternary quantum computation achieves higher error tolerance when compared to binary quantum computation [55]. In a quantum ternary system, the unit of information is called qutrit (quantum ternary digit). There are three basic states for a qutrit, namely $|0\rangle$, $|1\rangle$, and $|2\rangle$. These basic states are called qutrit states and can be represented by 3×1 vectors [25_ENREF_11]:

$$|0\rangle = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \quad |1\rangle = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \quad |2\rangle = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \quad (5)$$

Qutrits can be represented by linear superpositions of basis states in a quantum ternary system. Superposition is the term for this technique, which can be defined with the following equation:

$$\psi = \alpha|0\rangle + \beta|1\rangle + \gamma|2\rangle \quad (6)$$

where ψ is the wave function and α, β, and γ are complex numbers. The quantum ternary system may be in each basis state with a specified probability. The probability measurement of the occurrences for state $|0\rangle$ is equal to $|\alpha|^2$, for state $|1\rangle$ is $|\beta|^2$, and for state $|2\rangle$ is equal to $|\gamma|^2$. The sum of these probabilities is shown in the following:

$$|\alpha|^2 + |\beta|^2 + |\gamma|^2 = 1 \tag{7}$$

2.2 Ternary galois field

In this section, an introduction to the ternary Galois Field 3 (GF3) is provided. The GF3 algebraic structure is composed of three elements $T = \{0, 1, 2\}$ and two primitive binary operations that are module 3. Table 1 and Table 2 show the operations of addition ($\oplus$) and multiplication ($\odot$), respectively [26, 40].

GF3 operations satisfy the following axioms. As can be seen, operations in GF3 are associative and commutative. Moreover, multiplication is distributive over addition.

Axiom 1: $a \oplus (b \oplus c) = (a \oplus b) \oplus c$ (Associative law for addition).

Axiom 2: $a \oplus b = b \oplus a$ (Commutative law for addition).

Axiom 3: $a \oplus 0 = a$ (Identity element for addition).

Axiom 4: $a \oplus (-a) = 0$ (Inverse element for addition).

Axiom 5: $a \odot (b \odot c) = (a \odot b) \odot c$ (Associative law for multiplication).

Axiom 6: $a \odot b = b \odot a$ (Commutative law for multiplication).

Axiom 7: $a \odot 1 = a$ (Identity element for multiplication).

Axiom 8: $a \odot a^{-1} = 1$ (Inverse element for multiplication).

Axiom 9: $a \odot (b \oplus c) = (a \odot b) \oplus (a \odot c)$ (Distributive law).

Table 1 The truth table of GF 3 addition operation [26, 29]	$\oplus$	0	1	2
	0	0	1	2
	1	1	2	0
	2	2	0	1

Table 2 The truth table of GF 3 multiplication operation [26, 29]	$\odot$	0	1	2
	0	0	0	0
	1	0	1	2
	2	0	2	1

2.3 Ternary permutation gates

In ternary logic, there are *3! = 6* possible permutations of *0, 1*, and *2*. Accordingly, a ternary logic variable can be transformed in 6 ways using unitary transformations. The truth tables for these transforms can be seen in Table 3.

According to Table 3, the value of the variable *a* changes from *x* to *y* and *y* to *x* without changing the other values if transforms of the form *Z (xy)* (where *x, y* ∈ {0, 1, 2}) and *x ≠ y*, are applied on a variable *a*. The value of the variable *a* will become *a* ⊕ *x* when the transforms of the form *Z (+ x)* (where *x* ∈ {0, 1, 2}) are applied on a variable *a*.

All transforms can also be represented by *3 × 3* matrixes. Any of these matrixes can be presented by a 1-qutrit permutation gate [30, 41]. Figure 1 illustrates 1-qutrit permutative transforms.

In the *Z (+ 0)* transformation, each column shows *0, 1*, and *2*, respectively, and it is known as an elementary state. In *Z (+ 1)* transformation, the qutrit states are *Z (+ 0)* shifted by 1, in *Z (+ 2)* transformation, the qutrits in elementary state shift by 2; with *Z (12)* transformation, the qutrit states |1⟩ and |2⟩ in *Z (+ 0)* will be exchanged, *Z (01)* exchanges qutrit states |0⟩ and |1⟩ in the elementary state, and with *Z (02)* qutrit states |0⟩ and |2⟩ will be exchanged. These transformations can be presented as 1-qutrit permutation gates. In the literature, each of these gates has various names [41–44, 56], *Z(+ 0)* is called buffer and represents a quantum wire; *Z(+ 2)* is named C2 and dual-shift; *Z(+ 1)* is called C1 and single-shift; *Z(12)* is termed D and self-shift; *Z(01)* called E and self-single-shift, and *Z(02)* is called N inverse and self-dual-shift. Figure 2 shows the symbolic representation of 1-qutrit permutation gates. In this gate,

Table 3 Ternary permutative unitary transforms [18]

Transform	Z(+ 0)	Z(+ 1)	Z(+ 2)	Z(12)	Z(01)	Z(02)
Input 012	012	120	201	021	102	210

$$Z\ (+0) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad Z\ (+1) = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \quad Z\ (+2) = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$$

$$Z\ (12) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \quad Z\ (01) = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad Z\ (02) = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$$

Fig. 1 1-qutrit permutative transforms [26, 30]
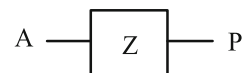
Fig. 2 Symbol of 1-qutrit permutation gates [25]

A —[Z]— P

Table 4 Ternary 1- qutrit gates and their inverse gates [18]

Gate	Z(+ 1)	Z(+ 2)	Z(12)	Z(01)	Z(02)
Inverse gate	Z(+ 2)	Z(+ 1)	Z(12)	Z(01)	Z(02)

the output P is equal to Z transform (where $Z = \{+ 0, + 1, + 2, 01, 02, 12\}$) of input A. The quantum cost of these gates is 1.

As an example, for 1-qutrit permutation gates, when the transform is $Z (+ 2)$ and the variable a is 1, we have:

$$Z\ (+2) = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \quad a = |1\rangle = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \tag{8}$$

Application of a transform Z on a variable a is computed as the matrix multiplication of $Z.a.$ The computation of $Z (+ 2).a$ is as follows:

$$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} . \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{9}$$

As can be seen in Table 3, when the input is 1, and the transform is $Z (+ 2)$, the result is 0. It is worth mentioning that each of the 1-qutrit permutation gates has a unitary inverse gate which is utilized in order to restore the inputs [45, 46]. Inverse gates for each 1-qutrit permutation gate are illustrated in Table 4. As shown in this table, $Z (01), Z (02),$ and $Z (12)$ are self-inverse gates.

2.4 Ternary muthukrishnan–stroud gates

Muthukrishnan and Stroud designed 2-qutrit quantum gates and demonstrated their ion-trap realizations [25]. Figure 3 shows the graphical symbol used for 2-qutrit Muthukrishnan-Stroud (M-S) gate. As shown, the inputs for this gate are A and B, and the outputs are P and Q where P equals A and Q equals Z transform (where $Z = \{+ 1, + 2, 01, 02, 12\}$) of B when $A = 2$, otherwise $Q = B$. This gate has a quantum cost of 1.

Fig. 3 Symbol of 2-qutrit Muthukrishnan-Stroud gate [25]
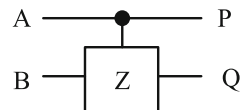
2.5 Ternary controlled feynman gate

Figure 4a shows the symbolic representation of the ternary Feynman gate. As shown, the inputs for this gate are *A* and *B*, and the outputs are *P* and *Q* where *P* equals *A* and *Q* equals $A \oplus B$. This gate can be realized using Muthukrishnan-Stroud gates and 1-qutrit permutation gates in Fig. 4b. According to the proofs stated in [47, 48] ternary Feynman gate evaluation matrix can be expressed as:

H.A Khan in [30] designed ternary Controlled Feynman gate and demonstrated their realization using 2-qutrit Muthukrishnan-Stroud gates. Figure 5a illustrates the symbolic representation of the ternary Controlled Feynman gate. As can be seen, the inputs for this gate are *A*, *B*, and *C*, and the outputs are *P*, *Q*, and *R*. *P* equals *A, Q*

Fig. 4 2-qutrit Feynman gates. **a** Symbol. **b** Realization using 2-qutrit M–S gates [30].

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}$$
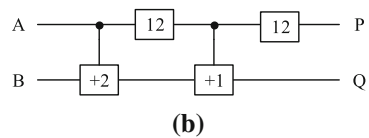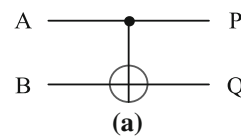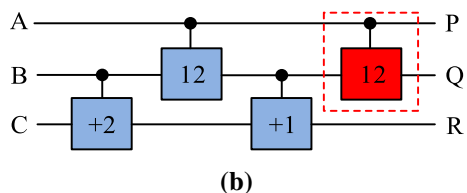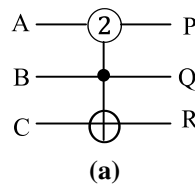

Fig. 5 3-qutrit Controlled Feynman gates. **a** Symbol. **b** Realization using 2-qutrit M–S gates [30].

equals B, and R equals $B \oplus C$ when $A = 2$; otherwise, $R = C$. This gate can be realized using Muthukrishnan-Stroud gates and 1-qutrit permutation gates in Fig. 5b. Resulting in a quantum cost of 4 for this gate. It is possible to remove the fourth 2-qutrit M-S gate in the red box if input B is not needed at the output Q. The quantum cost is reduced to 3 in this way.

3 The proposed quantum ternary circuits

In this section, we first propose two quantum ternary decoders. The quantum ternary multiplexer and demultiplexer circuits are then presented. The following subsections describe these designs in detail.

3.1 The proposed quantum ternary decoder circuits

One of the important ternary combinational logic circuits is the ternary decoder which converts ternary information from the N inputs to 3^N unique outputs. Figure 6 illustrates the block diagram of $N \times 3^N$ ternary decoder circuit. Table 5 shows the truth table of 2×9 ternary decoders with active-2 output. In this table, A and B are the input variables, whereas $D0$, $D1$, $D2$, $D3$, $D4$, $D5$, $D6$, $D7$, and $D8$ are the output variables. For each combination of inputs, only one output line will be activated. Here, the circuit is active-2, i.e. if the output line is 2, then the line is ON; otherwise, it is OFF.

According to the above true table, only one of the outputs will be 2 for a given input combination. The outputs are equal to:

$$D0 = A0B0 \quad D1 = A0B1 \quad D2 = A0B2$$
$$D3 = A1B0 \quad D4 = A1B1 \quad D5 = A1B2$$
$$D6 = A2B0 \quad D7 = A2B1 \quad D8 = A2B2$$

The outputs x in Table 5 can be either 0 or 1. In both cases, the output line will be inactive.

Here we present two approaches to constructing the proposed quantum ternary decoder.

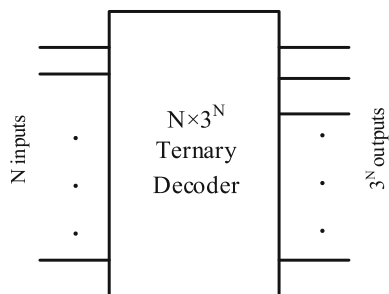**Fig. 6** Block diagram of $N \times 3^N$ ternary multiplexer circuit

Table 5 2×9 ternary decoder truth table.

Inputs (AB)	Outputs								
	D0	D1	D2	D3	D4	D5	D6	D7	D8
00	2	x	x	x	x	x	x	x	x
01	x	2	x	x	x	x	x	x	x
02	x	x	2	x	x	x	x	x	x
10	x	x	x	2	x	x	x	x	x
11	x	x	x	x	2	x	x	x	x
12	x	x	x	x	x	2	x	x	x
20	x	x	x	x	x	x	2	x	x
21	x	x	x	x	x	x	x	2	x
22	x	x	x	x	x	x	x	x	2

x: OFF, 2: ON.

3.1.1 The primary quantum ternary decoder design approach

In the Primary Quantum Ternary Decoder Design Approach (*PQTDA*), only one of the outputs will be equal to 2 for a given input combination, and the remaining outputs will be equal to 0 (i.e., $x = 0$). For better comprehension, first, we show the quantum ternary decoder operation in three parts (Fig. 7a-c). Then show the complete design in Fig. 7d. The realization of the first part is shown in Fig. 7a, which consists of five 1-qutrit permutation gates and nine 2-qutrit Muthukrishnan–Stroud gates. In the first part, if inputs *A* and *B* are equal to *00*, only output *D0* will be equal to *2*; however, when inputs *A* and *B* are *01*, only output *D1* is *2*; whereas if *A* and *B* are *02* will result in output *D2* to be *2*.

The realization of the second part is shown in Fig. 7b using five 1-qutrit permutation gates and nine 2-qutrit Muthukrishnan–Stroud gates. In this part, if inputs *A* and *B* are equal to *10*, only output *D3* will be equal to *2*; when inputs *A* and *B* are *11*, output *D4* is *2*; and if *A* and *B* are *12*, output *D5* will be *2*.

The realization of the last part is shown in Fig. 7c. In this part, if the inputs *A* and *B* are equal to *20*, only the output *D6* will be equal to *2*; when inputs *A* and *B* are *21*, output *D7* will be *2*; and finally, if *A* and *B* are *22*, output *D8* will be *2*. The realization of the proposed quantum ternary decoder is shown in Fig. 7d. As can be seen, twelve 1-qutrit permutation gates and twenty-seven 2-qutrit Muthukrishnan–Stroud gates were used in the proposed decoder. This circuit has a quantum cost of *39*. The outputs of this circuit for different input combinations are illustrated in Table 6. The depth of the proposed quantum ternary decoder circuit in Fig. 7d is 30.

3.1.2 Optimized quantum ternary decoder design approach

In the Optimized Quantum Ternary Decoder Design Approach (*OQTDA*), we present a lower quantum cost ternary decoder. In this optimized realization, all unselected
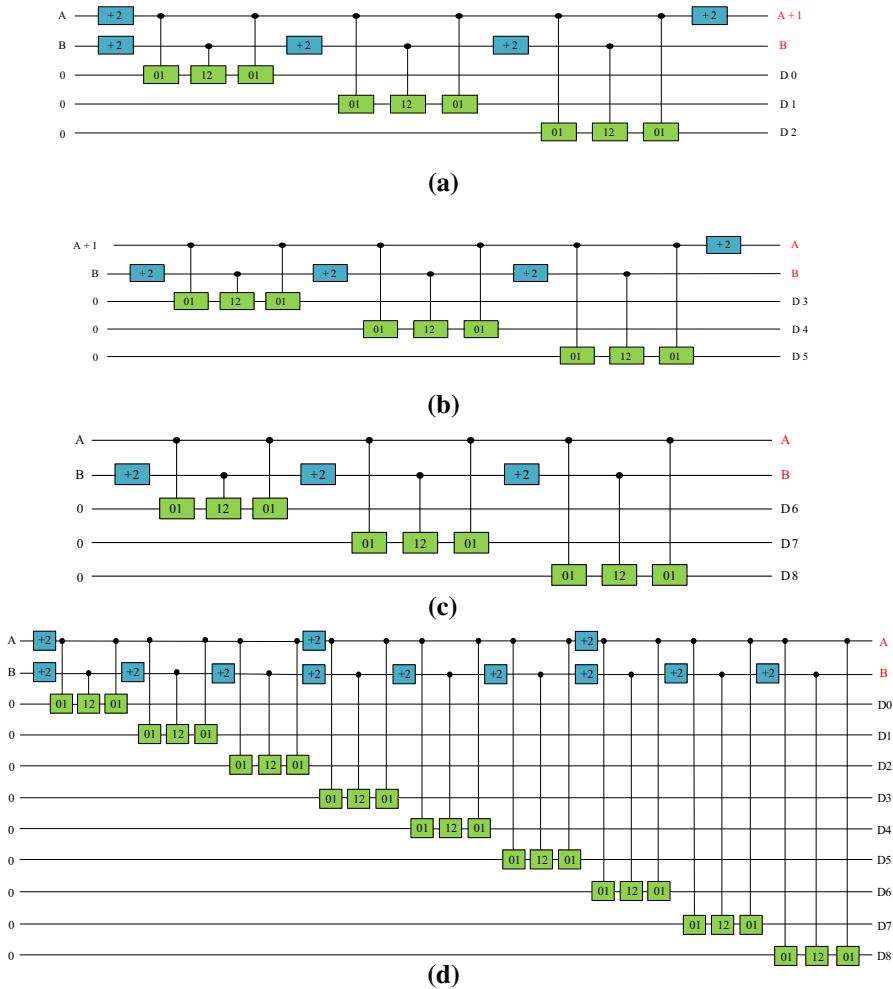
Fig. 7 The proposed *PQTDA*. **a** The first part. **b** The second part. **c** The third part. **d** Complete realization of *PQTDA* using 2-qutrit M–S and 1-qutrit permutation gates

outputs are allowed to take on the value 1 or 0 while only the selected output to be equal to 2. To design this circuit, we have used 1-qutrit permutation gates and 2-qutrit Muthukrishnan–Stroud. The proposed circuit is realized in Fig. 8. As shown, nine 1-qutrit permutation gates and eighteen 2-qutrit Muthukrishnan–Stroud gates are used. The quantum cost of this circuit is 27, resulting in a great improvement with respect to overall implementation cost and circuit depth as compared to *PQTDA*. The outputs of this circuit are shown in Table 7. The depth of the proposed quantum ternary decoder circuit in Fig. 8 is 18. It is to be noted that in *OQTDA*, at the first line, the output is restored to input A. If it is not essential to restore this input at the output, we can remove the last + 1 gate, which is marked with a red-colored dashed line in Fig. 8. As

Table 6 *PQTDA* truth table

Inputs (AB)	Outputs								
	D0	D1	D2	D3	D4	D5	D6	D7	D8
00	2	0	0	0	0	0	0	0	0
01	0	2	0	0	0	0	0	0	0
02	0	0	2	0	0	0	0	0	0
10	0	0	0	2	0	0	0	0	0
11	0	0	0	0	2	0	0	0	0
12	0	0	0	0	0	2	0	0	0
20	0	0	0	0	0	0	2	0	0
21	0	0	0	0	0	0	0	2	0
22	0	0	0	0	0	0	0	0	2

0: OFF, 2: ON
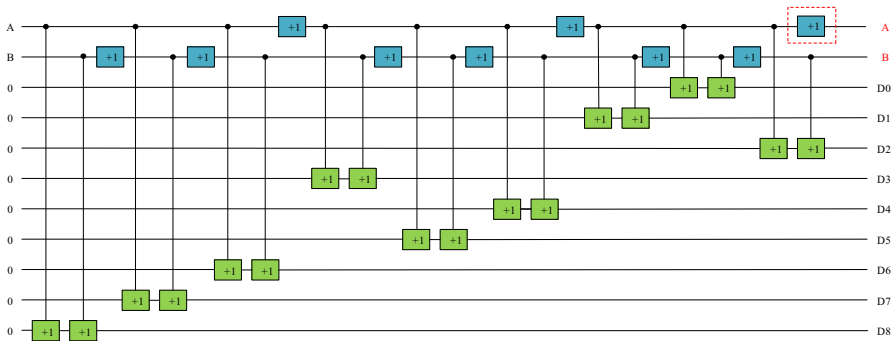
Fig. 8 *OQTDA* realization

Table 7 *OQTDA* truth table

Inputs (AB)	Outputs								
	D0	D1	D2	D3	D4	D5	D6	D7	D8
00	2	1	1	1	0	0	1	0	0
01	1	2	1	0	1	0	0	1	0
02	1	1	2	0	0	1	0	0	1
10	1	0	0	2	1	1	1	0	0
11	0	1	0	1	2	1	0	1	0
12	0	0	1	1	1	2	0	0	1
20	1	0	0	1	0	0	2	1	1
21	0	1	0	0	1	0	1	2	1
22	0	0	1	0	0	1	1	1	2

0, 1: OFF, 2: ON

a result, the quantum cost is reduced to 26, and the output on the first line will become A + 2.

3.2 The proposed quantum ternary multiplexer circuit

A multiplexer circuit has one output, multiple inputs, and selectors. Selectors specify which inputs are gated to the output. A ternary multiplexer takes N ternary numbers as selectors and 3^N ternary numbers as input and gives output as a number. The block diagram of $3^N \times 1$ ternary multiplexer circuit is illustrated in Fig. 9. Table 8 shows the truth table of 9×1 ternary multiplexer, where A and B are selectors, and $I0$, $I1$, $I2$, $I3$, $I4$, $I5$, $I6$, $I7$, and $I8$ are the inputs, and the output is depicted as O. For a given selector combination, only the selected input will be gated to the output.

According to Table 8, the output is equal to:

O = (A0B0) I0 + (A0B1) I1 + (A0B2) I2 + (A1B0) I3 + (A1B1) I4 + (A1B2) I5 + (A2B0) I6 + (A2B1) I7 + (A2B2) I8.

To construct a ternary multiplexer circuit, we use the proposed quantum ternary decoder and ternary Controlled Feynman gates. The realization of the proposed multiplexer is shown in Fig. 10. In this circuit, input restoration is necessary, where *PQTDA*, nine ternary controlled Feynman, and sixty-three 2-qutrit Muthukrishnan–Stroud gates are used. In this implementation, the outputs preserve their corresponding inputs by

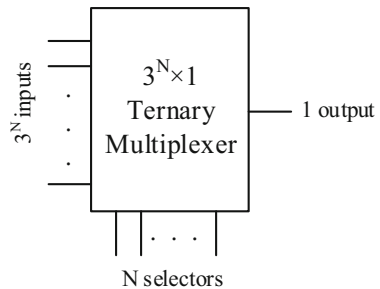**Fig. 9** Block diagram of $3^N \times 1$ ternary multiplexer circuit

Table 8 9×1 ternary multiplexer truth table.

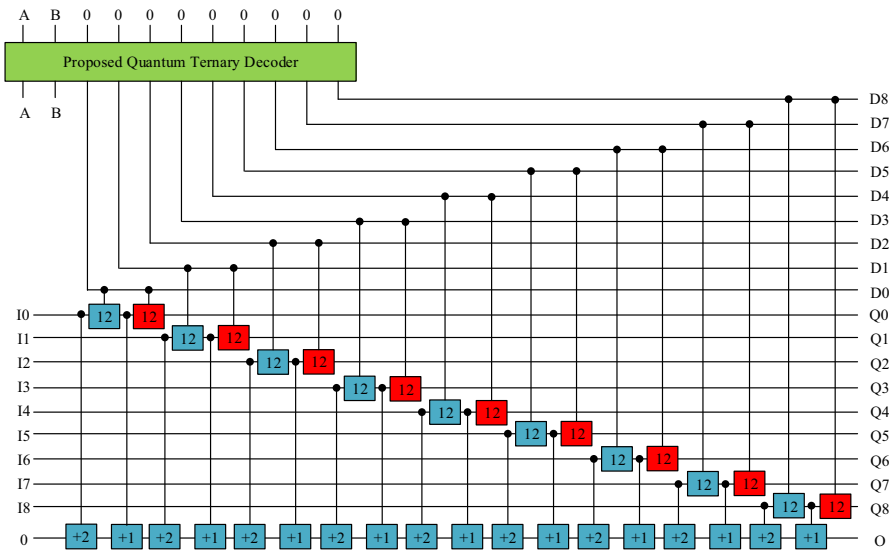| Selectors (AB)	Output (O)
00	I0
01	I1
02	I2
10	I3
11	I4
12	I5
20	I6
21	I7
22	I8

Fig. 10 Realization of the proposed quantum ternary multiplexer circuit

utilizing nine Muthukrishnan–Stroud gates shown in red in the figure, resulting in a total quantum cost of *75*. Cost can be further decreased to *53* if input restoration is not necessary and can be accomplished using *OQTDA* and removing the 1-qutrit permutation gates shown in red from Fig. 10.

3.3 The proposed quantum ternary demultiplexer circuit

A demultiplexer circuit has one input, multiple outputs, and selectors. The selector specifies how the input is switched to the specified output. *A* ternary demultiplexer takes N ternary numbers as selectors and one ternary number as input and gives 3^N numbers as outputs. The block diagram of 1×3^N ternary demultiplexer is shown in Fig. 11, whereas Table 9 shows the truth table of 1×9 ternary demultiplexer. The input is specified as *I*, selectors are *A* and *B*, and outputs as *O*. Only one of the outputs will be equal to *I* for a given selectors combination, and the remaining ones will be *0*.

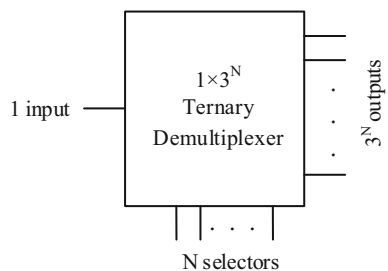**Fig. 11** Block diagram of 1×3^N ternary demultiplexer circuit

Table 9 1×9 ternary demultiplexer truth table.

Selectors (AB)	Outputs								
	O0	O1	O2	O3	O4	O5	O6	O7	O8
00	I	0	0	0	0	0	0	0	0
01	0	I	0	0	0	0	0	0	0
02	0	0	I	0	0	0	0	0	0
10	0	0	0	I	0	0	0	0	0
11	0	0	0	0	I	0	0	0	0
12	0	0	0	0	0	I	0	0	0
20	0	0	0	0	0	0	I	0	0
21	0	0	0	0	0	0	0	I	0
22	0	0	0	0	0	0	0	0	I

According to Table 9, The outputs are equal to:

$$O0 = A0B0I \quad O1 = A0B1I \quad O2 = A0B2I$$
$$O3 = A1B0I \quad O4 = A1B1I \quad O5 = A1B2I$$
$$O6 = A2B0I \quad O7 = A2B1I \quad O8 = A2B2I$$

The proposed decoder and ternary-controlled Feynman gates are used to construct the ternary demultiplexer circuit. The proposed quantum ternary demultiplexer is realized in Fig. 12. In this circuit, input restoration is necessary, and the proposed *PQTDA* and nine ternary controlled-Feynman gates are utilized. By using the red-colored Muthukrishnan–Stroud gates, inputs can be restored, leading to a total quantum cost of *75*. However, if input restoration is not necessary, then *OQTDA* design can be used, along with removing red-colored gates, decreasing the quantum cost to *53*.

4 Result assessment

The proposed quantum ternary decoders, multiplexer, and demultiplexer are analyzed with respect to their quantum cost, depth, number of garbage outputs, and constant inputs. These are the most important metrics to evaluate the efficiency of any quantum circuits.

Table 10 compares our proposed quantum ternary decoder circuit with its counterpart in [31]. As can be seen, the proposed decoder (*OQTDA*) has less quantum cost, depth, garbage outputs, and constant inputs than the design in [31], eliminating 27 M-S gates and four permutation gates and reducing by one both constant input and garbage output.

According to Table 10, the proposed multiplexer improves quantum cost, depth, garbage outputs, and constant inputs when compared with the similar circuit suggested
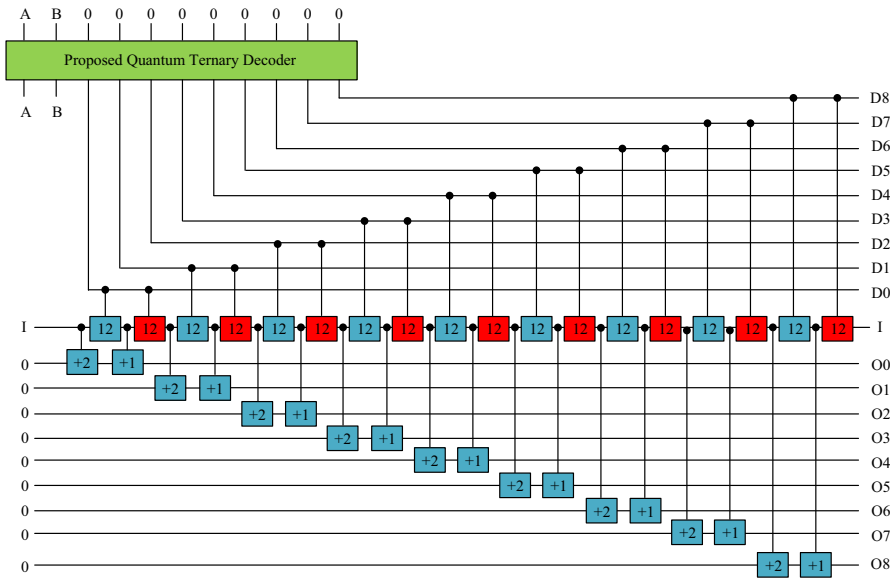
Fig. 12 Realization of the proposed ternary demultiplexer circuit

in [30]. In particular, the improvement in quantum cost, depth, garbage outputs, and constant inputs are 48%, 41%, 4%, and 9%, respectively.

The comparison in Table 10 clearly demonstrates the proposed design of the demultiplexer leads to improvements in terms of quantum cost (48%), depth (41%), garbage outputs (7%), and constant inputs (5%) as compared to its counterpart in [30].

It should be noted that although all the proposed designs are more efficient when compared with the circuits suggested in [30, 31], the comparison has been done using the best-proposed designs, which do not restore inputs.

5 Conclusion

Quantum ternary circuits are the new generation of quantum circuits, and they have advantages over their binary counterparts. Many quantum ternary circuits and optimization approaches to construct different computational units of quantum computers and other complicated systems have been investigated in the literature. This paper proposes two new realizations of quantum ternary decoder by using 1-qutrit permutation gates and 2-qutrit Muthukrishnan–Stroud gates. We have also presented quantum ternary multiplexer and demultiplexer based on the realization of the decoder circuit. The proposed circuits in this work reduce quantum cost, depth, the number of garbage outputs, and constant inputs. Since the lower values of these figures of merit lead to more efficient quantum ternary circuit designs compared to the existing counterparts, our proposed realizations are more efficient. In addition, the proposed designs in this

Table 10 Evaluation of quantum ternary decoder, multiplexer, and demultiplexer circuits

	Decoder Designs			Multiplexer Designs			Demultiplexer Designs		
	OQTDA	Design in [31]	Improvement percentage	Proposed design	Design in [30]	Improvement percentage	Proposed design	Design in [30]	Improvement percentage
Quantum Cost	26	57	54%	53	102	48%	53	102	48%
Depth	18	54	66%	44	75	41%	44	75	41%
Constant Input	9	10	10%	10	11	9%	18	19	5%
Garbage Output	2	3	33%	20	21	4%	12	13	7%
Input restoration capability	No	Yes	–	No	Yes	–	No	Yes	–

study can be utilized to design various components for ternary quantum computers and other intricate computational systems.

6 Data availability statement

Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

Author contributions All authors contributed equally to the paper. All authors read and approved the final manuscript.

Declarations

Conflict of interest The authors declare no conflict of interest.

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