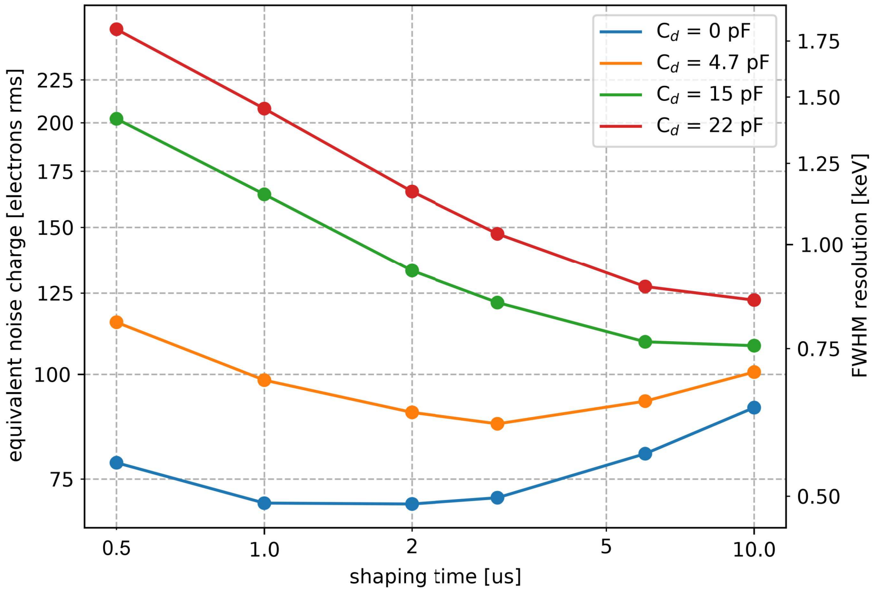

Figure 4.32: CSP equivalent noise charge and energy resolution measurements. Different capacitors were connected between the CSP input node and ground to simulate different electrodes capacitances.

shaping time [μs]		0.5	1	2	3	6	10
ASIC CSP	RES_{fwhm} [keV]	1.41	1.15	0.93	0.85	0.76	0.75
	ENC [e^-_{rms}]	202	164	133	122	109	108
PANDORA CSP	RES_{fwhm} [keV]	1.79	1.44	1.19	1.09	1.01	0.97
	ENC [e^-_{rms}]	256	206	169	156	145	138
PANDORA CSP_{cold}	RES_{fwhm} [keV]	-	1.22	0.98	0.88	0.80	0.79
	ENC [e^-_{rms}]	-	178	143	128	116	115

Table 4.6: Comparison of the ENC and energy resolution performance between the ASIC developed in this work and the discrete-component charge sensitive preamplifier designed for the PANDORA experiment, tested both at room temperature and with input transistor and feedback resistor cooled to cryogenic temperature (approximately 130 K).

4.3.3 Noise Power Spectral Density Analysis

To study the CSP noise power spectral density, the circuit was directly connected to an Agilent 4395A Network/Spectrum Analyzer, as illustrated in Fig. 4.34. On one side, the device measures, frequency by frequency, the ratio between the amplitude of the CSP output signal, v_{out}, and that of the applied input signal, v_{in}. This result gives us the possibility to find, frequency by frequency, the circuit transfer function:

$$H(f) = \frac{100}{11}\frac{1}{2\pi f C_t} \cdot \frac{v_{out}}{v_{in}} \tag{4.45}$$

On the other side, this device calculates the noise output power spectral density, providing information on the frequency-dependent noise characteristics of the circuit.

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[8] In practice, however, the actual resolution of a real detector is degraded by several additional factors, such as spatial variations in detector response and incomplete charge collection.

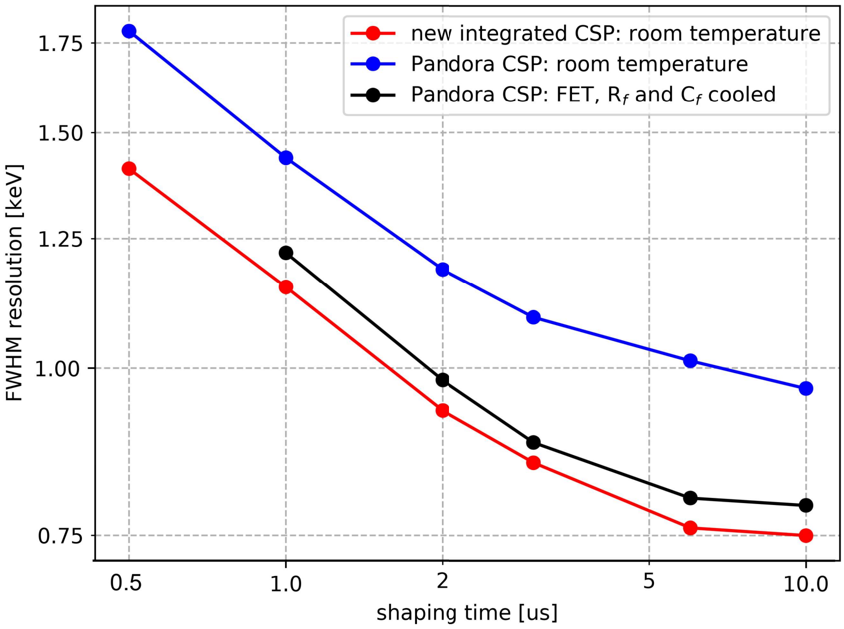

Figure 4.33: Comparison of the ENC and energy resolution performance between the ASIC developed in this work (red line) and the discrete-component charge sensitive preamplifier designed for the PANDORA experiment, tested both at room temperature (blue line) and with input transistor and feedback resistor cooled to approximately 130 K (black line).

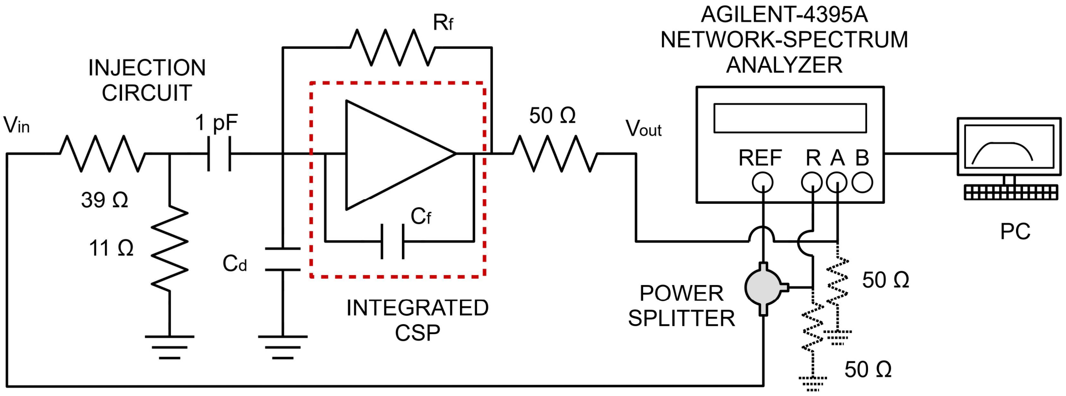

Figure 4.34: Electronic chain used to measure the preamplifier transfer function and output spectral density of noise. For noise measurements, the test input was short-circuited to ground and the power splitter was removed from the setup.

Fig. 4.35 shows both the transfer function and the output-referred power spectral density evaluated for different values of C_d capacitance. The input-referred noise power spectral density, reported in Fig. 4.36, can be finally obtained as follows:

$$S_{in}(f) = \frac{S_{out}(f)}{|H(f)|^2} \tag{4.46}$$

As previously done, the PSD curves were fitted using the functional form described in Eq. 3.58. This allowed the extraction of the fit coefficients a, b and c, defined in Eq.

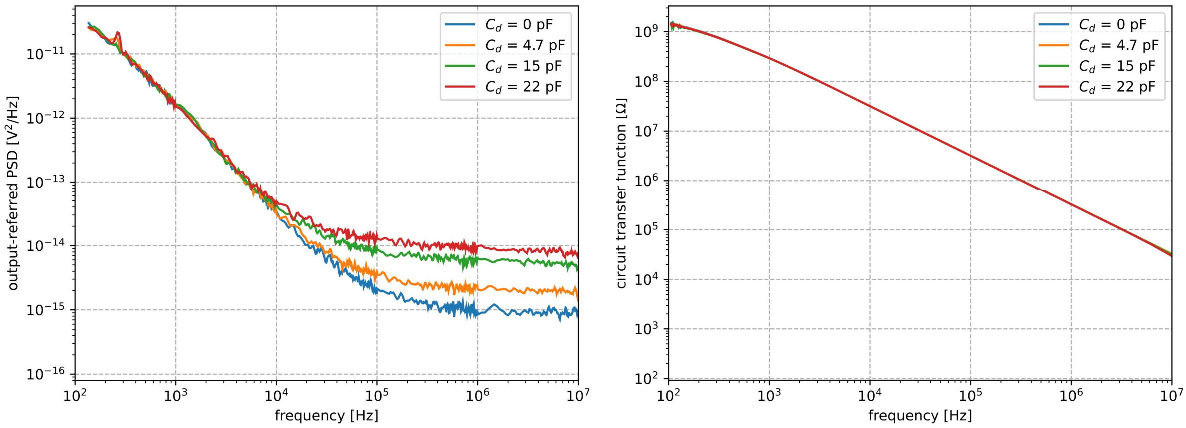

Figure 4.35: On the left, CSP output-referred noise power spectral density. On the right CSP transfer function H(f). As expected H(f) doesn't depend on the detector capacitance C_d.

3.59, for various detector capacitance values.

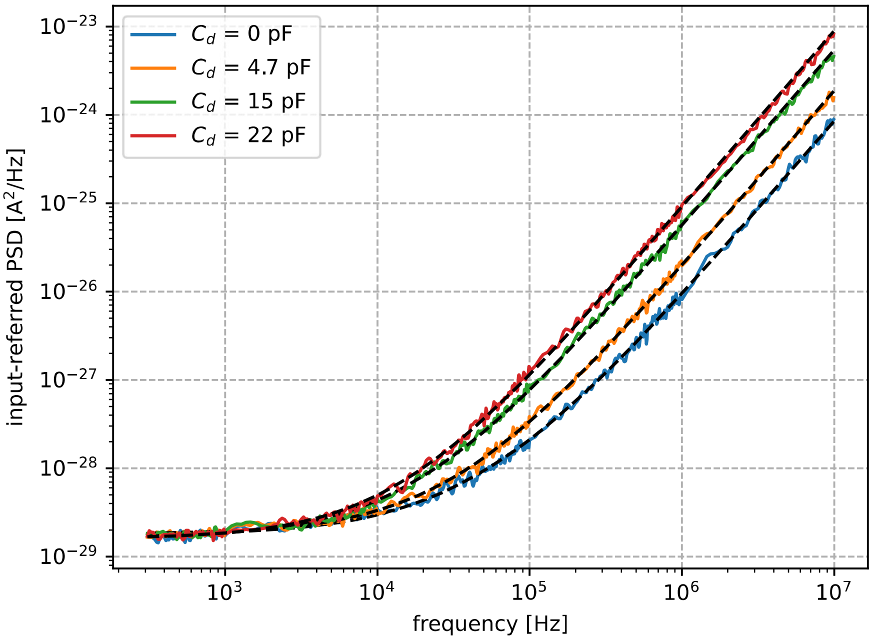

Figure 4.36: CSP input-referred noise power spectral density measured for different values of detector capacitance. The dashed clack lines represent the fit curves based on Eq. 3.58.

The white parallel noise coefficient a was found to lie between $1.59 \times 10^{-29}\ \mathrm{A}^2\,\mathrm{Hz}^{-1}$ and $1.79\times10^{-29}\ \mathrm{A}^2\,\mathrm{Hz}^{-1}$, in agreement with the simulated value of $1.66\times10^{-29}\ \mathrm{A}^2\,\mathrm{Hz}^{-1}$.

The noise coefficient b, on the other hand, shows no agreement with the simulation predictions, as illustrated in Fig. 4.37. As evident from the data, there is not only a discrepancy with the simulations, but also a deviation from the expected behavior. As a matter of fact, attempts to fit the data using either Eq. 4.27 or Eq. 4.33 were unsuccessful. As a direct consequence, and in contrast to the simulations, it was not possible to extract the CSP input capacitance from this experimental data.

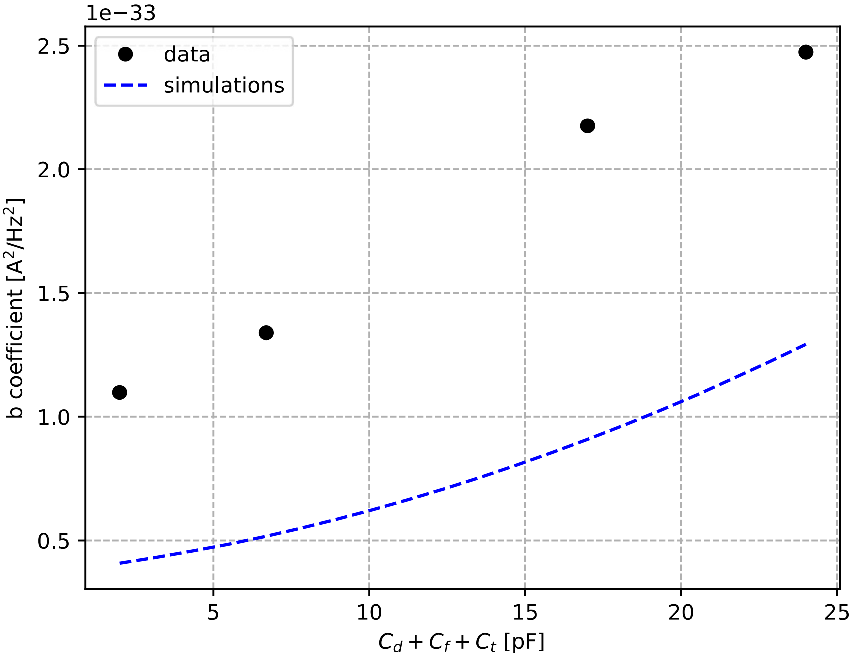

Figure 4.37: Noise coefficient b determined by fitting the experimental input-referred power spectral densities obtained for different values of detector capacitance. As evident from the data, there is not only a discrepancy with the simulations, but also a deviation from the expected behavior of (4.33).

Let us now consider the white series noise coefficient c, reported in Fig. 4.38. Neglecting, for now, second-order effects introduced by the ESD protection resistor (Eq.4.41), we can write (Eq. 4.34):

$$c = (2\pi)^2 \frac{4kT\gamma}{g_m}(C_d + C_f + C_t + C_{in})^2$$

As the input capacitance of the CSP is unknown, it can be estimated by fitting the data with the following function:

$$y = k \cdot (x + p)^2$$

where x = $C_d + C_f + C_t$, y = c and the parameters k and p are the fit coefficients. The results of this fit procedure are shown in Fig. 4.38. As observed, the fitting curve shows excellent agreement with the experimental data. From the fit coefficients we can estimate C_{in} and g_m, the CSP input transistor transconductance:

$$\begin{aligned} C_{in} &= p = 7.8\,\text{pF} \\ g_m &= \frac{4kT\gamma}{k} = 4.95\,\text{mS} \qquad (\gamma = 2/3) \end{aligned} \tag{4.47}$$

While the extracted capacitance matches the expected one ($7.7\,\text{pF}$), the extracted transconductance is slightly lower than the simulated value ($6.2\,\text{mS}$), possibly due to a process corner. This discrepancy explains the small differences observed between the experimental and simulated coefficients, which can be accurately fitted by ignoring the noise contribution from the ESD protection resistor (see Fig. 4.38). Because the transconductance appears in the denominator of its associated noise term, a lower value increases

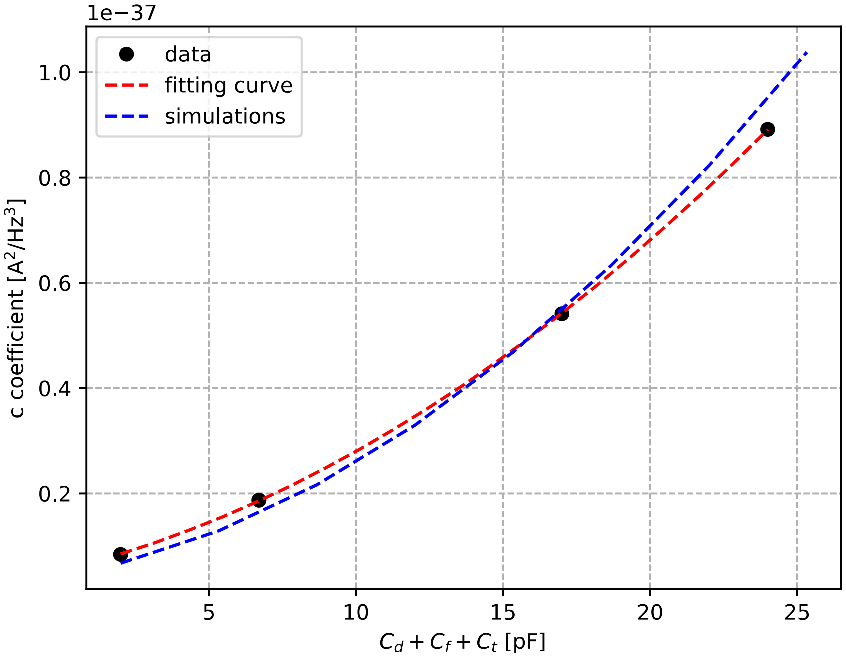

Figure 4.38: White series noise coefficient c determined by fitting the experimental input-referred power spectral densities obtained for different values of detector capacitance. The fitting curve has the form $c = k(C_d + C_f + C_t + p)^2$, with k = $8.79 \cdot 10^{-17}$ and p = $7.84 \cdot 10^{-12}$.

its relative contribution to the overall noise. As a result, the noise contribution from the ESD protection resistor becomes negligible [9]. This allows Eq. 4.41 to be simplified into Eq. 4.34.

We now come back to the analysis of the noise coefficients b. In order to extend the available capacitance range and increase the number of data points, we repeated the measurements of noise power spectral density using the following values of C_d: 0 pF, 22 pF, 44 pF, 66 pF, 88 pF and 110 pF. These were obtained by soldering multiple 22 pF capacitors of the same type in parallel. With this new dataset, and knowing the CSP input transistor capacitance, we performed a new fitting procedure using the following function (Eq. 4.32):

$$y = k \cdot x^2 + q \tag{4.48}$$

where x = $C_d + C_f + C_t + C_{in}$, y = b and the parameters k and q are the fit coefficients. The results obtained are reported in Fig. 4.39.

From k and q we found the experimental flicker noise parameter of the CSP input transistor, A_f, and that of the line-driver input transistor, A'_f: $A_f = 1.93 \times 10^{-14}\,\mathrm{V}^2$, $A'_f = 4.00 \times 10^{-11}\,\mathrm{V}^2$. While A_f is consistent with the simulated value ($2.46 \times 10^{-14}\,\mathrm{V}^2$), A'_f deviates from it significantly ($8.11 \times 10^{-12}\,\mathrm{V}^2$). As a consequence, we suggest the presence of a noise contribution that is not accounted for by the simulator. This contri-

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[9] The actual resistance value may be lower than the 30 Ω implemented. As previously noted, the foundry does not guarantee precise control over such low resistance values in the adopted integration technology. A lower actual resistance would result in a further reduction of its associated noise contribution, thereby reinforcing the assumption that the impact of the ESD protection resistor can be neglected in the experimental noise analysis.

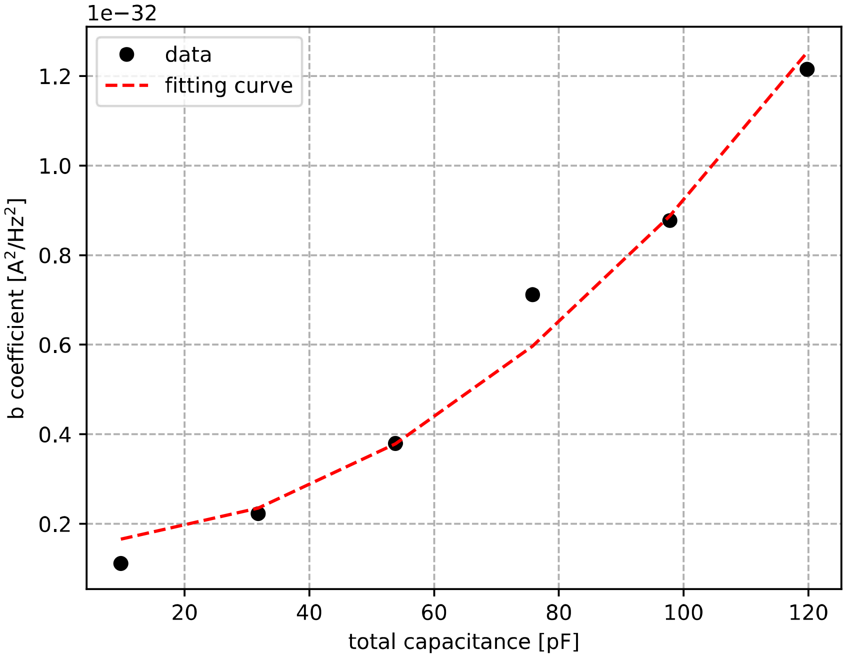

Figure 4.39: b coefficients determined by fitting the experimental noise input-referred power spectral densities obtained with the new dataset of C_d capacitances. The fitting curve has the form $b = k(C_d + C_f + C_t + C_{in})^2 + q$, with k = $7.62 \cdot 10^{-13}$ and q = $1.58 \cdot 10^{-33}$. The coefficient of determination is R^2 = 0.980.

bution can not be related to the integrated circuit itself, but rather to the test PCB. We think it is dielectric noise, whose power spectral density exhibit the same behavior of the $1/f$ noise (Appendix B). Since the PCB was manufactured on a PTFE substrate, which features very low dielectric losses ($\tan\delta < 0.0012$), we believe that this additional noise mostly originates from the dielectric material of the SMD capacitors soldered at the input node: C_d and C_t.

According to this hypothesis, Eq. 4.32 would be rewritten as follows:

$$b = (2\pi)^2 \cdot A_f \cdot [C_d + C_f + C_t + C_{in}]^2 + (2\pi)^2 C_f^2 A'_f + \lambda \cdot (C_d + C_t) \;, \tag{4.49}$$

with the last term corresponding to the dielectric noise contribution and λ defined in Eq. A.12 (see Appendix B). Therefore, the noise coefficients b could be fitted using a function of the form:

$$y = k \cdot (x + C_f + C_{in})^2 + \lambda \cdot x + q \tag{4.50}$$

with x = $C_d + C_t$ and y = b. The outcomes of this new fitting procedure are shown in Fig. 4.40. From the fit coefficients, we derive the following parameters: A_f =$1.10 \times 10^{-14}\,\mathrm{V}^2$, A'_f =$2.14 \times 10^{-11}\,\mathrm{V}^2$ and λ = $4.56 \times 10^{-23}\,\mathrm{A}^2/(\mathrm{Hz}^2\mathrm{F})$. Using Eq. A.12 for λ, we obtain the following value of dielectric loss: $\tan\delta = 0.0005$. This is fully consistent with the specifications of the NP0 capacitors employed in our PCB: $\tan\delta < 0.001$ [48]. Since the experimental value of A'_f is still greater than the simulated one, we may consider the q coefficient as the sum of the noise contribution of the line-driver input-transistor and that of the PCB substrate, $\tilde{b}$. This allows us to complete Eq. 4.49:

$$b = (2\pi)^2 \cdot A_f \cdot [C_d + C_f + C_t + C_{in}]^2 + (2\pi)^2 C_f^2 A'_f + \tilde{b} + \lambda \cdot (C_d + C_t) \tag{4.51}$$

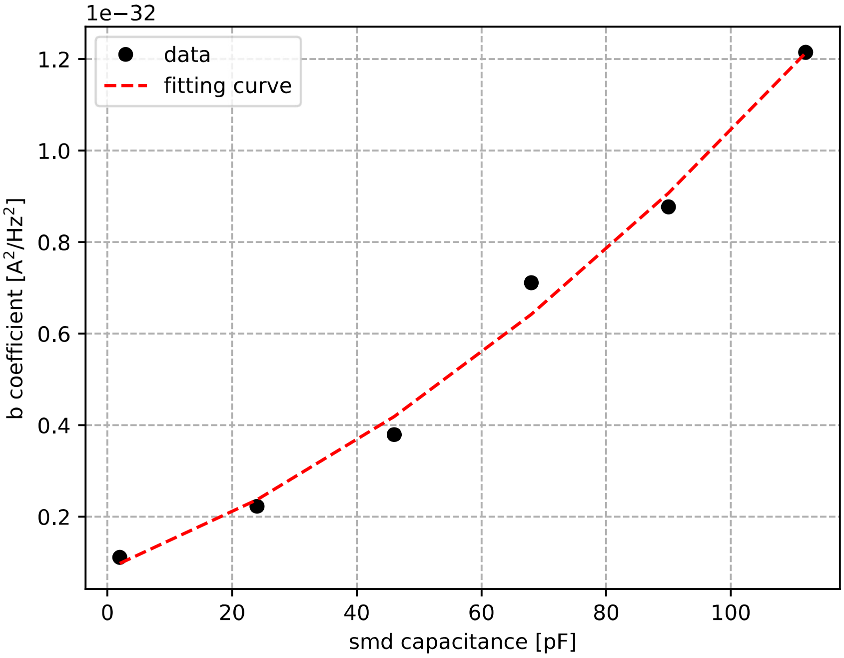

Figure 4.40: b coefficients determined by fitting the experimental noise input-referred power spectral densities obtained with the new dataset of C_d capacitances. The fitting curve has the form $b = k(C_d + C_f + C_t + C_{in})^2 + \lambda \cdot (C_d + C_t) + q$, with k = $4.31 \cdot 10^{-13}$, λ = $4.56 \cdot 10^{-23}$ and q = $8.45 \cdot 10^{-34}$. The coefficient of determination is R^2 = 0.991.

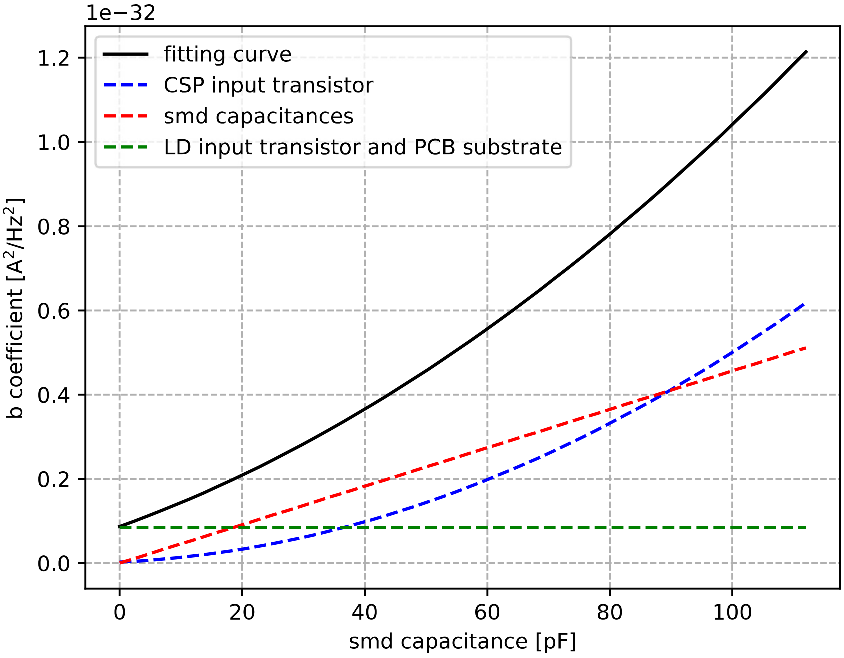

Figure 4.41: Different noise contributions to the b coefficient.

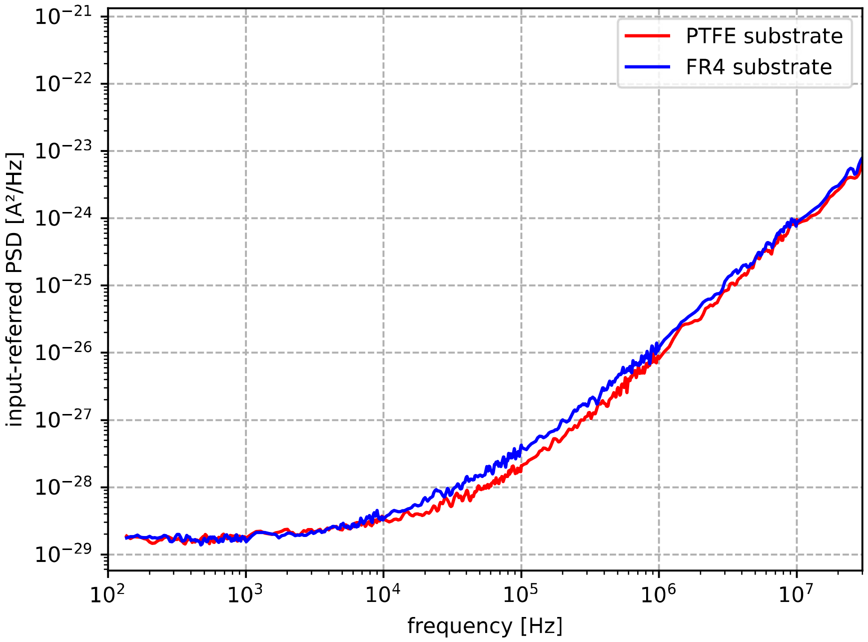

Figure 4.42: Comparison of the CSP input-referred noise power spectral density with the ASIC mounted on either a PTFE or FR4 substrate. While the curves overlap at low and high frequencies, a clear discrepancy emerges at mid frequencies due to the substrate noise contribution. Measurements were performed with zero detector capacitance.

Fig. 4.41 illustrates the individual noise contributions to the b coefficient. As shown, at low capacitance values, the dominant contribution originates from the PCB substrate, followed by the dielectric noise of the SMD capacitors connected to the CSP input node and finally by the intrinsic flicker noise of the CSP input transistor.

To better understand how the dielectric properties of the PCB substrate affect the noise performance of the charge sensitive preamplifier, we designed a test board using standard FR4 material, replicating the layout of the PTFE-based PCB previously used for ASIC characterization. Both boards were tested under identical conditions, with the detector capacitance set to zero in order to focus on the spectral region where substrate noise is expected to dominate.

The comparison between the input-referred noise power spectral densities are reported in Fig. 4.42. While the noise spectra overlap at low and high frequencies, a clear discrepancy emerges at mid frequencies, where the input-referred power spectral density exhibits an f-proportional dependence. In this regime, the FR4-based implementation shows a higher noise level compared to its PTFE counterpart. This discrepancy is attributed to the higher dielectric loss of FR4. This effect can also be observed by comparing the equivalent noise charge curves obtained for the two substrates, as reported in Fig. 4.43.

We complete the analysis by showing the resolution curves obtained with the FR4 substrate for different values of detector capacitance C_d (see Fig. 4.44 and Tab. 4.7).

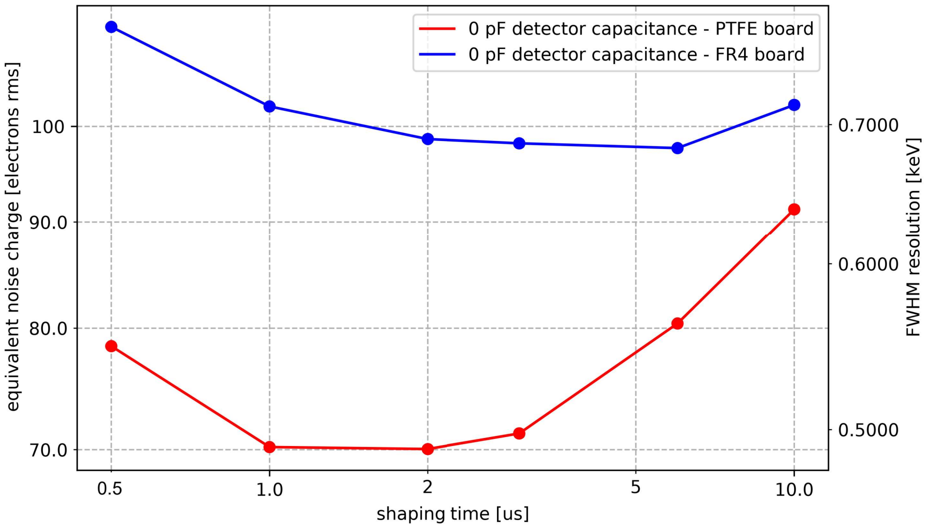

Figure 4.43: Equivalent Noise Charge comparison for the CSP mounted on PTFE and FR4 substrates. The observed discrepancy highlights the impact of substrate-related noise, particularly visible in the absence of detector capacitance. $1\,\mathrm{MeV}$ equivalent events were considered.

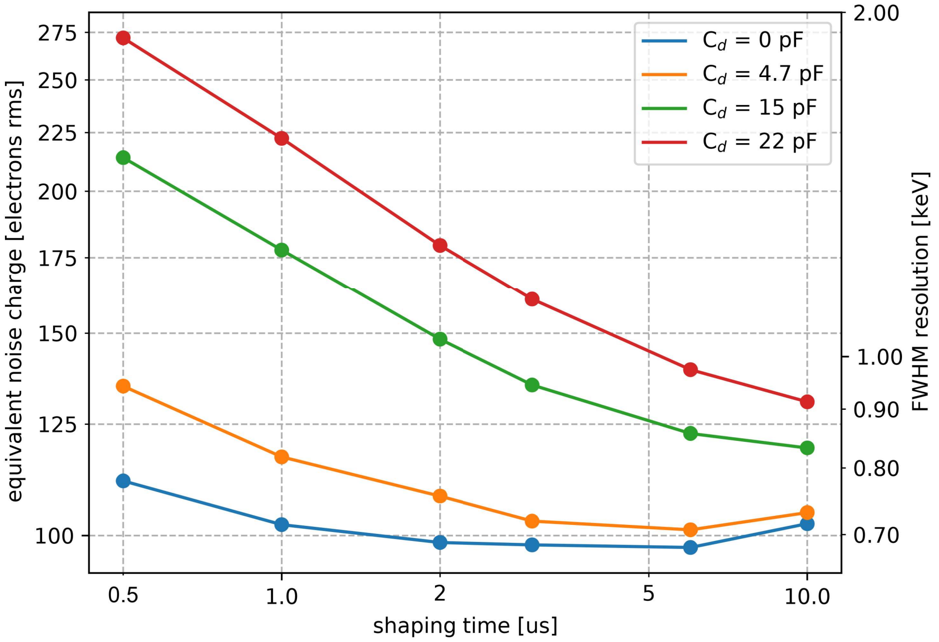

Figure 4.44: CSP equivalent noise charge and energy resolution measurements on FR4 substrate. Different capacitors were connected between the CSP input node and ground to simulate different electrodes capacitances. As observed, the increased dielectric noise contribution from the substrate leads to significantly flatter curves compared to those measured with the ASIC mounted on a PTFE substrate. This is particularly evident for C_d values of $0\,\mathrm{pF}$ and $4.7\,\mathrm{pF}$.

shaping time [μs]		0.5	1	2	3	6	10
C_d = 0 pF	RES$_{fwhm}$ [keV]	0.78	0.71	0.69	0.69	0.68	0.72
	ENC [e$^-_{rms}$]	111	102	98	98	97	102
C_d = 4.7 pF	RES$_{fwhm}$ [keV]	0.94	0.82	0.76	0.72	0.71	0.73
	ENC [e$^-_{rms}$]	135	117	108	103	101	105
C_d = 15 pF	RES$_{fwhm}$ [keV]	1.49	1.24	1.04	0.94	0.86	0.83
	ENC [e$^-_{rms}$]	214	178	148	135	122	119
C_d = 22 pF	RES$_{fwhm}$ [keV]	1.90	1.55	1.25	1.12	0.97	0.91
	ENC [e$^-_{rms}$]	272	222	179	160	139	130

Table 4.7: CSP equivalent noise charge and energy resolution measurements. The circuit was mounted and tested on a FR4-based PCB. 1 MeV equivalent pulses were injected and an ORTEC-572 shaping amplifier was connected to the CSP output.

4.4 Single-Ended Preamplifier Optimized for Electron-Collecting Electrode Readout

Fig. 4.45 shows the block diagram of the single-ended ASIC preamplifier optimized for electrodes that collect electrons[10]. The circuit consists of two main building blocks: a preamplifier, designed to maximize the positive voltage swing, and a line driver, capable of driving a $100\,\Omega$ terminated transmission line.

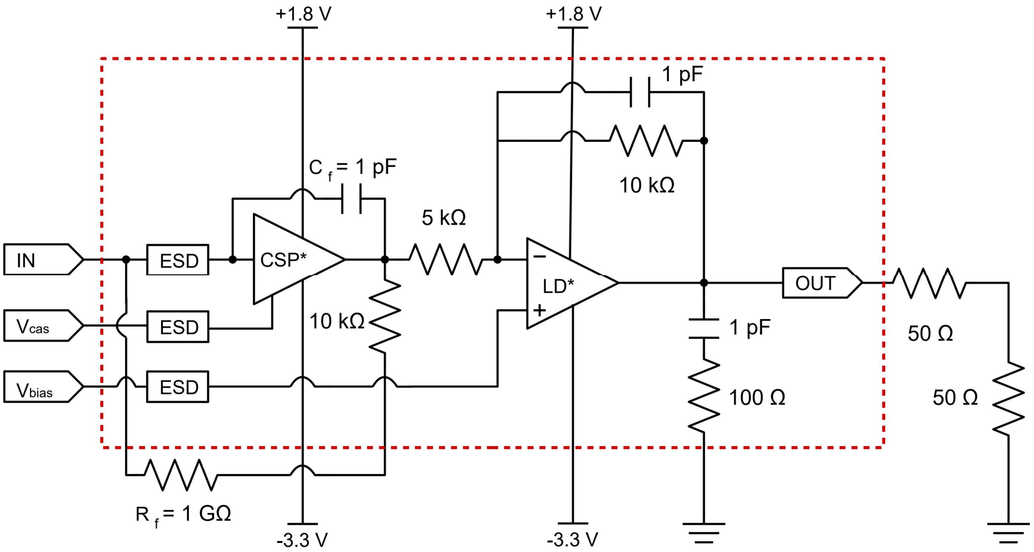

Figure 4.45: Block diagram of the single-ended ASIC preamplifier optimized for reading electron-collecting electrodes. All the integrated elements are included within the red dashed rectangle. To optimize the circuit operation, it is useful to set $V_{cas} = -1.8\,\mathrm{V}$ and $V_{bias} = -0.55\,\mathrm{V}$.

The transistor-level schematic of the preamplifier is shown in Fig. 4.46. Its overall architecture is broadly consistent with the circuit configuration presented in Sec. 4.1. However, the operating points and the output stage have been modified to enhance the circuit positive dynamic range. In particular, the output stage was separately biased using a dedicated current mirror working between $1.8\,\mathrm{V}$ and $-3.3\,\mathrm{V}$.

The line-driver schematic, on the other hand, is shown in Fig.4.47. It consists of an operational transconductance amplifier operating in an inverting configuration. It includes a differential input stage based on nMOS transistors and a compensation network made of a capacitor and a resistor in series, as previously discussed. As in the case of the single-ended preamplifier optimized to read holes-collecting electrodes, a local load was connected to the output node. It consists of a $1\,\mathrm{pF}$ capacitor in series with a $100\,\Omega$ resistor, in order to mitigate the inductive and capacitive parasitism introduced by wire bonding.

The circuit described was experimentally validated according to the setups and procedures described in Sec. 4.3. It features $40.5\,\mathrm{mW}$ power consumption, primarily due to the preamplifier output stage and the line-driver. By considering a $15\,\mathrm{pF}$ detector capacitance, a $35\,\mathrm{ns}$ rise-time was measured. This parameter is higher compared to the CSP optimized for reading hole-collecting electrodes, however it remains fully compatible

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[10] Future detector designs will also include configurations with an external segmented n-type contact. In such arrangements, electrons will be collected by the outer read-out electrodes, producing signals of opposite polarity compared to hole ones. For this reason, charge-sensitive preamplifiers specifically capable of handling these signals were developed and tested.

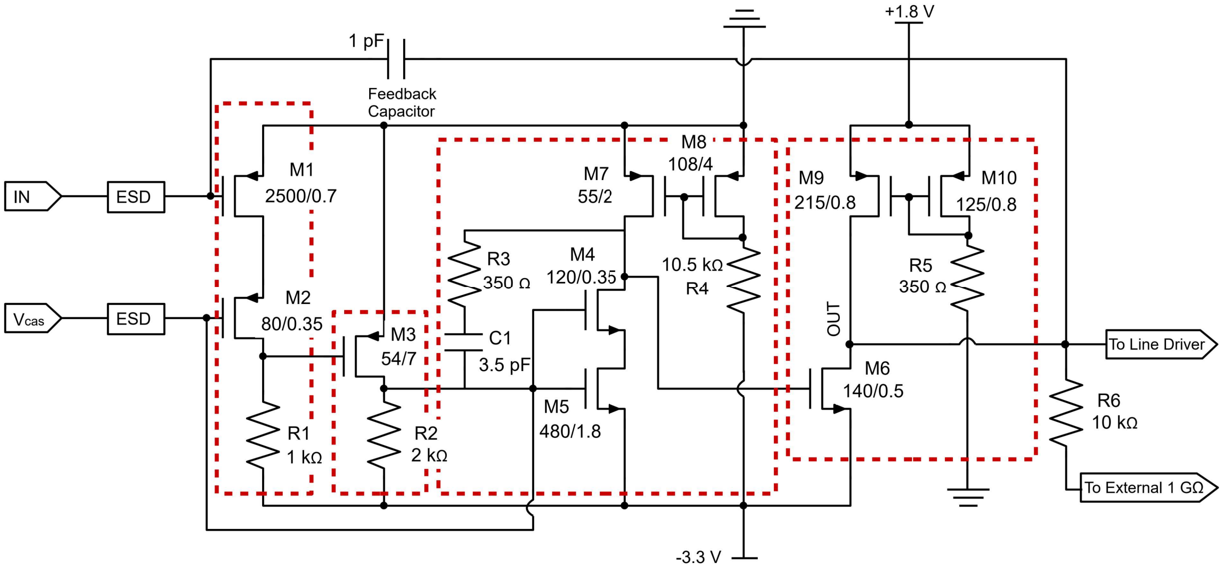

Figure 4.46: Transistor-level schematic of the single-ended ASIC preamplifier optimized for reading electron-collecting electrodes. The four stages of the circuit are outlined by the red dashed rectangles.

shaping time [μs]		0.5	1	2	3	6	10
$C_d = 0\,\text{pF}$	RES_{fwhm} [keV]	0.83	0.69	0.62	0.60	0.62	0.67
	ENC [e^-_{rms}]	118	99	88	85	89	96
$C_d = 4.7\,\text{pF}$	RES_{fwhm} [keV]	1.05	0.85	0.72	0.67	0.66	0.69
	ENC [e^-_{rms}]	150	121	103	96	94	99
$C_d = 15\,\text{pF}$	RES_{fwhm} [keV]	1.61	1.32	1.11	1.01	0.86	0.84
	ENC [e^-_{rms}]	231	189	159	144	123	121
$C_d = 22\,\text{pF}$	RES_{fwhm} [keV]	2.11	1.66	1.33	1.17	0.99	0.92
	ENC [e^-_{rms}]	301	237	191	167	142	132

Table 4.8: CSP equivalent noise charge and energy resolution measurements. The circuit was mounted and tested on a PTFE-based PCB. 1 MeV equivalent pulses were injected and an ORTEC-572 shaping amplifier was connected to the CSP output.

with the requirements of gamma spectroscopy experiments. The reason for the increased rise-time relies on the need to have a stronger compensation of the preamplifier, realized with a 3.5 pF capacitor.

Fig. 4.48 shows the waveforms acquired at the output of the proposed circuit within the equivalent energy range of 1 MeV - 15 MeV. A slight ringing is observed on the rising edge of the signals, however it does not affect the circuit's linearity and resolution. This is demonstrated by an integral non-linearity factor slightly above 3 ‰, as reported in Fig. 4.49.

Finally, Fig. 4.50 and Tab. 4.8 report the measured equivalent noise charge and energy resolution obtained with the ASIC mounted on a test PCB made with PTFE substrate. At shaping times typical of gamma spectroscopy, a resolution better than 0.9 ‰was achieved with $C_d = 15\,\text{pF}$, and better than 1 ‰with $C_d = 22\,\text{pF}$. This represents an excellent result, particularly in comparison with the typical intrinsic resolution values observed for HPGe detectors.

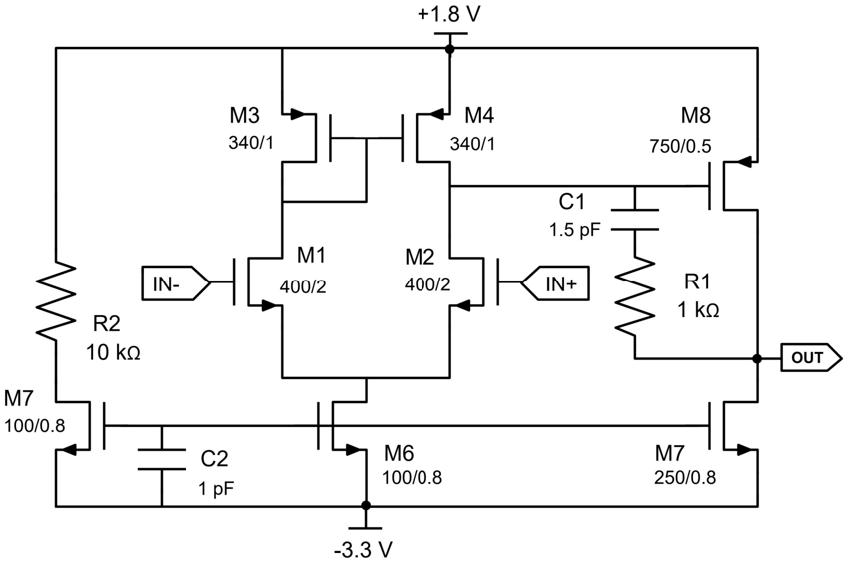

Figure 4.47: Transistor-level schematic of the line-driver connected to the single-ended preamplifier optimized for processing electron-induced signals.

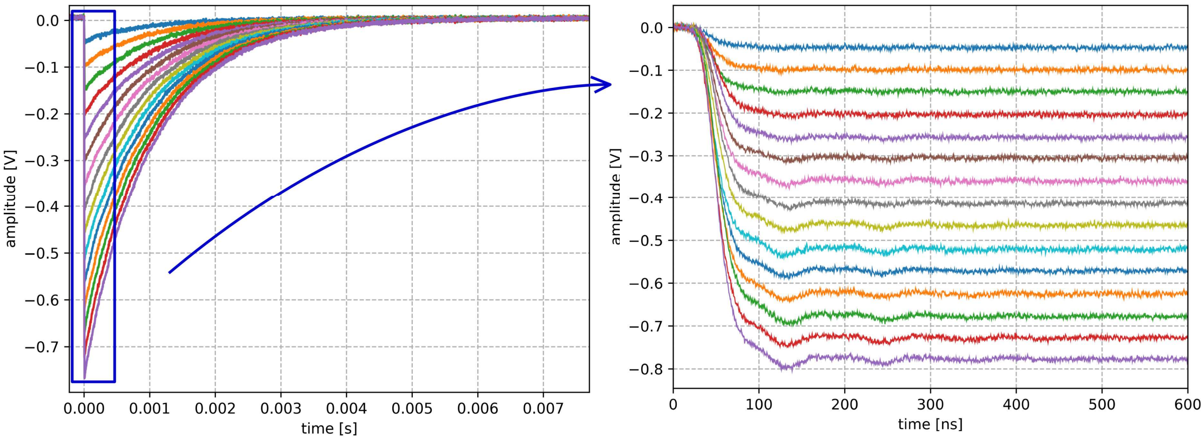

Figure 4.48: CSP output waveforms for injected pulses with equivalent energy between 1 MeV and 15 MeV. A 15 pF detector capacitor was connected between the input node of the circuit and ground. The left panel shows the full signal shape, while the right panel zooms in on the rising edges. A slight ringing is visible, however the overall signal integrity is maintained.

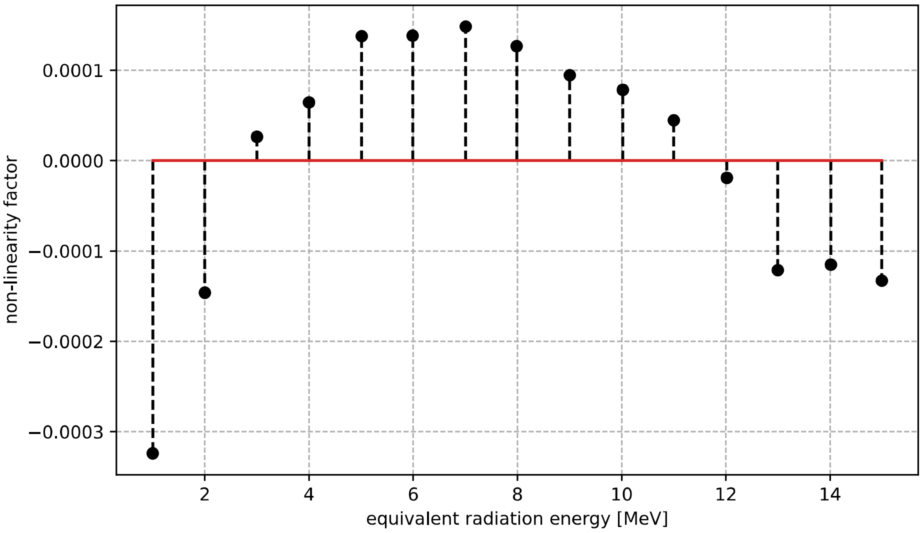

Figure 4.49: Measured non-linearity factors over the 15 MeV equivalent energy range of interest for the high-resolution gamma spectroscopy experiments. An integral non linearity factor just over 0.3 ‰was found.

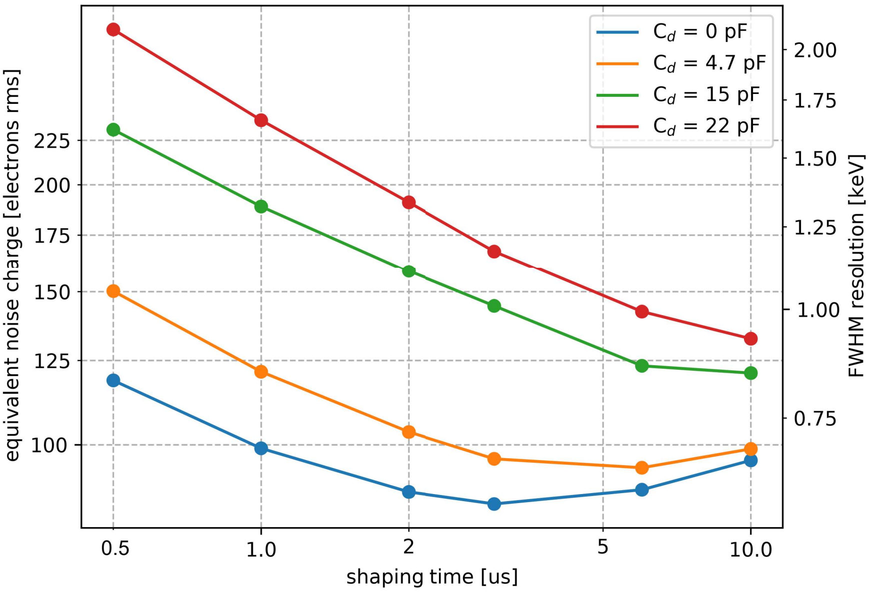

Figure 4.50: CSP equivalent noise charge and energy resolution measurements. Different capacitors were connected between the CSP input node and ground to simulate different electrodes capacitances. The ASIC was tested on a PCB with PTFE substrate.

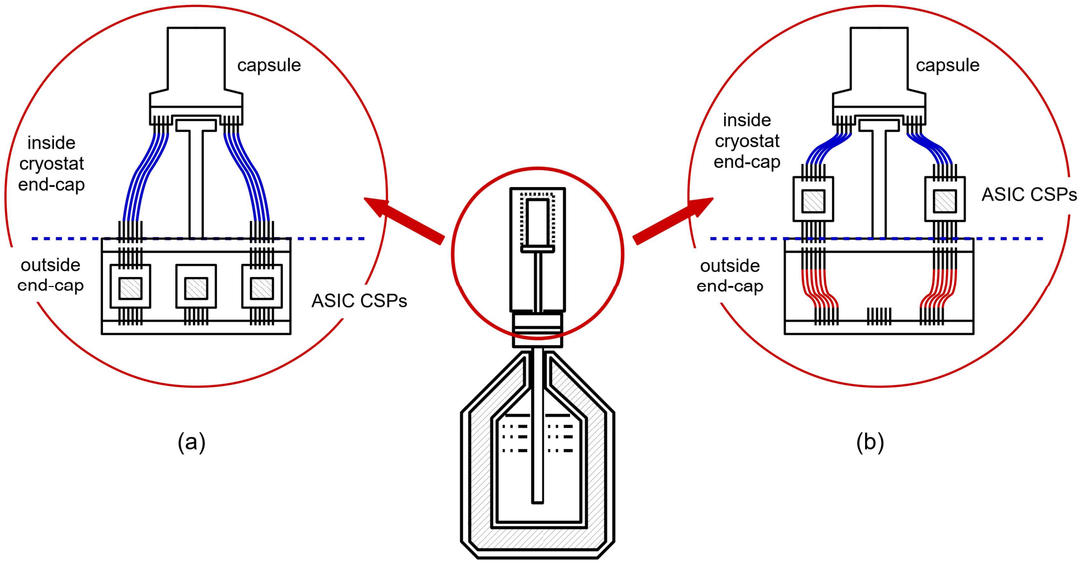

Figure 4.51: Mounting strategies for integrated electronics in the cryostats available at the Legnaro National Laboratories. On the left, configuration with the electronics installed in the warm section, currently hosting state-of-the-art discrete-component preamplifiers. On the right, configuration with the electronics mounted in the cryostat's cold section, while maintaining strong thermal coupling with the external environment. Constantan wires are used to minimize thermal transfer between the detector and the preamplifiers.

4.5 ASIC assembly within the cryostat

The ASIC's low power consumption and area compactness open up the possibility of exploring alternative mounting strategies for charge sensitive preamplifiers within the cryostat.

One potential approach involves placing the integrated circuits along with their PCB in the warm section of the cryostat, which currently houses their discrete-component counterparts[11], as illustrated in Fig. 4.51(a). Owing to the monolithic nature of an ASIC, no additional circuit elements would be required in the cold section. In this configuration, the capsule feed-throughs could be directly connected to the cryostat ones using constantan wires of length between $10\,\mathrm{cm}$ and $15\,\mathrm{cm}$. Unfortunately, this solution introduces parasitic inductance and capacitance at the preamplifier input node due to the relatively long wire length, potentially degrading the signal integrity.

On the other side, an alternative configuration, shown in Fig. 4.51(b), places the ASIC and the PCB directly within the cold section of the cryostat. In this scenario the circuit is mounted onto the electrical feed-throughs located on the cryostat flange, allowing for efficient thermal coupling with the external environment. This mechanical arrangement ensures that the ASIC operates close to room temperature despite being physically located inside the cryogenic volume.

Signal lines from the detector capsule are connected to the ASIC input nodes via constantan wires. The use of constantan, a material with low thermal conductivity, is critical in this configuration, as it minimizes heat flow from the warmer ASIC to the colder detector region. This thermal decoupling preserves the detector's cryogenic operating

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[11] For a comprehensive discussion of the state-of-the-art front-end electronics, the reader is invited to refer to section 1.1.1

conditions while allowing the front-end electronics to function near room temperature[12], where their performance is more stable and predictable[13]. Furthermore, by reducing the distance between the ASIC and the detector to just a few centimeters, this configuration significantly shortens the input signal path. As a result, it mitigates parasitic inductance and capacitance that typically arise in longer connections. This reduction in parasitic leads to improved signal quality and lower noise pickup that are especially relevant in high-resolution systems. Experimental validation of this innovative setup is currently being carried out at the Legnaro National Laboratories.

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[12] In our setup, we have a printed circuit board with at least two copper layers, to which a constantan wire is soldered. One end of the PCB is maintained at room temperature, while the free end of the constantan wire is at approximately 130 K. The large difference in thermal conductivity between constantan ($\approx 20\,\mathrm{W\,m^{-1}\,K^{-1}}$) and copper ($\approx 400\,\mathrm{W\,m^{-1}\,K^{-1}}$), combined with the fact that the constantan wire diameter is equal to $0.1\,\mathrm{mm}$, ensures that the PCB remains essentially at room temperature. This thermal behavior exemplifies a well-known problem in heat transfer theory, commonly referred to as the pin fin or heat fin problem. Here, the constantan wire acts as a thermal fin connecting a cold environment to a warmer thermal mass (the PCB). Due to its low thermal conductivity and small cross-sectional area, the wire presents a significant thermal resistance, minimizing heat flow and thus limiting the temperature drop along the PCB itself.

[13] Simulation software for integrated circuits can accurately predict device behavior down to approximately -40°C. Below this temperature, however, reliable transistor models are generally unavailable, as most standard device models do not account for the physical phenomena occurring at cryogenic temperatures. This limitation represents a major challenge in designing ASICs capable of stable operation in cryogenic environments. To address this gap, our research group has initiated a comprehensive characterization campaign of the AMS C35B4C3 transistor technology at liquid nitrogen temperatures. The goal is to extract and develop accurate transistor models that capture the device physics under cryogenic conditions. These refined models will then be integrated into circuit simulators, enabling predictive and reliable ASIC design for cryogenic applications.

Conclusion

This work describes the successful development and test of a complete system that combines mechanical structures, electrical interconnections and custom integrated electronics to support the operation of advanced high-purity germanium detectors.

As part of this system, an innovative interconnection scheme was implemented using custom-designed flexible printed circuit boards fabricated on ultra-thin polyimide substrates. This solution provides a reliable and solder-free electrical connection to the fragile detector electrodes, while maintaining excellent mechanical and thermal stability. Compared to conventional spring–indium methods, it significantly reduces leakage current, leading to improved noise performance and long-term operational reliability.

Complementing the interconnection system, a custom cylindrical aluminum capsule was engineered to serve both as a mechanical housing and as an infrared radiation shield, with internal components tailored for high mechanical compliance, minimal thermal stress and compatibility with cryogenic operation. The use of ceramic and polymeric materials for internal structures and the integration of a porous getter contribute to long-term vacuum integrity and mechanical robustness under various environmental conditions.

Finally, the front-end electronic was implemented using a novel ASIC charge sensitive preamplifier fabricated in the AMSC35B4C3 $350\,\mathrm{nm}$ CMOS process. The circuit demonstrated outstanding linearity (0.3 ‰over a $15\,\mathrm{MeV}$ range) and low noise (ENC = 108 electrons rms at a shaping time $\tau = 10\,\mu\mathrm{s}$ and considering a detector capacitance C_d = $15\,\mathrm{pF}$), all comparable to the best discrete-component preamplifiers currently in use, allowing to reach excellent energy resolution ($0.75\,\mathrm{keV}$ FWHM). The integrated nature of the ASIC offers significant advantages in terms of compactness and power efficiency, paving the way for future integration within the cryostat and closer coupling to the detector element.

Taken together, these results validate a complete and scalable solution for next - generation HPGe detection systems. The design approaches developed here, particularly in mechanical encapsulation, low-noise interconnects and front-end electronics, are not only directly applicable to gamma spectroscopy but also provide a foundation for broader application in other high-resolution radiation detection technologies, where mechanical robustness, low power and high performance are essential.

Part of this work was presented at the PRIME 2025 (20^{th} International Conference on PhD Research in Microelectronics and Electronics) conference and was distinguished as one of the top 10% contributions, highlighting the relevance and impact of the proposed solutions within the scientific community.

APPENDIX A

Green's Reciprocity Theorem

Let's consider independently two different charge distributions, $\rho_1(\mathbf{r})$ and $\rho_2(\mathbf{r})$, and their associated potentials, $V_1(\mathbf{r},t)$ and $V_2(\mathbf{r},t)$, as reported in Fig.A.1.

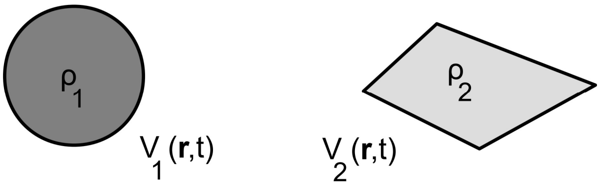

Figure A.1: Independent distributions of charge and associated potentials.

Given the two electric fields, $\mathbf{E}_1$ and $\mathbf{E}_2$, it follows that:

$$\begin{aligned} \int (\mathbf{E}_1 \cdot \mathbf{E}_2) d^3\mathbf{r} &= \int -\nabla V_1 \cdot \mathbf{E}_2 d^3\mathbf{r} = -\int \mathbf{E}_2 \cdot \nabla V_1 d^3\mathbf{r} \\ &= -\int \big[\nabla \cdot (V_1\mathbf{E}_2) - (\nabla \cdot \mathbf{E}_2)V_1\big] d^3\mathbf{r} \\ &= \int \left[\frac{\rho_2(\mathbf{r})}{\varepsilon_0} V_1 - \nabla(-(\nabla V_2)V_1)\right] d^3\mathbf{r} \\ &= \frac{1}{\varepsilon_0}\int \rho_2(\mathbf{r}) V_1 d^3\mathbf{r} + \int \nabla \cdot ((\nabla V_2)V_1) d^3\mathbf{r} \end{aligned} \tag{A.1}$$

The following vector relation has been employed:

$$\nabla \cdot (f\mathbf{A}) = (\nabla \cdot \mathbf{A})f + \mathbf{A} \cdot (\nabla f) \tag{A.2}$$

According to the divergence theorem, the last term on the right-hand side of Eq.A.1 cancels out, as the integral is evaluated over all space. As a consequence,

$$\int (\mathbf{E}_1 \cdot \mathbf{E}_2) d^3\mathbf{r} = \frac{1}{\varepsilon_0}\int \rho_2(\mathbf{r}) V_1 d^3\mathbf{r} \tag{A.3}$$

Following the same approach of Eq.A.1 and expressing $\mathbf{E}_2$ as the gradient of V_2, we can write:

$$\int (\mathbf{E}_1 \cdot \mathbf{E}_2) d^3\mathbf{r} = \int \mathbf{E}_1 \cdot [-(\nabla V_2)] d^3\mathbf{r} = \ \dots \ = \frac{1}{\varepsilon_0}\int \rho_1(\mathbf{r}) V_2 d^3\mathbf{r} \tag{A.4}$$

From the combined results of Eq.A.1 and Eq.A.4, one obtains:

$$\int \rho_1(\mathbf{r}) V_2(\mathbf{r},t) d^3\mathbf{r} = \int \rho_2(\mathbf{r}) V_1(\mathbf{r},t) d^3\mathbf{r} \tag{A.5}$$

APPENDIX B

Noise in Dielectric Materials

Let's consider a linear dielectric subjected to a harmonic electric field, **E**(t):

$$\mathbf{E}(t) = \mathrm{Re}\left\{\mathbf{E}_0 \cdot e^{j\omega t}\right\} \tag{A.1}$$

The electric displacement **D**(t) is the product of the electric field and the medium dielectric constant, ϵ:

$$\mathbf{D}(t) = \mathrm{Re}\left\{\epsilon\mathbf{E}_0 \cdot e^{j\omega t}\right\} \tag{A.2}$$

The electric field transfers to the medium an average power given by the following expression:

$$\begin{aligned}\langle P\rangle &= \langle \mathbf{E}(t) \cdot \frac{d}{dt}\mathbf{D}(t)\rangle \\ &= \langle \mathrm{Re}\left\{\mathbf{E}_0 \cdot e^{j\omega t}\right\} \cdot \mathrm{Re}\left\{\frac{d}{dt}\epsilon\mathbf{E}_0 \cdot e^{j\omega t}\right\}\rangle \\ &= \langle \mathrm{Re}\left\{\mathbf{E}_0 \cdot e^{j\omega t}\right\} \cdot \mathrm{Re}\left\{j\omega\epsilon\mathbf{E}_0 \cdot e^{j\omega t}\right\}\rangle\end{aligned} \tag{A.3}$$

Since the following mathematical relation holds,

$$\langle \mathrm{Re}\left\{A \cdot e^{j\omega t}\right\} \cdot \mathrm{Re}\left\{B \cdot e^{j\omega t}\right\}\rangle = \frac{1}{2}\mathrm{Re}\left\{A \cdot B^*\right\} = \frac{1}{2}\mathrm{Re}\left\{A^* \cdot B\right\}, \tag{A.4}$$

we can write:

$$\langle P\rangle = \frac{1}{2}\mathrm{Re}\left\{\mathbf{E_0} \cdot (j\omega\epsilon\mathbf{E_0})\right\} = \frac{1}{2}\mathrm{Re}\left\{j\omega\epsilon E_0^2\right\} \tag{A.5}$$

In a non-ideal medium, the electric field dissipates a non-zero amount of power. Consequently, its dielectric constant must be a complex function:

$$\epsilon = \epsilon' - j\epsilon'' \tag{A.6}$$

Let us now consider a non-ideal parallel-plate capacitor. Based on what has just been discussed, its capacitance, C, can be expressed as follows:

$$C = \epsilon\frac{S}{d} = (\epsilon' - j\epsilon'')\frac{S}{d} \tag{A.7}$$

where S is the plate surface and d is the distance between plates. To this capacitor, we can associate the following admittance Y:

$$\begin{aligned}Y &= j2\pi f \cdot \epsilon_0(\epsilon_r' - j\epsilon_r'')\frac{S}{d} \\ &= j2\pi f \cdot \epsilon_0\epsilon_r'\frac{S}{d} + 2\pi f \cdot \epsilon_0\epsilon_r''\frac{S}{d} \\ &= j2\pi f \cdot C + \frac{1}{R}\end{aligned} \tag{A.8}$$

Therefore, the non-ideal capacitor with losses can be modeled as an ideal lossless capacitor in parallel with a resistor that accounts for the power dissipated by the electric field within the dielectric medium:

$$C = \epsilon_0 \epsilon_r' \frac{S}{d} \qquad R = \frac{d}{2\pi f \epsilon_0 \epsilon_r'' S} \tag{A.9}$$

By defining the loss-factor $\tan\delta$ as follows:

$$\tan\delta = \frac{\epsilon''}{\epsilon'}, \tag{A.10}$$

we can rewrite R:

$$R = \frac{1}{2\pi f C \tan\delta} \tag{A.11}$$

This resistor is a noise source, referred to as dielectric noise, to which we associate a current noise power spectral density given by:

$$S_i(f) = \frac{4kT}{R} = 4kT(2\pi)C\tan\delta \cdot f = \lambda C f \tag{A.12}$$

As can be observed, $S_i(f)$ is proportional to the frequency, exhibiting the same behavior that characterizes the flicker noise.

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List of Publications

- S. Capra, G. Secci and A. Pullia, ”An Innovative Analog Circuit to Retrieve Energy Information From Signals of Deeply Saturated Preamplifiers Connected to Semiconductor Detectors,” in IEEE Transactions on Nuclear Science, vol. 69, no. 7, pp. 1757-1764, July 2022, doi: 10.1109/TNS.2022.3178760.
- S. Capra, G. Secci, B. Million, L. Manara, S. Coelli, M. Citterio, D. De Salvador, W. Raniero, D.R. Napoli and A. Pullia, ”Front-End Electronics and Mechanical Developments for the N3G Project.” 2022 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC). IEEE, 2022.
- S. Capra, G. Secci and A. Pullia, ”Effects of Different Spectroscopic Filtering Techniques on the Noise Produced by Charge-Sensitive Pre-amplifiers with Feedback Resistors Characterized by High Distributed Capacitance.” 2022 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC). IEEE, 2022.
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Patents

- L. Manara, S. Coelli, G. Secci, and S. Capra, “Container for radiation detector and detector apparatus”, Italian patent 102023000009687 (WO2024236424A1), granted on 2025-03-29.