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Self-Assembled Nanodielectrics for Solution-Processed Top-Gated Amorphous IGZO Thin Film Transistors

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Keywords: amorphous IGZO, hybrid dielectrics, low-voltage electronics, top-gate thin film transistor, solution processing, unconventional electronics

Abstract

Metal oxide semiconductors, such has amorphous indium gallium zinc oxide (a-IGZO), have made impressive strides as alternatives to amorphous silicon for electronics applications. However, to achieve the full potential of these semiconductors, compatible unconventional gate dielectric materials must also be developed. To this end, solution-processable self-assembled nanodielectrics (SANDs) comprised of structurally well-defined and durable nanoscopic alternating organic (e.g., stilbazolium) and inorganic oxide (e.g., ZrO_x, HfO_x) layers offer impressive capacitances and low processing temperatures ($T \leq 200$ °C). While SANDs have been paired with diverse semiconductors and yielded excellent device metrics, they have never been implemented in the most technologically relevant top-gated thin-film

transistor (TFT) architecture. Here we combine solution-processed a-IGZO with solution-processed four-layer Hf-SAND dielectrics to fabricate top-gated TFTs, which exhibit impressive electron mobilities (μ_{SAT} = 19.4 cm^2 V^{-1} s^{-1}) as well as low threshold voltages (V_{th} = 0.83 V), subthreshold slopes (SS = 293 mV/dec), and gate leakage currents (10^{-10} A), as well as high bias stress stability.

Introduction

Solution-processing of functional electronic materials for optoelectronic devices is a viable emerging strategy for technologies that require large-area coverage, low manufacturing cost, and/or mechanical flexibility.[1-3] Representative applications include display backplanes, radio-frequency identification tags, smart windows, and high-volume sensor arrays.[3] To this end, several diverse electronically active and passive material systems are emerging, including organics, metal oxides, nanomaterials, and organic-inorganic hybrids. Achieving the optimum combination of semiconductors, dielectrics, contacts, interconnects, encapsulation/passivation, and substrates, with the most suitable architectures for a given application, is currently one of the key challenges in this rapidly developing field.[4-6]

Two promising solution phase approaches recently developed for the low-temperature growth of high-performance dielectric and semiconductor films are, respectively, the self-assembly of organic-inorganic hybrid nanodielectrics (SANDs)[7-8] and the combustion synthesis of metal oxides.[9-10] SANDs feature nanolayers of inorganic oxide dielectrics such as SiO_x, ZrO_x, and HfO_x, interleaved with highly polarizable conjugated organic molecules, e.g., phosphonic acid derivatives of stilbazolium salts, which undergo self-assembly onto the inorganic nanolayers. This durable materials platform provides high gate capacitances in TFT devices, lower gate leakage currents than the neat solution-processed inorganic films, chemical and thermal stability, suppression of trapped charge, radiation hardness, and dielectric

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thicknesses ideal for device scaling.[7-8, 11] Combustion synthesis of metal oxide films has been shown to lower the processing temperature requirements for the growth of diverse semiconducting oxides, including In_2O_3, In-Zn-O, and In-Ga-Zn-O (IGZO).[9, 12] This is achieved by including an oxidizer (e.g., NO_3^-) and a fuel (acetylacetone) in the metal oxide precursor solution, which promotes a highly exothermic film growth reaction, thereby achieving efficient oxide network condensation and carbon impurity removal.[9]

The broad compatibility of SANDs with diverse semiconductors has been demonstrated with pentacene,[7] printed IGZO,[13] graphene,[11] and carbon nanotubes.[14] These pairings have yielded impressive TFT mobilities and other important device metrics. Furthermore, the advantages are not limited to the broad array of compatible unconventional semiconductors, but also in the tailorability of the SAND structure itself in regards to both the inorganic[6-8] and organic components.[15-16] Note that IGZO is currently the most important manufactured metal oxide semiconductor material, and sputtered IGZO TFTs have been implemented in many commercial devices.[3] In previous studies, we demonstrated combustion synthesis as a route to high-quality amorphous-IGZO (a-IGZO) films from precursor solutions.[17-18] Furthermore, we showed that the combination of combustion processed a-IGZO with HfO_x based SAND (Hf-SAND) in a bottom-gated top-contact TFT architecture affords impressive device metrics such as $\mu_{SAT} = 20.6 \pm 4.3$ cm^2 V^{-1} s^{-1}, $V_{th} = 0.0$ V, on current to off current ratio (I_{on}:I_{off}) of 10^7, and SS = 125 mV/dec.[13] Interestingly, the question of why a-IGZO/Hf-SAND devices afford superior TFT performance over analogous devices fabricated with a-IGZO and similar thicknesses of ALD HfO_2 (μ_{SAT} = 2 cm^2 V^{-1} s^{-1}) is not currently resolved but indicates that there are additional performance enhancements from Hf-SAND which likely reflect charge-trapping effects moderated by the polar organic layers.[11]

Top-gated TFT devices offer many attractions over bottom-gate architectures, especially for metal oxide semiconductors.[19-20] Oxides are well known to react with atmospheric oxygen

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and water, and top-gated structures enable the dielectric to passivate the oxide surface by functioning as an encapsulation layer, thus making device response more uniform.[21-24] Top-gate IGZO TFTs have been reported with several classes of insulators including polymers and metal oxides. Polymer dielectrics offer mechanical flexibility and solution processing at low temperatures; however they typically exhibit low dielectric constants (*k*), excessive gas/H_2O permeability, and limited thermal stability.[7, 25-26] Inorganic dielectrics offer high-*k*s and environmental stability but generally require either capital-intensive vacuum deposition or high annealing temperatures, which can compromise the underlying semiconductor.[7, 25-26] While solution-processed SANDs combine many of the attractions of both inorganic and organic dielectrics and minimize many of their limitations,[5, 7-8, 26] they have never been implemented in top-gated devices due to fabrication challenges.

In this contribution, we demonstrate the first use of solution-processed SANDs in top-gate bottom-contact (TG-BC) oxide TFT structures. We first establish that SANDs can be grown successfully on combustion-processed a-IGZO films while preserving well-defined nanostructures, as verified by optical spectroscopy (UV-Vis), AFM, X-ray reflectivity (XRR), and cross sectional-TEM measurements. In addition, Hf-SAND dielectric properties are assessed in metal-insulator-metal device structures via impedance spectroscopy. Finally, top-gate a-IGZO/Hf-SAND TFTs are fabricated and are shown to exhibit impressive device metrics such as a $\mu_{SAT} = 19.4 \pm 0.5$ cm^2 V^{-1} s^{-1}, $V_{th} = 0.83 \pm 0.04$ V, $\log(I_{on}:I_{off}) = 4.26 \pm 0.31$, and SS $= 293 \pm 22$ mV/dec.

Results and Discussion

Hf-SAND on IGZO Growth. Figure 1 shows the fabrication scheme for top-gate bottom-contact a-IGZO/Hf-SAND TFT devices with further details reported in the Experimental section. Briefly, chromium/gold source and drain contacts were evaporated on SiO_2 substrates using photolithography, where the chromium serves as an adhesion layer for the gold.

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Combustion processed a-IGZO was then deposited by spin-coating the precursor solution followed by a brief annealing step (20 min) at 300 °C. Oxalic acid was used to etch/pattern the a-IGZO channel. The initial HfO_x priming layer needed for the assembly of the four-layer Hf-SAND film was deposited by spin-coating and then annealed at 200 °C. The HfO_x layers are not combustion processed like the a-IGZO. Previous Hf-SAND work used XPS to compare the O 1s peak in films processed at both 150 °C and 300 °C, which were found to be similar and dominated by Hf-O-Hf network.[6] The XPS measurements also showed that there was no remaining chloride in the film and that despite the low processing temperature good quality HfO_x layers were formed.[6] The organic stilbazolium constituent, 4-[[4-[bis(2-hydroxyethyl)amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl) benzyl]pyridinium bromide (PAE), was self-assembled onto the HfO_x priming layer. The PAE self-assembly was followed by the deposition of a thin HfO_x capping layer. The PAE/capping-HfO_x deposition steps were then repeated another three times. Each capping-HfO_x and PAE deposition forms an inorganic/organic bilayer. The thin HfO_x layers are not self-assembled onto the PAE layers as the oxide is deposited by spin-coating not

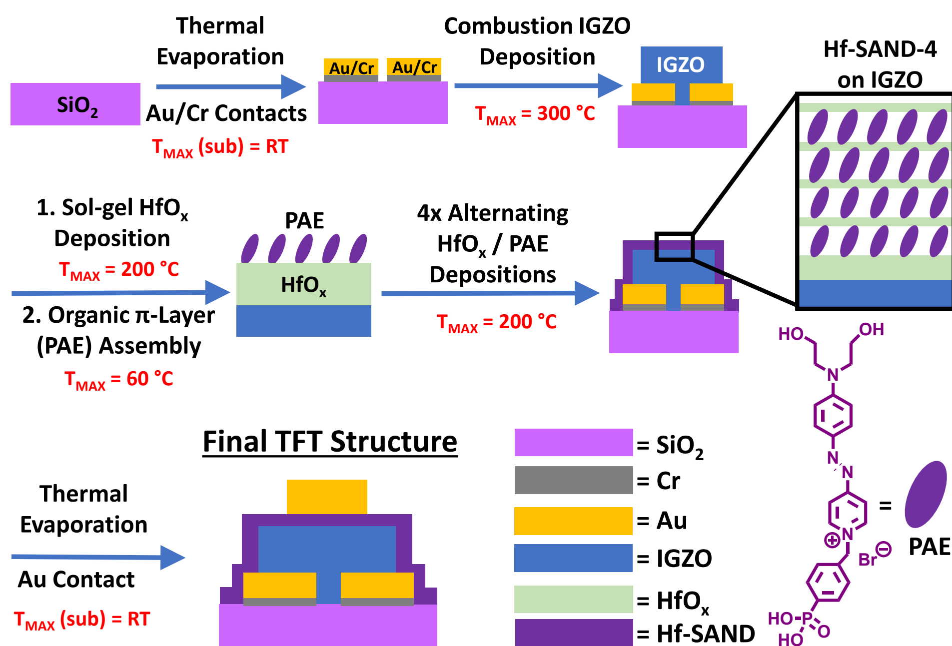

Figure 1. Fabrication scheme for top-gate a-IGZO/Hf-SAND-4 TFTs. The maximum processing temperature of each step is indicated. Note that components are not drawn to scale.

immersion. However, the terminal hydroxyl groups of the PAE are expected to react with the capping HfO_x layer subsequently spin-coated onto the organic layer, which doubtless contributes to the robust character of the multilayer SAND structures. The deposition of the thicker HfO_x priming layer followed by a total of four bilayers comprises the Hf-SAND-4 gate dielectric employed here. Finally, gold gate electrodes are photolithographically patterned and evaporated to complete the TFT structures.

Hf-SAND on a-IGZO Characterization. Before TFT device fabrication, the Hf-SAND films were characterized using UV-Vis optical absorption spectroscopy, AFM, x-ray reflectivity (XRR), and cross sectional-TEM (CS-TEM). Although SANDs of different types have been fabricated on glass and doped Si substrates for bottom-gated TFTs,[6, 13] it was not obvious that gate insulator quality Hf-SAND films could be grown on a-IGZO. It was expected that PAE would self-assemble directly onto the IGZO surface.[27-28] However previous work comparing zirconia-based SAND (Zr-SAND) and Hf-SAND indicated that the composition of the metal oxide affects the self-assembly in terms of regular surface coverage. Hf-SAND had a 30% greater surface coverage compared to Zr-SAND resulting in an overall higher *k* for the PAE layers.[6] Since good surface coverage of PAE is essential to the further SAND layer growth and electrical performance, a thin HfO_x priming layer was utilized in this work.

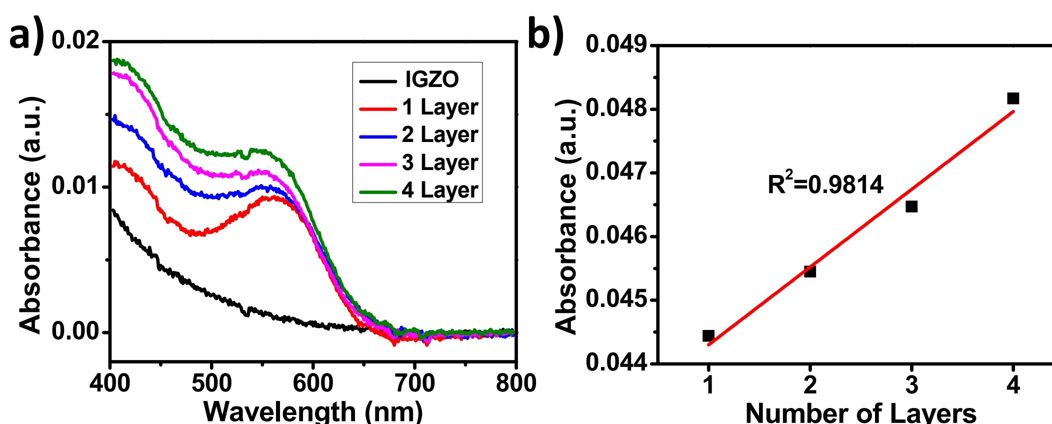

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Figure 2. a) UV-Vis absorption spectra of Hf-SAND films on a-IGZO/ITO. b) Optical absorption of Hf-SAND films at 575 nm vs. number of layers.

Additionally, the fabrication of top-gated structures requires intricate patterning not necessary for the simple common bottom-gate TFTs fabricated previously,[6-8, 11, 13] further challenging Hf-SAND processing. Thus, a-IGZO coated glass substrates (~8 nm thick deposited by spin-coating combustion synthesis) were first investigated for sequential Hf-SAND film bilayer growth and the resulting films characterized by UV-Vis spectroscopy. The absorption spectra in Figure 2 verify the uniform layer-by-layer growth of the SAND multilayer stack on a-IGZO. Thus, the absorption increases linearly at 575 nm, where PAE absorption is greatest (Fig 2b), indicating that uniformly oriented PAE molecules assemble in effectively equal densities on each sublayer, as is seen in previous analysis of Zr-SAND growth on glass.[7] The Hf-SAND spectra show a slight shift in the PAE peak maxima to lower wavelengths as the number of layers increase which may reflect slight changes in chromophore aggregation and/or tilt angle.

Next, AFM images of Hf-SAND on a-IGZO/Si substrates were used to assess the SAND surface topology after each bilayer deposition step. The underlying a-IGZO has a rms roughness of only 0.184 nm (Figure S1), which is consistent with previously reported combustion-processed metal oxide films.[9, 29-31] As shown in Figure 3, the films remain continuous and smooth after each bilayer deposition and, as expected, have slightly greater roughnesses than in bottom-gate structures.[6] The rms roughnesses for the top-gate Hf-SAND samples are 0.329 nm for one bilayer, 0.266 nm for two bilayers, 0.356 nm for three bilayers, and 0.253 nm for four bilayers, while the previously reported roughness values for bottom-gate

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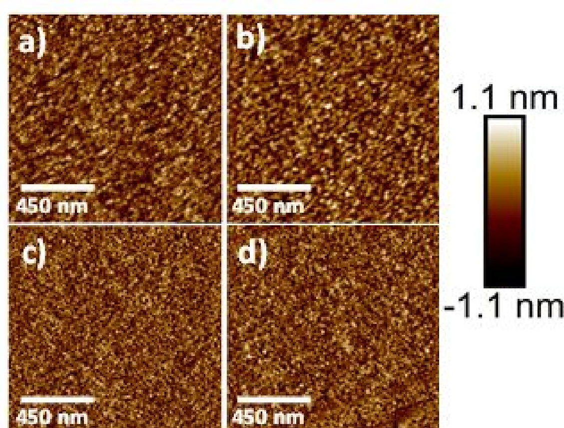

Figure 3. AFM images of Hf-SAND on IGZO. (a) Hf-SAND-1 layer rms: 0.329 nm, (b) Hf-SAND-2 layer rms: 0.266 nm, (c) Hf-SAND-3 layer rms: 0.356, and (d) Hf-SAND-4 layer rms: 0.253 nm. Note that Si substrates are used here.

Hf-SAND multilayers are 0.13-0.17 nm for one - four bilayers.[6] The exceptionally smooth Hf-SAND surfaces assembled on a-IGZO indicates the overall good quality of the films and that the interfaces between the semiconductor and dielectric layers are likely to be excellent with negligible defects, which is essential to minimize carrier scattering and ensure good TFT metrics.[32]

XRR (x-ray reflectivity) measurements, which provide film electron density profiles in the surface normal direction, were next used to evaluate the Hf-SAND film growth regularity on two layers of combustion-processed a-IGZO. The initial out-of-plane scattering data ($q = 4\pi\sin\theta/\lambda$) and the subsequent best fit model are shown in Figure S2a. The electron density profile was additionally normalized to the electron density of the underlying Si (ρ_{Si}) substrate (Figure S2b). The electron density profile in Figure 4 reveals the clearly defined alternating pattern of the lower and higher electron density regions in Hf-SAND-4 corresponding to the PAE and hafnia layers, respectively, as seen in previous SAND studies.[6-8] The appearance of the uniform periodic variations between organic and inorganic layers further demonstrates that SAND film growth has excellent regularity, which is not compromised by assembly on the a-

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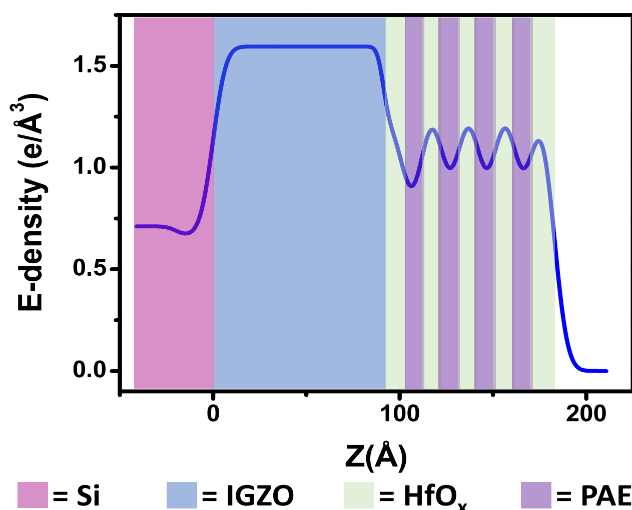

Figure 4: The XRR electron density profile vs. height (z) above the Si surface. The reflectivity data clearly show the growth of well-defined alternating hafnia and PAE layers. The priming hafnia layer blends into the electron density of the underlying a-IGZO. Note, two layers of a-IGZO were spin-coated onto a Si substrate for this experiment.

IGZO surface. The capping hafnia layers and PAE layers are on average 1.05 nm and 1.08 nm thick, respectively, so that one bilayer is ~2.13 nm. The priming HfO_x layer is about 1.82 nm thick, which is slightly thinner than might be expected. However, the exact thickness of the priming layer is difficult to determine as its electron density peak blends into that of the a-IGZO. The complete Hf-SAND-4 dielectric multilayer consisting of a priming layer and four-bilayers (PAE/capping HfO_x) has a total thickness of ~10.1 nm, which is slightly smaller than Hf-SAND-4 structures previously grown on Si substrates (~13 nm).[6] From the electron density and thickness of the organic layers, the surface coverage is estimated to be ~0.025 PAE molecules/Å^2, consistent with previous results on stilbazolium-based molecules self-assembled on Si/SiO_2.[33] PAE has a molecular length of ~1.5 nm which is larger than the experimental PAE layer thickness (1.08 nm) which reflects a PAE molecule tilt of ~40° with respect to the surface normal, as found in other SAND derivatives.[8,9] The XRR derived interfacial roughnesses (~0.27 - 0.68 nm) are consistent with those determined by AFM (*vide supra*; Table S1).

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Finally, CS-TEM imaging (Figure 5a and Figure S3) elucidates the final top-gate TFT structure and the good quality of the a-IGZO/Hf-SAND interface. The bright area in the upper right corner corresponds to the SiO_2 substrate on which the TFTs were fabricated. Since the

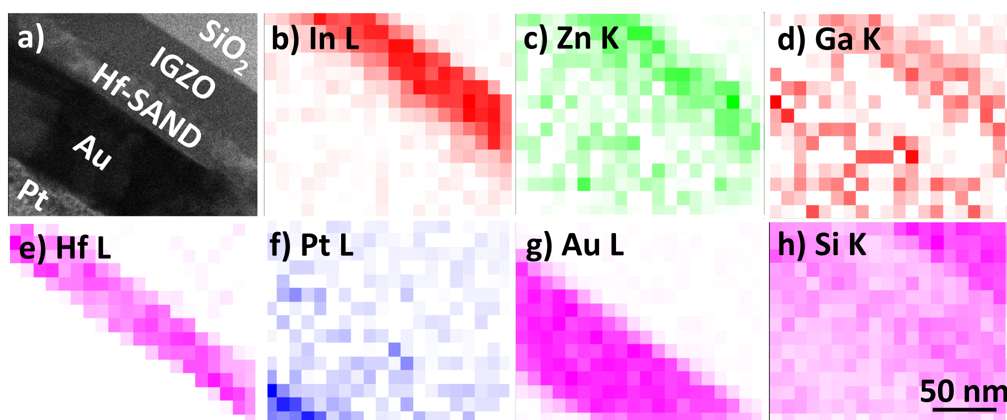

Figure 5. (a) Cross-sectional TEM image of the top gate Hf-SAND TFT. EDS elemental mapping images of (b) indium, (c) zinc, (d) gallium, (e) hafnium, (f) platinum, (g) gold, and (h) silicon of the CS-TEM image of top gate SAND TFT (a).

semiconductor is grown by combustion synthesis with multiple spin-coating/annealing steps to achieve film densification and the desired thickness,[9, 34] the CS-TEM image clearly shows the multilayer character of the a-IGZO structure. In the Hf-SAND dielectric region, the alternating layers of low and high scattering contrast corresponding to the HfO_x and PAE layers, respectively, are also clearly visible (Figure S3). However, SAND is more sensitive to X-ray beam damage, so the layers are not as well-defined as those in the a-IGZO. Based on the CS-TEM, the approximate thicknesses of the Hf-SAND-4 and a-IGZO (12 spin-coated) layers are 16 nm and 38 nm, respectively. These thicknesses are both in the expected range for the respective layers, thus further confirming the good SAND growth on a-IGZO. The Hf-SAND-4 is thicker in the CS-TEM than the XRR (~16 nm vs. ~10.1 nm). This is likely due, in part, to the differences in the TFT substrate used for the CS-TEM and the Si/a-IGZO substrate used for the XRR. For the CS-TEM substrate the contacts and a-IGZO were already fabricated and patterned when the Hf-SAND was deposited. Therefore, the HfO_x layers in the final TFT

sample are at a greater distance from the annealing heat source, potentially resulting in slightly less oxide layer densification. Again, the full thickness of the priming HfO_x layer is difficult to determine from the XRR due to the blending of the a-IGZO electron density with that of the HfO_x priming layer.

The identities of the Hf-SAND-4 layers were further confirmed by energy dispersive spectroscopy (EDS) mapping, revealing that In, Hf, and Au are present in the expected regions. The lighter elements Zn, Ga, and Si are more dispersed but are detected in the anticipated areas (Figures 5b-h). Therefore, it is confirmed that Hf-SAND growth on solution processed a-IGZO is eminently feasible with no significant differences versus growth on thermal Si/SiO_x substrates.

SAND Electrical Characterization. Before performing transport measurements on top-gate TFTs, the dielectric characteristics of the Hf-SAND-4 multilayers were assessed in metal-insulator-metal (MIM) capacitors. MIM devices were fabricated on ITO (bottom electrode) substrates with thermally evaporated gold contact pads (200 μm × 200 μm, top electrode) on the Hf-SAND-4 films. The capacitance and leakage properties were evaluated using a two-point probe station with a Signatone “cat-whisker” tungsten probe on the contact pads. To obtain accurate capacitances for Hf-SAND-4, it was essential to prepare MIM device structures as opposed to the metal-insulator-semiconductor (MIS) structures used in previous Hf-SAND studies.[6] The latter capacitance value is limited by the native SiO_x layer especially if the Si substrate is not in complete accumulation within the voltage range of the measurement.[5] The Hf-SAND-4 on ITO samples exhibit a capacitance of 732 ± 45 nF/cm^2 at 2.5 V (Figure 6a and Figure S4), which is higher than that previously reported for Hf-SAND-4 on Si (610 nF/cm^2)

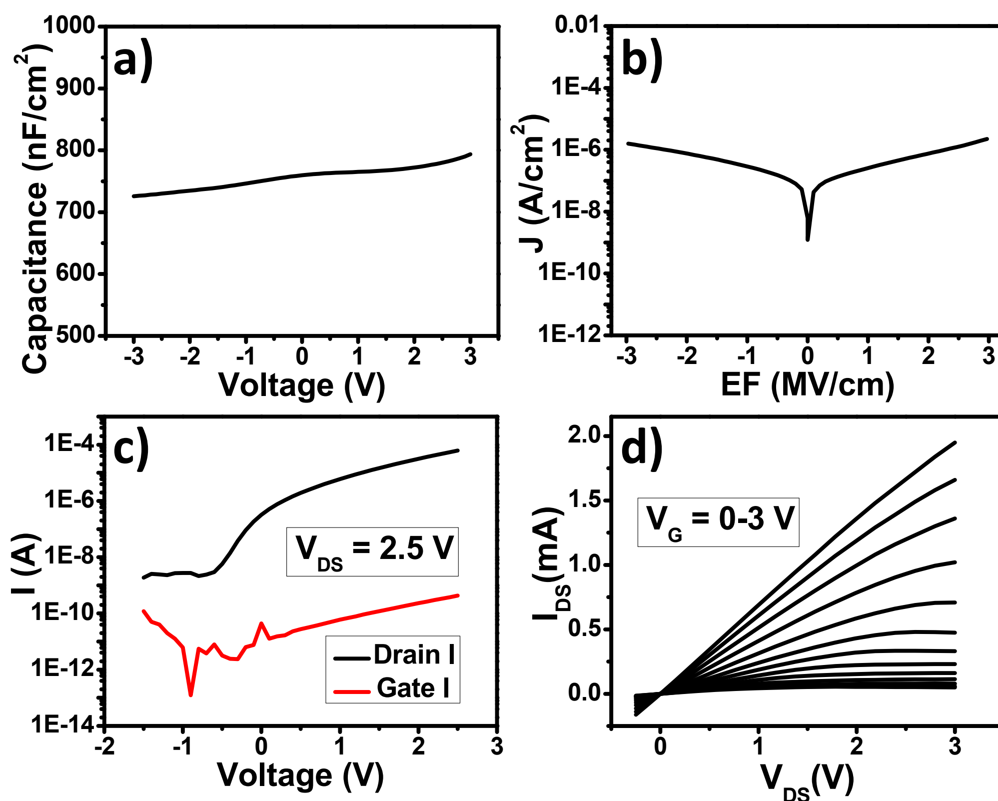

Figure 6. a) Representative capacitance curve at 10 kHz and b) leakage current of Hf-SAND-4 on ITO. c) Log transfer and d) output plots for top-gate a-IGZO/Hf-SAND-4 TFTs.

due to the limiting effects of the substrate.[6] The k_{eff} value for the Hf-SAND-4 on ITO fabricated here is 13.89. An additional advantage of Hf-SAND on ITO, and thus the similar environment of the present top-gate TFT structure as well, is that the Hf-SAND-4 capacitance varies by only ~8% (65 nF/cm^2) over a -3 to 3 V range. Capacitance-frequency measurements show a gradual decline in capacitance as the frequency increases with a sharp drop near 10^6 Hz (Figure S5). The capacitance averages were 845 nF/cm^2 at 1 kHz, 759 nF/cm^2 at 10 kHz, and 708 nF/cm^2 at 100 kHz. Leakage current densities (J-V) were also measured for the MIM devices. The leakage current at 2 MV/cm is 7.41×10^{-7} A/cm^2. While at the extremes of the bias window (-2.97 MV/cm to 2.97 MV/cm), the leakage current densities are in the low-10^{-6} A/cm^2 range, consistent with previous Hf-SAND-4 devices (Figure 6b, Figure S6, and Table S2).[6] Considering the large contact pads, especially when compared to the dielectric thickness used in these measurements, it is evident that Hf-SAND-4 fabricated on ITO is essentially pinhole-free and of high quality.

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Next, the top-gate a-IGZO/Hf-SAND-4 TFT (L = 50 μm, W =150 μm) properties were evaluated. The TFT I-V curves (Figure 6c and Figure S7) exhibit the expected linear and saturation behavior. Using the Hf-SAND-4 on ITO capacitance value of 732 nF/cm^2, the average saturation electron mobility is found to be 19.4 ± 0.5 $cm^2 V^{-1} s^{-1}$. The small variance in the capacitance from -3 to 3 V means that the mobility varies by less than 6% for the entire capacitance range. The most direct comparison for the top-gate TFTs materials presented here is previous work using Hf-SAND-4 and printed combustion processed a-IGZO in a bottom-gate top-contact device geometry.[13] In both sets of devices the a-IGZO was annealed at 300 °C. Note that the previous bottom gate devices were unpatterned and had a (common) doped Si bottom gate and Al as the top source/drain contacts. The average saturation mobility of the printed devices, 20 $cm^2 V^{-1} s^{-1}$, is very similar to that achieved in the current work, and further demonstrates the integrity of both the solution-processed a-IGZO and Hf-SAND-4 in a top-gate device configuration, despite the more complex fabrication process.[13] For the present top-gate a-IGZO/Hf-SAND-4 devices, the average threshold voltage (V_{th}) is 0.83 ± 0.04 V, and the small operating voltage range (-1.5 V to 2.5 V) is desirable for most technological applications.[6, 8, 13, 35] The present TFTs also exhibit low gate leakage currents with maxima in the mid 10^{-10} A range. The average $\log(I_{on}:I_{off})$ and SS for the top gate devices are 4.26 ± 0.31 and 293 ± 22 mV/dec (Equation S1), respectively. Positive and negative bias stress tests indicate V_{th} shifts of ~0.1-0.2 V (Figure S9), which is common in a-IGZO TFTs.[36-38]

In a-IGZO films, oxygen vacancies and other defects play a significant role in device performance.[37, 39-41] Studies of a-IGZO films indicate that the role of oxygen vacancies and trap densities is highly dependent on the growth conditions such O_2 partial pressure and annealing parameters; the density of defects is expected to be higher in solution-processed films and their effects more evident.[39-40] Note that often the dielectric leakage current dictates the off current of a device. In the present case the top-gate a-IGZO/Hf-SAND-4 TFTs off current is a few

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orders of magnitude greater than the leakage current (Figure 6c and Figure S7) indicating significant defects. The layered structure of the a-IGZO seen in the cross sectional TEM (Figure 5) seems to indicate that there is variation in the oxide throughout the semiconductor. This could be due to the differing exposure of the layers to ambient during processing and is potentially a source of bulk trap states, however further investigation will be necessary to determine the extent and nature of the effects.[18, 42]

The subthreshold slope depends on both the bulk trap density (D_{bulk}) and the trap density of the interface (D_{it}). The D_{it} was calculated using the following equation:

$$D_{it} = \frac{C_i}{e^2}\left(\frac{eSS}{k_B T \ln(10)} - 1\right)$$

where C_i is the geometric capacitance of the dielectric, e is the elementary charge, SS is the subthreshold slope, k_B is the Boltzmann constant, and T is the temperature. This calculation of the trap density D_{it} assumes that $D_{bulk} = 0$. As noted above, the presence of bulk trap states is expected in both sputtered and solution processed a-IGZO. Regardless, this estimation of D_{it} gives an indication of the interface trap density. Comparing the trap densities of the present Hf-SAND devices and other a-IGZO TFTs from the literature indicates that Hf-SAND devices tend to have a higher trap density (1.18E+13 eV^{-1} cm^{-2}) than most comparable devices (Table S5). Higher D_{it} versus other devices in literature is not necessarily unexpected as the top-gated Hf-SAND-4 TFTs fabricated here are the first examples where both the semiconductor and dielectric were solution processed.

The interface trap density also has a significant impact on the hysteresis of a TFT. The hysteresis seen in the a-IGZO/Hf-SAND-4 devices (Figure S8) is in the anticlockwise direction, which is unusual since a-IGZO device hysteresis is typically in the clockwise direction.[37] In previous work using combustion processed IGZO, clockwise hysteresis is observed.[18] However the anticlockwise hysteresis behavior is also seen in the bottom-gate

printed a-IGZO devices on Hf-SAND-4 implying that the hysteresis is dominated by interactions with the Hf-SAND.[13] A threshold voltage shift (ΔV_{th}) of 1.86 V in the negative direction is observed between the forward and reverse sweeps of the top-gate TFTs, which is somewhat larger than that seen in the printed a-IGZO/Hf-SAND-4 bottom gate devices (Figure S8).[13] This is expected as the more complex fabrication process required for the top-gate devices may create more interfacial states. Additionally spin-coated combustion processed semiconductors are known to be porous particularly in the last layer applied, and is generally beneficial in the bottom gate architecture as successive layers can fill in the pores and potential defects of the previous layers.[10, 18] In the case of these top-gated devices, however, the last IGZO layer applied is that which forms the interface with the dielectric, and thus the porosity might be a source of traps. Further optimization of these promising devices should result in lowering the bulk and interfacial trap densities.

IGZO-SAND TFT Performance Comparison with the Literature. For greater context regarding IGZO top-gated devices, the a-IGZO/Hf-SAND-4 TFTs are compared to literature examples in Figure 7 and Tables S3 and S4. The highest mobility for top-gate IGZO transistors in the literature is 44.57 $cm^2\ V^{-1}\ s^{-1}$ reported by Hseich et al.[43] These devices were fabricated with a 300 nm SiN_x dielectric and IGZO layers deposited via PECVD and RF sputtering,

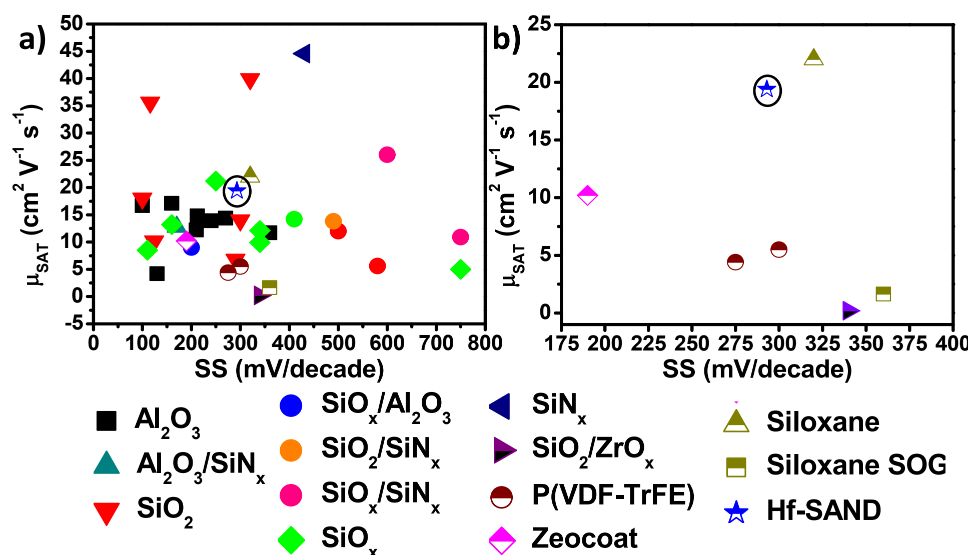

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Figure 7. a) Mobility vs subthreshold slope (SS) of literature top-gate IGZO TFTs for various dielectric materials.[19-20, 38, 43-70] b) Mobility vs. SS for IGZO TFTs with solution-processed dielectrics. The circular symbols represent linear mobilities. Symbols that are partially filled indicate solution-processed dielectrics. The black circles designate solution-processed semiconductors. See Tables S3 and S4 for more complete fabrication information and literature TFT metrics.

respectively.[43] Another impressive mobility of 39.9 cm^2 V^{-1} s^{-1} was reported for devices fabricated with a PEALD-deposited SiO_2 dielectric and sputtered IGZO.[60] Additional large literature mobilities are 35.6 cm^2 V^{-1} s^{-1}, 26 cm^2 V^{-1} s^{-1}, 22 cm^2 V^{-1} s^{-1}, and 21.20 cm^2 V^{-1} s^{-1} produced by top-gate top-contact (TG-TC) devices with 10 nm RF sputtered SiO_2 and a buried ITO layer in the a-IGZO via RF sputtering, TG-BC devices with a sputtered SiO_x/SiN_x dielectric, TG-TC transistors utilizing a 250 nm spin-coated siloxane dielectric, and coplanar contact devices with a 150 nm SiO_x dielectric, respectively.[54, 59, 66, 69] All of the aforementioned devices used sputtered IGZO. Impressively, the present Hf-SAND devices yield the 7th highest mobility (μ_{SAT} = 19.4 cm^2 V^{-1} s^{-1}) out of 31 literature examples, while being the only TFTs fabricated from both solution-processed dielectric and semiconductor layers.

The performance of the present Hf-SAND transistors is impressive in the context of all reported top-gate IGZO devices, but especially so in comparison to TFTs with spin-coated dielectrics. Lee et al. reported TG-TC RF sputtered a-IGZO devices with a spin-coated 110 nm poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] dielectric, having a linear mobility of 5.5 cm^2 V^{-1} s^{-1}. The P(VDF-TrFE) layer is >10x thicker than Hf-SAND dielectric but has higher leakage currents, 2.2×10^{-6} A/cm^2 at 2 MV/cm and 7.41×10^{-7} A/cm^2 at 2 MV/cm, respectively.[68] Zeocoat, another polymer dielectric, was used by Toda et al. to produce TG-TC transistors with DC magnetron-sputtered IGZO, where the mobility was 9.8 cm^2 V^{-1} s^{-1} and the V_{th} was -1.3 V.[71] The highest mobility for a solution-processed dielectric with a sputtered IGZO film was 22 cm^2 V^{-1} cm^{-1} reported by Kulchaisit et al. These devices had a TG-TC structure with RF magnetron sputtered a-IGZO and a spin-coated siloxane dielectric. The siloxane

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devices additionally had a V_{th} = 5.6 V, a SS of 320 ± 10 mV/decade, and an I_{on}:I_{off} of ~10^6. The 250 nm thick siloxane layer had gate leakage currents comparable to the ~16 nm Hf-SAND during TFT operation.[69] However, the siloxane layer required annealing at 300 °C -- 100 °C higher than for Hf-SAND. Thus, the combination of combustion-processed a-IGZO and Hf-SAND-4 in TG-BC TFTs yields impressive mobilities versus all previous top-gate IGZO TFTs, especially those with solution-processed dielectrics, and is the only example in the peer-reviewed literature of solution-processed semiconductor + solution-processed dielectric pairing. These results are especially significant given the general desire for the manufacturing of optoelectronic devices to transition from capital-intensive vapor deposition techniques to more cost-effective solution-based ones.[1-4] In addition to the results presented here, the potential use of solution processed SANDs in manufacturing is further strengthened by the recent development of printed SANDs.[16]

The well-known sensitivity of a-IGZO to atmospheric effects is known to contribute to device instability and is a major attraction of top-gated devices.[37, 48, 66] Numerous studies have reported improved environmental stability of top-gate a-IGZO TFTs using a variety of dielectric materials.[41, 43, 60, 69] It is therefore expected that the top-gated SAND TFTs will have superior environmental stability compared to bottom-gated devices. A further advantage of the solution processed Hf-SAND used here is limiting a-IGZO damage by high-energy dielectric deposition techniques such as sputtering.[19, 60, 67] The confirmed viability of SAND in top-gate TFT structures also opens possibilities for further work on SAND-based device durability, such as long-term stability testing, an important step for deeper of understanding the properties of this unconventional hybrid dielectric.

Conclusions

This investigation demonstrates that Hf-SAND gate dielectrics can be successfully self-assembled from solution in top-gate TFT architectures using combustion-processed a-IGZO as

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the underlying channel layer. Characterization of Hf-SAND films grown on a-IGZO via UV-Vis spectroscopy, AFM, XRR, and CS-TEM demonstrates that the robust, regular SAND nanostructure is preserved under the processing conditions required for top-gate TFT fabrication. These solution-processed a-IGZO/Hf-SAND top-gate devices exhibit impressive mobilities of 19.4 $cm^2 V^{-1} s^{-1}$ with low (<1 V) operating voltages, low gate leakage currents (10^{-10} A), and a good SS of 293 mV/dec. As SAND has already shown extensive durability and versatility in terms of well-matched semiconductors, this newly confirmed compatibility with top-gate structures further expands the uses and applications of this effective unconventional dielectric family.

Experimental Section

SAND Film Fabrication. The $HfCl_4$ (99.9+%, sublimated, Sigma Aldrich) was stored under vacuum when not being used to prevent the absorption of water. An initial 0.1 M HfO_x solution was prepared with 93.7 mg $HfCl_4$ and 4 mL of 100% ethanol. The solution was stirred at room temperature for five min before the addition of 264 μL nitric acid. The 0.1 M solution was stirred at 50 °C for 3 h and then at 25°C for at least 12 h. The initial 0.1 M HfO_x solution was then diluted to 0.01 M or 0.02 M HfO_x using absolute ethanol. The diluted solutions were aged while stirring for at least 30 min. ITO substrates were sonicated in acetone, hexanes, and absolute ethanol for at least 10 min each before being plasma cleaned for 5 min at 400-500 mTorr. SAND growth was carried out in a HEPA-filtered laminar flow clean hood (NuAire) which contained plasma cleaning, spin coating, annealing, and self-assembly apparatus. All HfO_x solutions were filtered through a 0.2 μm Teflon syringe filter during the spin-coating process. The 0.02 M HfO_x was spin-coated directly onto the ITO substrates at 5000 rpm for 30 s to produce the HfO_x primer layer. The substrates were then annealed at 200 °C for 20 min. The PAE used for the organic layer was synthesize in this Laboratory as previously described.[7] A 3.0 mM solution of PAE in methanol was used for the organic layer self-assembly. The

primer layer coated substrates were submerged in the PAE solution at 60 °C for 1 h. The substrates were then sonicated in methanol for a 5 min before being individually sonicated in fresh methanol for 1 min. The capping layer was next spin-coated with the 0.01 M HfO_x solution on top of the organic layer and annealed in the same manner as the primer layer. These steps were repeated to achieve four-layer SAND stacks. Additional SAND structures were produced on Si/SiO_2 substrates for the AFM and XRR characterization and on glass for UV-Vis measurements. These substrates were prepared with two layers of combustion-processed a-IGZO before the SAND deposition. The a-IGZO preparation is described in the transistor fabrication and characterization method section.

SAND Film Characterization. X-ray reflectivity (XRR) measurements were performed on a 9 kW Rigaku Smartlab Workstation. X-rays were generated from the Cu rotating anode (X-ray wavelength is 1.542 Å) and collimated to produce a monochromated X-ray beam with dimension 0.1x5 mm and flux ~3 x 10^8 cps at the sample surface. The XRR data were modeled and fitted by using the Motofit package[72] to obtain electron-density profiles, which contain information on the thickness, electron density, and interfacial roughness of each layer. UV-Vis spectra of SAND films on ITO substrates were obtained on a Varian Cary 50 Scan spectrophotometer. AFM measurements were made on a Bruker Dimension FastScan AFM. Cross-sectional transmission electron microscopy (CS-TEM) images were collected using a JEOL JEM-2100F transmission electron microscope. The CS-TEM samples were prepared directly from actual TFT devices with standard focused ion beam (FIB) milling techniques (FEI Helios NanoLab 600). A ~2 μm thick platinum layer was deposited prior to the ion milling to protect samples from ion beam damage.

SAND Film Electrical Measurements. Metal-insulator-metal (MIM) capacitors were fabricated on four-layer Hf-SAND stacks on ITO substrates. Gold contacts (200 μm × 200 μm) were deposited via thermal evaporation (Denton evaporator) through shadow masks. An Agilent

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B1500A semiconductor parameter analyzer was used for MIM characterization under ambient. A flexible tungsten whisker probe (SE-SM, Signatone) served as the cathode while a beryllium-copper alloy probe (SE-BC, Signatone) served as an anode for the capacitance vs voltage (C-V) curves and the leakage current density vs voltage (J-V) curves. The C-V curves were performed at 10 kHz. The C-f curves (1 kHz to 100 kHz) where measured using an Agilent B1500A, while the curves ranging from 100 Hz to 100 kHz where performed using a Biologic SP-1500.

Transistor Fabrication and Electrical Measurements. Cr/Au (5 nm/30 nm) source-drain contacts were sputtered (Denton) at a base pressure of 3×10^{-6} Torr onto silicon substrates with a 300 nm thermal oxide layer (WRS) and patterned by lift-off using a Suss MABA6 Mask Aligner (L_{ds} = 50 µm, W_{ds} =150 µm). All solution materials were obtained from Sigma-Aldrich unless otherwise stated. The following metal salts were used indium (III) nitrate hydrate [$In(NO_3)_3 \cdot xH_2O$], gallium (III) nitrate hydrate [$Ga(NO_3)_3 \cdot xH_2O$], and zinc nitrate hydrate [$Zn(NO_3)_2 \cdot xH_2O$]. All salts were 99.999% pure by trace metals basis and stored under vacuum when not in use. The IGZO precursor solutions were prepared by dissolving $M(NO_3)_3$ in 2-methoxyethanol to produce 0.05 M solutions (10 mL, M = In, Ga, Zn). The addition of 32 µL acetylacetone (≥99%) and 30 µL NH_3 (28% NH_3 in H_2O, ≥99.99 trace metals basis) was performed immediately to each solution. The solutions were aged for ~16 h before being mixed in the correct atomic ratio (72.5:7.5:20 In:Ga:Zn). The substrates with the patterned contacts were sonicated in ethanol for 10 min before being plasma-cleaned for 5 min (400-500 mTorr) in preparation for spin-coating. The final IGZO solution was passed through a 0.2 µm Teflon filter as part of the spin-coating process. The IGZO was deposited at 3500 rpm for 30 sec and annealed at 300 ˚C in air for 20 min. The spin-coating and annealing was repeated 12 times to achieve the desired semiconductor thickness. The IGZO was then photolithographically patterned and etched with oxalic acid (10% in water) to isolate the devices. The four-layer Hf-

SAND was grown as described in the previous section. Au gate electrodes (40 nm) were deposited and patterned by lift-off. The completed TFTs were evaluated using an autoprober to test the devices with automatic sorting and parameter extraction. I–V measurements were made with a Keithley 4200. The standard field effect transistor model was used to extract the saturation regime carrier mobilities (μ). Output plots were performed using an Agilent B1500A semiconductor parameter analyzer. The bias stress devices were made in a separate batch than the TFTs in the basic I-V measurements and were left to relax in the dark for at least 1 h and annealed at 60 °C for 30 mins, after being engaged. All devices were tested in ambient atmosphere and temperature. The TFT metrics were obtained from the average of 8 devices across two batches.

ASSOCIATED CONTENT

Supporting Information. AFM of IGZO on Si substrate, XRR of Hf-SAND-4 on IGZO with best fit, XRR derived roughness, CS-TEM of Hf-SAND-4 TFT, additional C-V data, C-f data, additional I-V data, table of leakage values at various EF, additional saturation transfer plots, $I_{DS}^{1/2}$ vs. voltage plot with V_{th} extrapolation, forward and reverse sweep transfer plots, SS formula, bias stress data, and tables of IGZO TFT metrics from literature.

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Notes

The authors declare no competing financial interest.

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