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Recent developments on CMOS MAPS for the SuperB Silicon Vertex Tracker

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ABSTRACT

In the design of the Silicon Vertex Tracker for the high luminosity SuperB collider, very challenging requirements are set by physics and background conditions on its innermost Layer0: small radius (about 1.5 cm), resolution of 10−15 μm in both coordinates, low material budget $<1\%X_0$, and the ability to withstand a background hit rate of several tens of MHz/cm^2. Thanks to an intense R&D program the development of Deep NWell CMOS MAPS (with the ST Microelectronics 130 nm process) has reached a good level of maturity and allowed for the first time the implementation of thin CMOS sensors with similar functionalities as in hybrid pixels, such as pixel-level sparsification and fast time

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stamping. Further MAPS performance improvements are currently under investigation with two different approaches: the INMAPS CMOS process, featuring a quadruple well and a high resistivity substrate, and 3D CMOS MAPS, realized with vertical integration technology. In both cases specific features of the processes chosen can improve charge collection efficiency, with respect to a standard DNW MAPS design, and allow to implement a more complex in-pixel logic in order to develop a faster readout architecture. Prototypes of MAPS matrix, suitable for application in the SuperB Layer0, have been realized with the INMAPS 180 nm process and the 130 nm Chartered/Tezzaron 3D process and results of their characterization will be presented in this paper.

1. Silicon vertex tracker and layer0

The high luminosity SuperB asymmetric e^+e^- collider, to be built by the Cabibbo-Lab in the University of Rome "Tor Vergata" campus, has been designed to deliver a luminosity greater than 10^{36} cm^{-2} s^{-1} with moderate beam currents and a reduced center of mass boost with respect to earlier B-Factories ($\beta\gamma = 0.24$ compared to $\beta\gamma = 0.55$ of BaBar). The Conceptual Design Report [1] has been published and reviewed by an international committee in 2007, Design Progress Reports on the major parts of the project have been written [2], and the Technical Design Report is now in preparation.

The Silicon Vertex Tracker (SVT) is crucial for the SuperB physics program to provide the vertex resolution needed both for time-dependent measurements and for physics background rejection. An improved vertex resolution is required for precise time-dependent measurements in order to compensate the reduced boost and retaining the proper time-difference resolution for B decays achieved in BaBar ($\Delta t \simeq \Delta z/(\beta\gamma c)$).

The SuperB SVT design (Fig. 1) is based on the BaBar vertex detector layout, with five layers of double sided silicon strip detectors, with the addition of a sixth layer (Layer0) closer to the interaction point.

Stringent requirements are imposed on Layer0 design by physics studies [2]: small radius (about 1.5 cm), resolution of 10−15 μm in both coordinates, and low material budget ($< 1\%X_0$). An example of the studies performed with a fast simulation program is illustrated in Fig. 2. Here the resolution on the proper time difference (Δt) is shown for $B^0 \to \phi K^0_S$ events, for different Layer0 radii and as a function of the total Layer0 material, compared to the reference value obtained in BaBar.

Background considerations influence several aspects of the SVT design: readout segmentation, electronics shaping time, data transmission rate and radiation hardness. The different sources of background have been simulated with a detailed Geant4-based detector model and beamline description [1,2]. According to these studies the track rate at the Layer0, at a radius of about 1.5 cm, is about 2 MHz/cm^2, corresponding to a much larger requirement on the target hit rate of 100 MHz/cm^2, including loopers (multiple crossing of the low p_t background tracks with the sensors, about 2.5), the average cluster multiplicity (about 4) and a safety factor of 5 on the nominal background conditions. The equivalent neutron fluence for nominal background is about 5×10^{12} n/cm^2/yr, and the dose rate expected is about 3 Mrad/yr.

Several options are under evaluation for the Layer0 technology. The current baseline configuration for the beginning of data taking is based on striplets, high resistivity sensors with short strips, which is a mature technology and has been shown [2,3] to provide good physics performance thanks to the low material budget associated (i.e. no readout electronics in the active area). However an upgrade to hybrid pixels [4] or thinner CMOS Monolithic Active Pixel Sensor (MAPS) is planned at the full luminosity run, being the pixel options more robust against background occupancy. For this purpose the SuperB interaction region and the SVT mechanics will be designed to ensure rapid access to the detector for a relatively fast replacement procedure of the Layer0.

Recent results on the development of CMOS MAPS suited for application in Layer0 are reviewed in the rest of the paper.

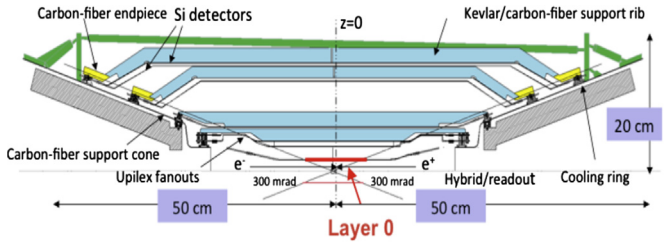

Fig. 1. Longitudinal section of the SVT.

2. Deep NWell CMOS MAPS

CMOS MAPS are very appealing for application in Layer0 where the material budget is critical: in this technology the sensor and readout electronics share the same substrate that can be thinned down to several tens of microns. In order to overcome the readout speed limitation of standard CMOS sensor, not adequate for Layer0 hit rates, an original new Deep NWell MAPS design approach has been developed in the last few years in the framework of the SLIM5 collaboration [3].

The DNW MAPS approach takes advantage of the properties of triple well structures to realize a sensor with relatively large area (as compared to standard three transistor MAPS) readout by a classical processing chain for capacitive detectors.

The concept of the DNW design approach is shown in Fig. 3: the sensor realized with a buried N-type layer collects the charge released

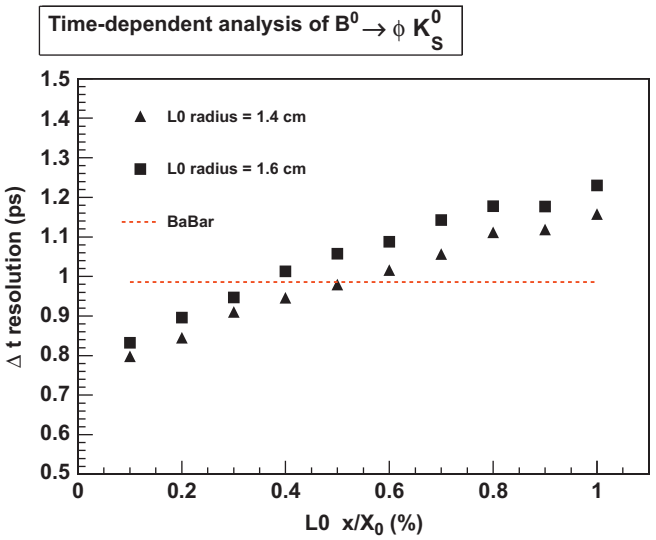

Fig. 2. Resolution on the proper time difference of the two B mesons (Δt), for $B^0 \to \phi K^0_S$ events. Different Layer0 configurations are considered in terms of radius $r_1 = 1.4, 1.6$ cm and material budget $(0.1-1.0)\%X_0$, compared with the reference value of BaBar (dashed line). In the simulation the beam pipe was set at radius of 1 cm with a total material of about $0.45\%X_0$.

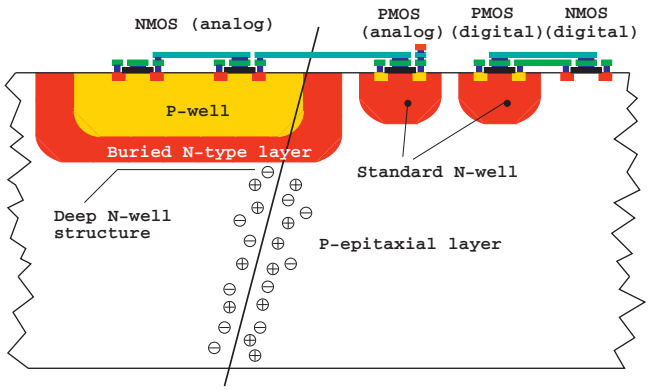

Fig. 3. Simplified cross-section of a DNW MAPS.

by the impinging particle and diffusing through the substrate, whose active volume is limited to the uppermost 20−30 μm thick layer below the collecting electrode. Therefore, within this extent, substrate thinning is not expected to affect charge collection efficiency.

The area taken by the DNW collecting electrode can also be used to integrate the NMOS parts of the analog front-end inside the internal P-well. Having a large DNW collecting electrode allows to include in the pixel cell a small amount of standard N-well for PMOS devices, instrumental to the design of high performance analog and digital blocks taking full advantage of CMOS technology properties. Note that in standard MAPS design these competitive N-wells are not permitted, since they can subtract charge to the tiny collecting electrode and would jeopardize sensor operation. On the contrary in DNW MAPS a good charge collection efficiency could be achieved, even with the competitive N-wells in the design, maximizing the fill factor (ratio of the DNW area to the total area of N-wells).

Thanks to an intense R&D program the development of DNW CMOS MAPS (with the ST Microelectronics 130 nm process) has reached a good level of maturity and allowed for the first time the implementation of thin CMOS sensors with similar functionalities as in hybrid pixels, such as pixel-level sparsification and fast time stamping [5,6]. The last prototype realized, the APSEL4D chip, a 4k pixel matrix with 50×50 μm^2 pitch has been tested with beams [3] reporting a hit efficiency of 92%, related to the pixel cell fill factor, which is about 90% in the APSEL design.

Since radiation hardness is a critical issue for the application in Layer0, DNW MAPS have been characterized after exposure to ionizing radiation and to neutron irradiation. Some degradation of the noise, about 35%, was detected after irradiation up to 10 Mrad with gamma-rays from a ^{60}Co source [7], but the use of an enclosed layout approach is expected to reduce the effect of ionizing radiation. A significant degradation of the charge collected (about 50%) has been measured [8] after irradiation with neutron up to a fluence of about 7×10^{12} n/cm^2, corresponding to about 1.5 years of operation in the Layer0, as illustrated in Fig. 4.

In order to meet the Layer0 requirements MAPS performance improvements are currently under investigation with two different approaches: 3D CMOS MAPS, realized with vertical integration of homogeneous layers, and the use of the INMAPS CMOS process, featuring a quadruple well and an high resistivity substrate.

3. 3D DNW MAPS in CMOS vertical technology

The realization of 3D MAPS, using two CMOS layers interconnected with vertical integration technology, offers several advantages with respect to standard 2D MAPS.

As illustrated in Fig. 5, in these devices one CMOS tier is hosting the sensor with the analog front-end and the second tier

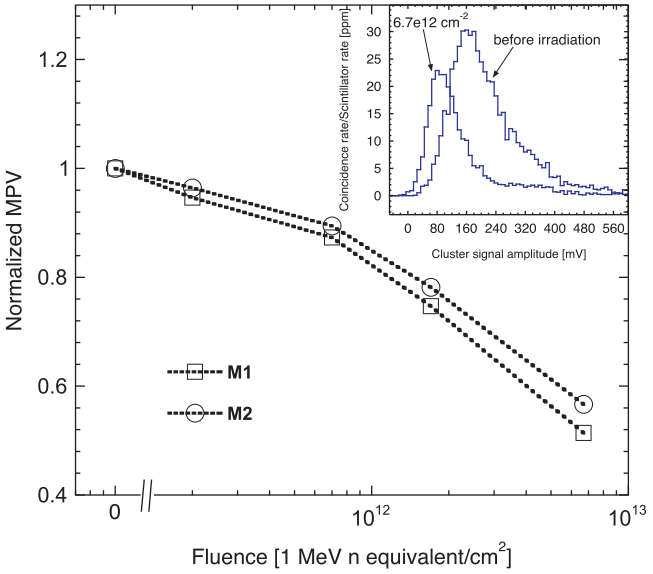

Fig. 4. Most probable value (MPV) of the ^{90}Sr spectra (shown in the inset before and after irradiation to a 6.7×10^{12} cm^{-2} neutron fluence) normalized to the pre-irradiation value as a function of the fluence for DNW MAPS with different sensor layout.

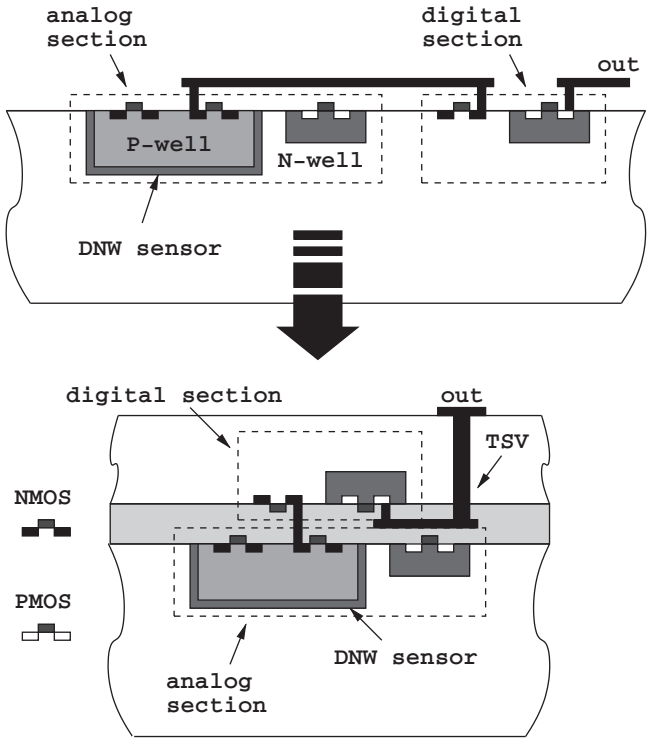

Fig. 5. Cross-section of a DNW CMOS MAPS: from a planar CMOS technology to a 3D process.

is dedicated to the in-pixel digital front-end and the peripheral readout logic. With this splitting of functionalities the collection efficiency can be improved, significantly reducing the N-Well competitive area in the sensor layer. Having more room for the in-pixel logic allows the implementation of a higher performance readout architecture. Finally in 3D MAPS the cross-talk between analog and digital blocks can be minimized.

Prototypes of 3D DNW CMOS MAPS have been designed and fabricated in the Chartered/Tezzaron technology [9], based on the vertical integration of two 130 nm CMOS layers of the Chartered

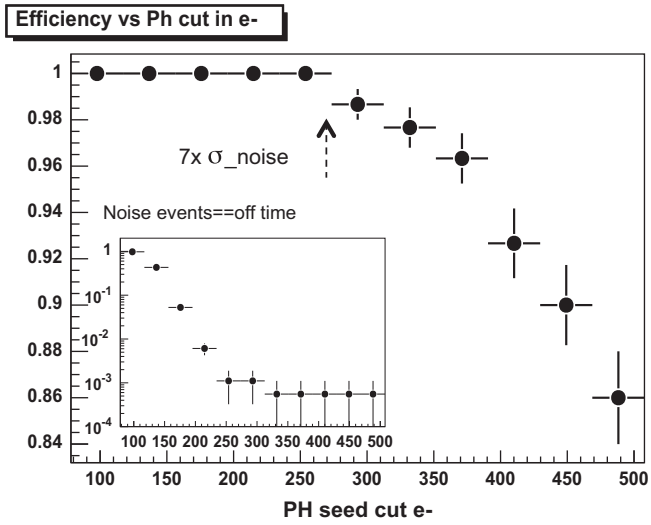

Fig. 6. Efficiency for hits on track on the sensor layer of 3D DNW MAPS as a function of the cut on the pulse height. The efficiency is above 98% for threshold values of 7 times the pixel noise.

Semiconductor process (now Globalfoundry). They include two small 3×3 matrices with analog output and a 8×32 matrix equipped with a digital readout circuit with data sparsification and time stamping features. In the 3D pixel cell, with 40 μm pitch, the fill factor has been increased up to 94% and the sensor layout has been optimized; according to device simulation collection efficiency above 98% is expected.

A number of different problems were encountered during fabrication of the first device batch. Among them, the misalignment between the two tiers prevented the analog and digital sections in each pixel cell to communicate to each other [10]. At this time other 3D wafers are being processed.

Tests on the CMOS layer hosting the sensor and the analog front-end, already available, allowed a first characterization of the process. Equivalent noise charge between 30 and 40 electrons and a charge sensitivity of about 300 mV/fC were measured. The 3×3 analog matrices have been tested on the PS beam at CERN and very promising results were obtained: the most probable value of the cluster signal for hits on track is about 1000 electrons and a hit detection efficiency above 98% has been measured, as displayed in Fig. 6.

3.1. Improved pixel readout architecture

An evolution of the readout architecture implemented in the 2D MAPS was developed [11] for the next 3D chip submission. Having more room for the in-pixel logic allowed to implement the latch of the TimeStamp (TS) at the pixel level when a hit occurs. The matrix readout is timestamp sorted and can be operated either in data push mode (selecting all the TS) or in triggered mode, where only triggered TS are readout.

With this architecture a TimeStamp of 100 ns can be used, greatly reducing the TS resolution with respect to standard CMOS sensor readout, where large frame readout are needed. For application in Layer0, where high rates are expected, a fast TS (<1 μs) is needed to reduce the module readout bandwidth to acceptable level (<5 Gbit/s). Full VHDL simulation of the readout has been implemented to test the performance on the full size matrix (1.3 cm^2) with a target Layer0 hit rate of 100 MHz/cm^2. Results from simulation showed that with a TS clock of 100 ns and a 50 MHz readout clock one can achieve efficiency above 99% for the data push architecture. Studies on the triggered architecture showed an efficiency of about 98%, for 6 μs trigger latency: in this configuration, where the pixel cell act as a single memory during the trigger latency, the associated pixel dead time dominates the inefficiency.

This new readout has been implemented in two devices in preparation for next 3D submission: a second prototype of a front-end chip for hybrid pixel (Superpix1, 32×128 pixels with 50×50 μm^2 pitch) and a larger MAPS matrix with the cell optimized for the vertical integration process (APSELVI, 128x100 pixels with 50×50 μm^2 pitch).

4. CMOS MAPS in quadruple well technology

In order to increase the charge collection efficiency a quadruple well 180 nm CMOS process, called INMAPS [12], is currently being explored. Fig. 7 shows a simplified cross-section of a pixel fabricated with the INMAPS process. By means of an additional processing step, a high energy deep P-well implant is deposited beneath the PMOS N-well containing in-pixel logic (and not under the N-well diode acting as collecting electrode). This implant creates a barrier to charge diffusing in the epitaxial layer, preventing it from being collected by the competitive N-wells and enabling a theoretical charge collection efficiency of 100%. The NMOS transistors are designed in heavily doped P-wells located in a P-doped epitaxial layer which has been grown upon the low resistivity substrate. The use of high resistivity epitaxial layer, also available in this process, can further improve charge collection and radiation resistance of INMAPS sensors with respect to standard CMOS devices.

The Apsel4well test chip, including 3×3 analog matrices with several diodes configurations, and a 32×32 digital matrix with the improved readout architecture described above, has been realized with different thickness (5−12 μm) and epitaxial layer resistivity (standard, about 50 Ω cm, and high resistivity, 1 kΩ cm).

In the Apsel4well pixel (50 μm pitch) the collecting electrode consists of 4 small interconnected Nwell diodes, readout by a channel similar to previous versions of DNW MAPS: including charge preamplifier, shaper, discriminator, and followed by the new in-pixel readout logic. With the new pixel design the total sensor capacitance is only about 30 fF, an order of magnitude smaller than in previous DNW pixels, allowing a reduction of almost a factor of 2 in power consumption (now 18 μW/pixel).

Preliminary results on the different INMAPS test structures realized showed very promizing results. In the 3×3 analog matrix equivalent noise charge of 30 e^- and gain of about 950 mV/fC were measured, both in good agreement with post layout simulation.

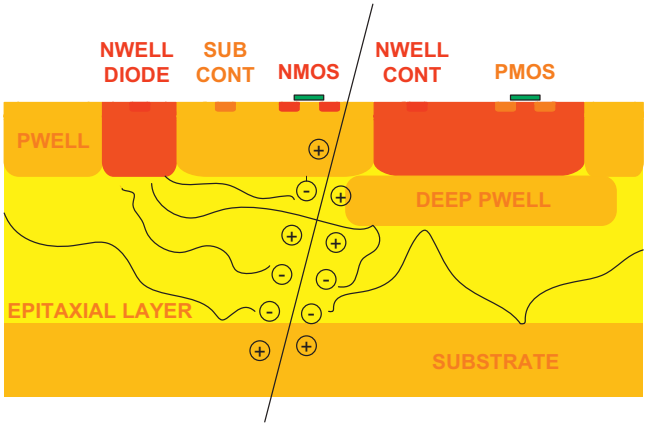

Fig. 7. Cross-sectional view of the INMAPS CMOS technology.

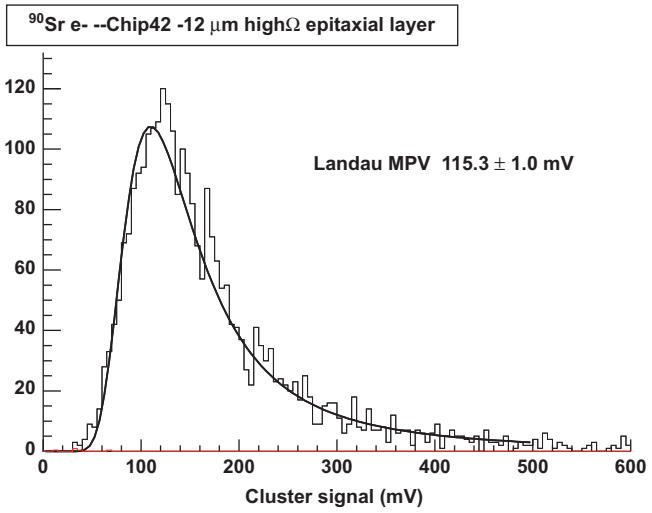

Fig. 8. Cluster signal for electrons from a ^{90}Sr source.

The characterization with laser and radioactive sources confirmed the deep p-well is beneficial in preserving charge collection by the small Nwell diodes, although most of the pixel area is now covered by competitive Nwells. In particular measurements with electrons from a ^{90}Sr source are shown in Fig. 8, for a chip with 12 μm high resistivity epitaxial layer. The cluster signal has been fitted with a Landau distribution with a MPV corresponding to about 930 e^- and giving a Signal-to-Noise of 27, considering the average pixel noise in the matrix.

Evaluation of the threshold dispersion and of the noise variation among pixels has been performed on the 32×32 digital matrix, measuring the hit rate as a function of the discriminator threshold. With a fit to the turn-on curve we report a threshold dispersion of about 7 mV, corresponding to about 2 times the average pixel noise of 30 e^-, and a noise variation of about 35% to 40% inside the matrix. These figures were obtained with a readout clock of 10 MHz, with no significant change in the performance with measurements done up to 100 MHz.

Specific tests on the 32×32 digital matrix were also performed to verify the new readout architecture in both the operation modes available on chip: data push and triggered. Both functionalities are working as expected with very similar performance verified with measurements of the pixel turn-on curve.

Radiation hardness of these devices is being investigated for application in SuperB. Irradiation with neutrons up to 10^{14} n/cm^2 has been performed and devices are currently under measurement with laser and radioactive sources.

4.1. Conclusions

In the SuperB Silicon Vertex Tracker, the Layer0, the innermost of the six SVT layers, has been added to improve the vertex resolution and compensate the reduced boost of the SuperB machine with respect to earlier B-Factories. Layer0 requirements on readout speed, material budget and resolution are very challenging for existing detectors. A Layer0 based on striplets modules, with short strips on high resistivity silicon sensors, is the baseline solution foreseen for the beginning of data taking; an upgrade to pixel sensors, more robust against high background occupancy, is planned at the full luminosity run. The development of DNW thin CMOS MAPS sensors with a fast readout, has now reached a good level of maturity. Further CMOS MAPS performance improvement are being explored to match all the Layer0 requirements with an intense R&D program, exploring 3D CMOS MAPS with vertical integration and 2D MAPS with the INMAPS quadruple well process. Very promizing results have been achieved with both approaches. In particular the Apsel4well INMAPS sensor seems to have the potential to solve the main limitations of DNW MAPS, in terms of collection efficiency and radiation hardness, with a reasonable timeline for application in SuperB.

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